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ZL50011

Flexible 512 Channel DX with on-chip DPLL

Data Sheet

September 2011

Features

- 512 channel x 512 channel non-blocking switch at 2.048 Mbps, 4.096 Mbps or 8.192 Mbps operation
- Rate conversion between the ST-BUS inputs and ST-BUS outputs
- Integrated Digital Phase-Locked Loop (DPLL) meets Telcordia GR-1244-CORE Stratum 4 specifications
- DPLL provides reference monitor, jitter attenuation and free run functions
- Per-stream ST-BUS input with data rate selection of 2.048 Mbps, 4.096 Mbps or 8.192 Mbps
- Per-stream ST-BUS output with data rate selection of 2.048 Mbps, 4.096 Mbps or 8.192 Mbps; the output data rate can be different than the input data rate
- Per-stream high impedance control output for every ST-BUS output with fractional bit advancement
- Per-stream input channel and input bit delay programming with fractional bit delay

Ordering Information

ZL50011/GDC	144 Ball LBGA	Trays
ZL50011QCG1	160 Pin LQFP*	Trays, Bake & Drypack
ZL50011GDG2	144 Ball LBGA**	Trays, Bake & Drypack

*Pb Free Matte Tin
** Pb Free Tin/Silver/Copper

-40°C to +85°C

- Per-stream output channel and output bit delay programming with fractional bit advancement
- Multiple frame pulse outputs and reference clock outputs
- Per-channel constant throughput delay
- Per-channel high impedance output control
- Per-channel message mode
- Per-channel Pseudo Random Bit Sequence (PRBS) pattern generation and bit error detection
- Control interface compatible to Motorola non-multiplexed CPUs
- Connection memory block programming capability
- IEEE-1149.1 (JTAG) test port
- 3.3 V I/O with 5 V tolerant input

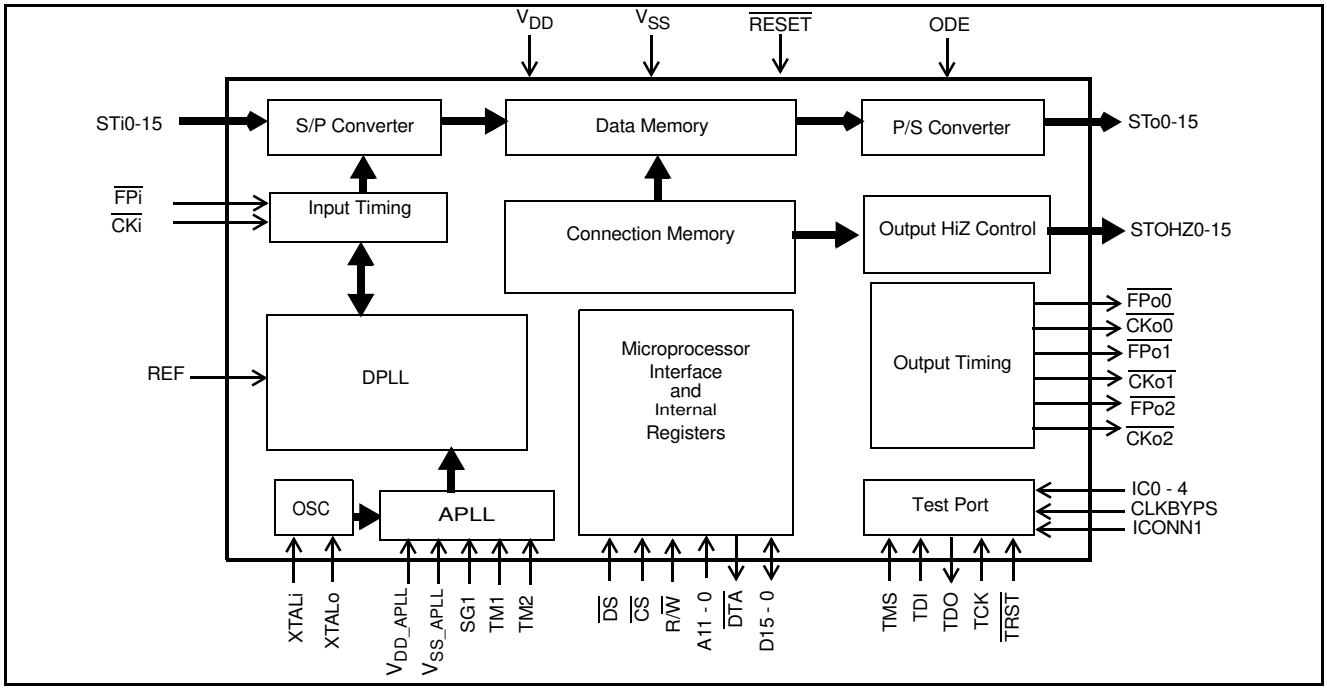

Figure 1 - ZL50011 Functional Block Diagram

Zarlink Semiconductor US Patent No. 5,602,884, UK Patent No. 0772912, France Brevete S.G.D.G. 0772912; Germany DBP No. 69502724.7-08

Applications

- Small and medium digital switching platforms
- Access Servers
- Time Division Multiplexers
- Computer Telephony Integration
- Digital Loop Carriers

Description

The device has 16 ST-BUS inputs (STi0-15) and 16 ST-BUS outputs (STo0-15). It is a non-blocking digital switch with 512 64 kbps channels and performs rate conversion between the ST-BUS inputs and ST-BUS outputs. The ST-BUS inputs accept serial input data streams with the data rate of 2.048 Mbps, 4.096 Mbps or 8.192 Mbps on a per-stream basis. The ST-BUS outputs deliver serial output data streams with the data rate of 2.048 Mbps, 4.096 Mbps or 8.192 Mbps on a per-stream basis. The device also provides 16 high impedance control outputs (STOHZ 0-15) to support the use of external high impedance control buffers.

The ZL50011 has features that are programmable on a per-stream or per-channel basis including message mode, input bit delay, output bit advancement, constant throughput delay and high impedance output control.

The on-chip DPLL meets Telcordia GR-1244-CORE stratum 4 specifications (Stratum 4). It accepts a dedicated timing reference input at either 8 kHz, 1.544 MHz or 2.048 MHz. Alternatively, the reference can be replaced by an internal 8 kHz signal derived from the ST-BUS input frame boundary. The DPLL provides reference monitor, jitter attenuation and free run functions. It can be used as a system's ST-BUS timing source which is synchronized to the network. The DPLL can also be bypassed so that the device operates under system timing.

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Changes Summary

The following table captures the changes from the March 2006 issue.

Page	Item	Change
1	Ordering Information	Removed leaded packages as per PCN notice.

The following table captures the changes from the July 2004 issue.

Page	Item	Change
12, 34, 40	(1) Pin Description - Signal XTALi (2) 2.9.3 “DPLL Bypass Mode“ (3) 3.0 “Oscillator Requirements“	• Clarified initialization input clock requirement in DPLL Bypass mode.
18	2.1.4 “Improved Input Jitter Tolerance with Frame Boundary Determinator“	• Added a new section to describe the improved input jitter tolerance with the frame boundary determinator.
47	Table 16 - “Control Register (CR) Bits“ - bits “FBDMODE“ and “FBDEN“	• Renamed bit 15 from Unused to FBDMODE and added description to clarify the frame boundary determinator operation. • Clarified FBDEN description.

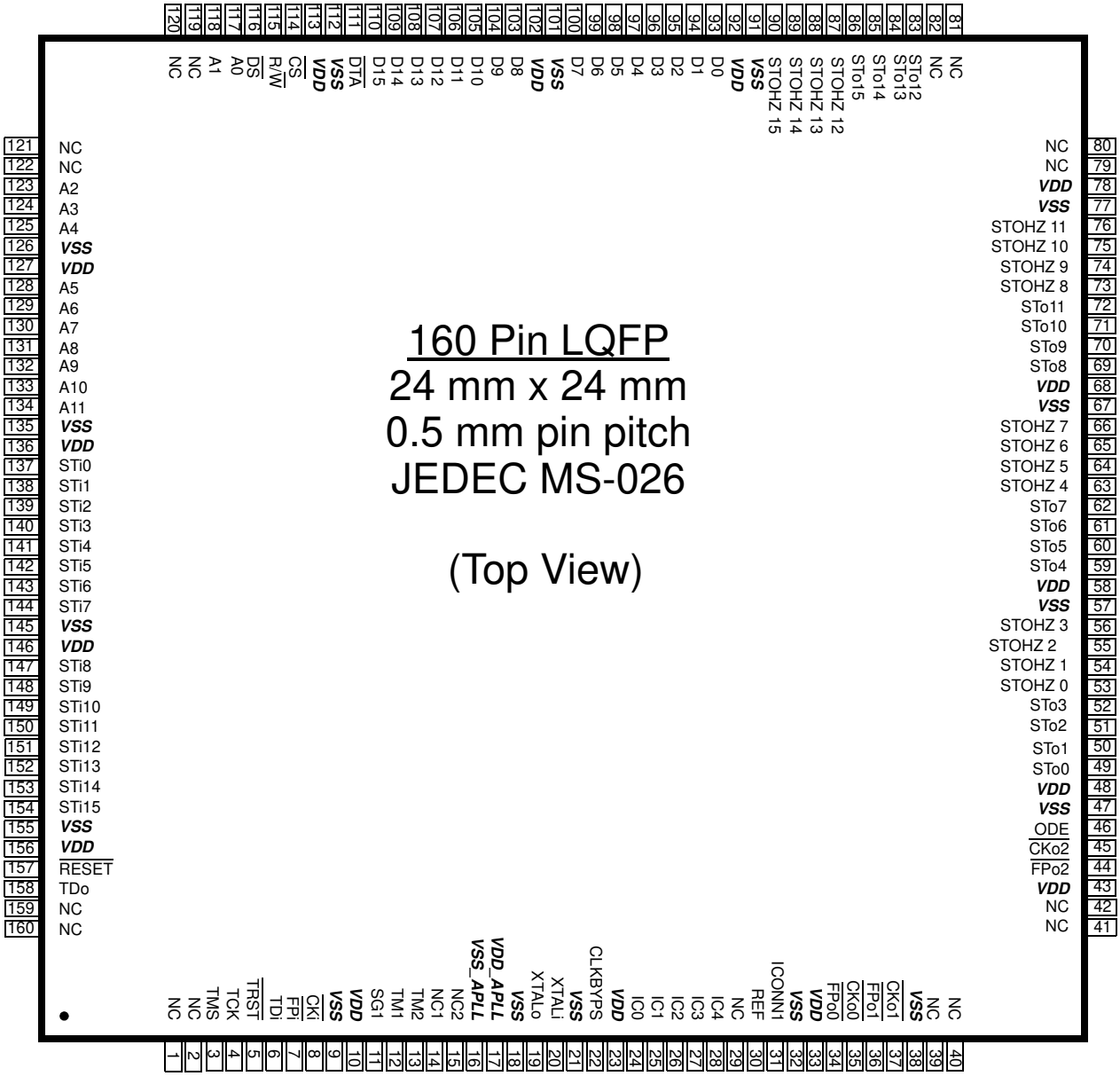

Figure 2 - 24 mm x 24 mm LQFP (JEDEC MS-026) Pinout Diagram

PINOUT DIAGRAM: (as viewed through top of package)

A1 corner identified by metallized marking, mould indent, ink dot or right-angled corner

	1	2	3	4	5	6	7	8	9	10	11	12
A	ODE	$\overline{FPo2}$	$\overline{FPo0}$	ICONN 1	IC1	IC0	XTALi	XTALo	TM1	$\overline{CKi}$	TDi	TCK
B	$\overline{CKo2}$	$\overline{CKo1}$	$\overline{FPo1}$	$\overline{CKo0}$	IC3	IC2	CLK BYPS	VDD_ APLL	SG1	$\overline{FPi}$	$\overline{TRST}$	TMS
C	STo2	STo1	STOHZ 0	REF	NC	NC	IC4	NC2	NC1	TM2	TDo	STi15
D	STo3	STo0	STOHZ 1	VSS	VDD	VDD	VDD	VSS_ APLL	VSS	STi8	$\overline{RESET}$	STi14
E	STo5	STo4	STOHZ 3	STOHZ 2	VSS	VSS	VSS	VSS	VDD	STi9	STi13	STi12
F	STo6	STo7	STOHZ 4	VDD	VSS	VSS	VSS	VSS	VDD	STi7	STi10	STi11
G	STOHZ 6	STOHZ 7	STOHZ 5	VDD	VSS	VSS	VSS	VSS	STi1	STi6	STi5	STi4
H	STo9	STo10	STo8	VDD	VSS	VSS	VSS	VSS	STi0	$\overline{DS}$	STi2	STi3
J	STo11	STOHZ 11	STOHZ 8	VSS	D2	VDD	VDD	VDD	A10	A9	A8	A11
K	STOHZ 9	STOHZ 15	STo15	STOHZ 13	D1	D5	$\overline{CS}$	D10	D11	A5	A4	A7
L	STOHZ 10	STo12	STo13	D3	D15	D4	D7	D12	D14	A2	A3	A6
M	STo14	STOHZ 12	STOHZ 14	D0	$\overline{DTA}$	D6	D8	D9	D13	A0	A1	R/$\overline{W}$

Figure 3 - 13 mm x 13 mm 144 Ball LBGA Pinout Diagram

Pin Description

LQFP Pin Number	LBGA Ball Number	Name	Description
10, 23, 33, 43, 48, 58, 68, 78, 92, 102, 113, 127, 136, 146, 156	D5, D6, D7 E9 F4, F9 G4 H4 J6, J7, J8	V_{DD}	**Power Supply for the device**: +3.3 V
9, 18, 21, 32, 38, 47, 57, 67, 77, 91, 101, 112, 126, 135, 145, 155	D4, D9 E5, E6, E7, E8 F5, F6, F7, F8 G5, G6, G7, G8 H5, H6, H7, H8 J4	V_{ss} (GND)	**Ground**.
3	B12	TMS	**Test Mode Select (3.3 V Tolerant Input with internal pull-up)**: JTAG signal that controls the state transitions of the TAP controller. This pin is pulled high by an internal pull-up resistor when it is not driven.
4	A12	TCK	**Test Clock (5 V Tolerant Input)**: Provides the clock to the JTAG test logic.
5	B11	$\overline{\text{TRST}}$	**Test Reset (3.3 V Tolerant Input with internal pull-up)**: Asynchronously initializes the JTAG TAP controller by putting it in the Test-Logic-Reset state. This pin should be pulsed low during power-up to ensure that the device is in the normal functional mode. When JTAG is not being used, this pin should be pulled low during normal operation.
6	A11	TDi	**Test Serial Data In (3.3 V Tolerant Input with internal pull-up)**: JTAG serial test instructions and data are shifted in on this pin. This pin is pulled high by an internal pull-up resistor when it is not driven.
7	B10	$\overline{\text{FPi}}$	**ST-BUS Frame Pulse Input (5 V Tolerant Input):** This pin accepts the frame pulse which stays low for 61 ns, 122 ns or 244 ns at the frame boundary. The frame pulse associating with the highest input data rate has to be applied to this pin. The frame pulse frequency is 8 kHz. The device also accepts positive frame pulse if the FPINP bit is high in the Internal Mode Selection register.
8	A10	$\overline{\text{CKi}}$	**ST-BUS Clock Input (5 V Tolerant Input):** This pin accepts a 4.096 MHz, 8.192 MHz or 16.384 MHz clock. The input clock frequency has to be equal to or greater than twice of the highest input data rate. The clock falling edge defines the input frame boundary. The device also allows the clock rising edge to define the frame boundary by programming the CKINP bit in the Internal Mode Selection register.

Pin Description (continued)

LQFP Pin Number	LBGA Ball Number	Name	Description
11	B9	SG1	**APLL Test Control (3.3 V Input with internal pull-down)**: For normal operation, this input MUST be low.
12	A9	TM1	**APLL Test Pin 1**: For normal operation, this input MUST be low.
13	C10	TM2	**APLL Test Pin 2**: For normal operation, this input MUST be low.
14, 15	C9, C8	NC1, NC2	**No Connection**: These pins MUST be left unconnected.
16	D8	V_{ss_APLL}	**Ground for the APLL Circuit**.
17	B8	V_{DD_APLL}	**Power Supply for the on-chip Analog Phase Lock Loop (APLL) Circuit**: +3.3 V
19	A8	XTALo	**Oscillator Clock Output (3.3 V Output).** This pin is connected to a 20 MHz crystal (see Figure 30 on page 40), or it is left unconnected if a clock oscillator is connected to the XTALi pin (see Figure 31 on page 41). If the device is to be used in DPLL Bypass mode only, the crystal or clock oscillator can be omitted, in which case this pin must be left unconnected.
20	A7	XTALi	**Oscillator Clock Input (3.3 V Input).** This pin is connected to a 20 MHz crystal (see Figure 30 on page 40), or it is connected to a clock oscillator (see Figure 31 on page 41). If the device is to be used in DPLL Bypass mode only, the crystal or clock oscillator can be omitted, but this pin should still get a valid clock signal so that the device can be initialized. The easiest way is to tie the CKi clock to this pin.
22	B7	CLKBYPS	**Test Clock Input:** For device testing only, in normal operation, this input MUST be low.
24 - 28	A6, A5, B6, B5, C7	IC0 - 4	**Internal connection (3.3 V Tolerant Inputs with internal pull-down)**: In normal mode, these pins must be low.
30	C4	REF	**Reference Input (5 V Tolerant Input):** This pin accepts an 8 kHz, 1.544 MHz or 2.048 MHz timing reference. It is used as one of the references for the DPLL in the Master mode. This pin is ignored in the DPLL Bypass Mode. When this pin is not in use, it is required to be driven high or low by connecting it to Vdd or ground through an external pull-up resistor or external pull-down resistor.
31	A4	ICONN1	**Internal Connection:** In normal mode, this pin must be low.
34	A3	$\overline{\text{FPo0}}$	**ST-BUS Frame Pulse Output 0 (5 V Tolerance Three-state Output):** ST-BUS frame pulse output which stays low for 244 ns or 122 ns at the output frame boundary. Its frequency is 8 KHz. The polarity of this signal can be changed using the Internal Mode Selection register.

Pin Description (continued)

LQFP Pin Number	LBGA Ball Number	Name	Description
35	B4	$\overline{\text{CKo0}}$	**ST-BUS Clock Output 0 (5 V Tolerant Three-state Output):** A 4.094 MHz or 8.192 MHz clock output. The clock falling edge defines the output frame boundary. The polarity of this signal can be changed using the Internal Mode Selection register.
36	B3	$\overline{\text{FPo1}}$	**ST-BUS Frame Pulse Output 1 (5 V Tolerant Three-state Output):** ST-BUS frame pulse output which stays low for 61 ns or 122 ns at the output frame boundary. Its frequency is 8 KHz. The polarity of this signal can be changed using the Internal Mode Selection register.
37	B2	$\overline{\text{CKo1}}$	**ST-BUS Clock Output 1 (5 V Tolerant Three-state Output):** A 16.384 MHz or 8.192 MHz clock output. The clock falling edge defines the output frame boundary. The polarity of this signal can be changed using the Internal Mode Selection register.
44	A2	$\overline{\text{FPo2}}$	**ST-BUS Frame Pulse Output 2 (5 V Tolerant High Speed Three-state Output):** ST-BUS frame pulse output which stays low for 30 ns or 61 ns at the frame boundary. Its frequency is 8 KHz. The polarity of this signal can be changed using the Internal Mode Selection register.
45	B1	$\overline{\text{CKo2}}$	**ST-BUS Clock Output 2 (5 V Tolerant High Speed Three-state Output):** A 32.768 MHz or 16.384 MHz clock output. The clock falling edge defines the output frame boundary. The polarity of this signal can be changed using the Internal Mode Selection register.
46	A1	ODE	**Output Drive Enable (5 V Tolerant Input):** This is the asynchronously output enable control for the STo0 - 15 and the output driven high control for the STOHZ 0 - 15 serial outputs. When it is high, the STo0 - 15 and STOHZ 0 - 15 are enabled. When it is low, the STo0 - 15 are in the high impedance state and the STOHZ 0 - 15 are driven high.
49 - 52 59 - 62 69 - 72 83 - 86	D2, C2, C1, D1 E2, E1, F1, F2 H3, H1, H2, J1 L2, L3, M1, K3	STo0 - 3 STo4 - 7 STo8 - 11 STo12 - 15	**Serial Output Streams 0 to 15 (5 V Tolerant Three-state Outputs):** The data rate of these output streams can be selected independently using the stream control output registers. In the 2.048 Mbps mode, these pins have serial TDM data streams at 2.048 Mbps with 32 channels per stream. In the 4.096 Mbps mode, these pins have serial TDM data streams at 4.096 Mbps with 64 channels per stream. In the 8.192 Mbps mode, these pins have serial TDM data streams at 8.192 Mbps with 128 channels per stream.

Pin Description (continued)

LQFP Pin Number	LBGA Ball Number	Name	Description
53 - 56 63 - 66 73 - 76 87 - 90	C3, D3, E4, E3 F3, G3, G1, G2 J3, K1, L1, J2 M2, K4, M3, K2	STOHZ 0 - 3 STOHZ 4 - 7 STOHZ 8 - 11 STOHZ 12 -15	**Serial Output Streams High Impedance Control 0 to 15 (5 V Tolerant Three-state Outputs):** These pins are used to enable (or disable) external three-state buffers. When an output channel is in the high impedance state, the STOHZ drives high for the duration of the corresponding output channel. When the STo channel is active, the STOHZ drives low for the duration of the corresponding output channel.
93 - 96 97 - 100 103 - 106 107 - 110	M4, K5, J5, L4 L6, K6, M6, L7 M7, M8, K8, K9 L8, M9, L9, L5	D0 - D3 D4 - D7 D8 - D11 D12 - D15	**Data Bus 0 - 15 (5 V Tolerant I/Os):** These pins form the 16-bit data bus of the microprocessor port.
111	M5	$\overline{DTA}$	**Data Transfer Acknowledgment (5 V Tolerant Three-state Output):** This active low output indicates that a data bus transfer is complete. A pull-up resistor is required to hold this pin at HIGH level.
114	K7	$\overline{CS}$	**Chip Select (5 V Tolerant Input):** Active low input used by the microprocessor to enable the microprocessor port access.
115	M12	R/$\overline{W}$	**Read/Write (5 V Tolerant Input):** This input controls the direction of the data bus lines (D0-D15) during a microprocessor access.
116	H10	$\overline{DS}$	**Data Strobe (5 V Tolerant Input):** This active low input works in conjunction with $\overline{CS}$ to enable the microprocessor port read and write operations.
117, 118 123 - 125 128 - 130 131 - 134	M10, M11 L10, L11, K11 K10, L12, K12 J11, J10, J9, J12	A0 - A1 A2 - A4 A5 - A7 A8 - A11	**Address 0 - 11 (5 V Tolerant Inputs):** These pins form the 12-bit address bus to the internal memories and registers.
137 - 139 140 - 142 143, 144 147 - 149 150 - 152 153, 154	H9, G9, H11 H12, G12, G11 G10, F10 D10, E10, F11 F12, E12, E11 D12, C12	STi0 - 2 STi3 - 5 STi6 - 7 STi8 - 10 STi11- 13 STi14 - 15	**Serial Input Streams 0 to 15 (5 V Tolerant Inputs):** The data rate of these input streams can be selected independently using the stream input control registers. In the 2.048 Mbps mode, these pins accept serial TDM data streams at 2.048 Mbps with 32 channels per stream. In the 4.096 Mbps mode, these pins accept serial TDM data streams at 4.096 Mbps with 64 channels per stream. In the 8.192 Mbps mode, these pins accept serial TDM data streams at 8.192 Mbps with 128 channels per stream. Unused serial input pins are required to connect to either Vdd or ground, through an external pull-up resistor or external pull-down resistor.

Pin Description (continued)

LQFP Pin Number	LBGA Ball Number	Name	Description
157	D11	$\overline{\text{RESET}}$	**Device Reset (5 V Tolerant Input):** This input (active LOW) puts the device in its reset state that disables the STo0 - 15 drivers and drives the STOHZ 0 - 15 outputs to high. It also clears the device registers and internal counters. To ensure proper reset action, the reset pin must be low for longer than 1 ms. Upon releasing the reset signal to the device, the first microprocessor access can take place after 600 µs due to the time required to stabilize the APLL and crystal oscillator blocks from the power down state.
158	C11	TDo	**Test Serial Data Out (3 V Tolerant Three-state Output)**: JTAG serial data is output on this pin on the falling edge of TCK. This pin is held in high impedance state when JTAG is not enabled.
1, 2, 29, 39 - 42, 79 - 82, 119 - 122, 159, 160	C5, C6	NC	**No Connection Pins**. These pins are not connected to the device internally.

1.0 Device Overview

The device uses the ST-BUS input frame pulse and the ST-BUS input clock to define the input frame boundary and timing for the ST-BUS input streams with various data rates (2.048 Mbps, 4.096 Mbps and/or 8.192 Mbps). The output frame boundary is defined by the output frame pulses and the output clock timing for the ST-BUS output streams with various data rates (2.048 Mbps, 4.096 Mbps and/or 8.192 Mbps).

By using Zarlink's message mode capability, microprocessor data can be broadcast to the data output streams on a per channel basis. This feature is useful for transferring control and status information for external circuits or other ST-BUS devices.

The on-chip DPLL can be operated in one of three modes: Master, Freerun or Bypass. In Master mode, the DPLL can be used as a system's timing source to provide ST-BUS clocks and frame pulses which are synchronized to the network. In Freerun mode, the DPLL can be used to provide system ST-BUS timing which is independent of the network. In Bypass mode, the DPLL is completely bypassed and the device operates entirely from system timing provided by the input ST-BUS clock and frame pulse. An external 20.000 MHz crystal or clock oscillator is required in Master and Freerun modes. The DPLL intrinsic jitter is 6.25 ns peak to peak.

In Master mode, the DPLL is synchronized to either the REF input or to an internal 8 kHz signal derived from the input ST-BUS clock and frame pulse. The REF input accepts an 8 kHz, 1.544 MHz or 2.048 MHz network timing reference signal. The DPLL also provides reference monitor and jitter attenuation functions. The DPLL output is an internal high-speed clock from which output ST-BUS clock and frame pulses are generated.

A non-multiplexed microprocessor port allows users to program the device with various operating modes and switching configurations. Users can use the microprocessor port to perform register read/write, connection memory read/write and data memory read operations. The microprocessor port has a 12-bit address bus, a 16-bit data bus and four control signals.

The device also supports the mandatory requirements of the IEEE-1149.1 (JTAG) standard via the test port.

2.0 Functional Description

A functional block diagram of the ZL50011 is shown in Figure 1 on page 1.

2.1 ST-BUS Input Data Rate and Input Timing

The device has 16 ST-BUS serial data inputs. Any of the 16 inputs can be programmed to accept different data rates, namely, 2.048 Mbps, 4.096 Mbps or 8.192 Mbps.

2.1.1 ST-BUS Input Operation Mode

Any ST-BUS input can be programmed to accept the 2.048 Mbps, 4.096 Mbps or 8.192 Mbps data using Bit 0 to 2 in the stream input control registers, SICR0 to SICR15 as shown in Table 24 on page 54 and Table 25 on page 56.

The maximum number of input channels is 512 channels. External pull-up or pull-down resistors are required for any unused ST-BUS inputs.

2.1.2 Frame Pulse Input and Clock Input timing

The frame pulse input $\overline{\text{FPi}}$ accepts the frame pulse used for the **highest** input data rate. The frame pulse is an 8 kHz input signal which stays low for 244 ns, 122 ns or 61 ns for the input data rate of 2.048 Mbps, 4.096 Mbps or 8.192 Mbps respectively. The frequency of $\overline{\text{CKi}}$ must be twice the highest data rate. For example, if users present the ZL50011 with 2.048 Mbps and 8.192 Mbps input data, the device should be programmed to accept the input clock of 16.384 MHz and the frame pulse which stays low for 61 ns.

Users have to program the CKIN2 - 0 bits in the Control Register (CR), for the width of the frame pulse low cycle and the frequency of the input clock. See Table 1 for the programming of the CKIN0, CKIN1 and CKIN2 bits in the Control Register.

CKIN2 - 0 bits	$\overline{FPi}$ Low Cycle	$\overline{CKi}$	Highest Input Data Rate
000	61 ns	16.384 MHz	8.192 Mbps
001	122 ns	8.192 MHz	4.096 Mbps
010	244 ns	4.096 MHz	2.048 Mbps
011 - 111	Reserved		

Table 1 - $\overline{FPi}$ and $\overline{CKi}$ Input Programming

The device also accepts positive or negative input frame pulse and ST-BUS input clock formats via the programming of the FPINP and CKINP bits in the Internal Mode Selection (IMS) register. By default, the device accepts the negative input clock format.

Figure 4, Figure 5 and Figure 6 describe the usage of CKIN2 - 0, FPINP and CKINP in the Internal Mode Selection (IMS) register:

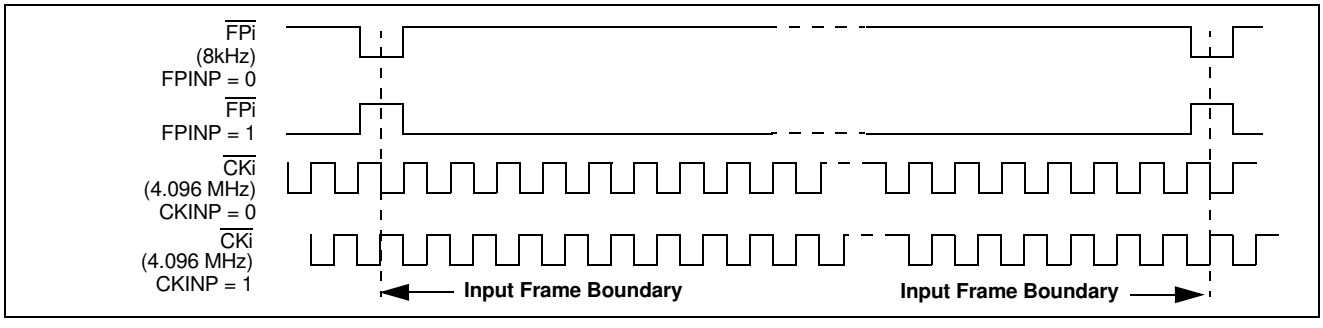

Figure 4 - Input Timing when (CKIN2 to CKIN0 bits = 010) in the Control Register

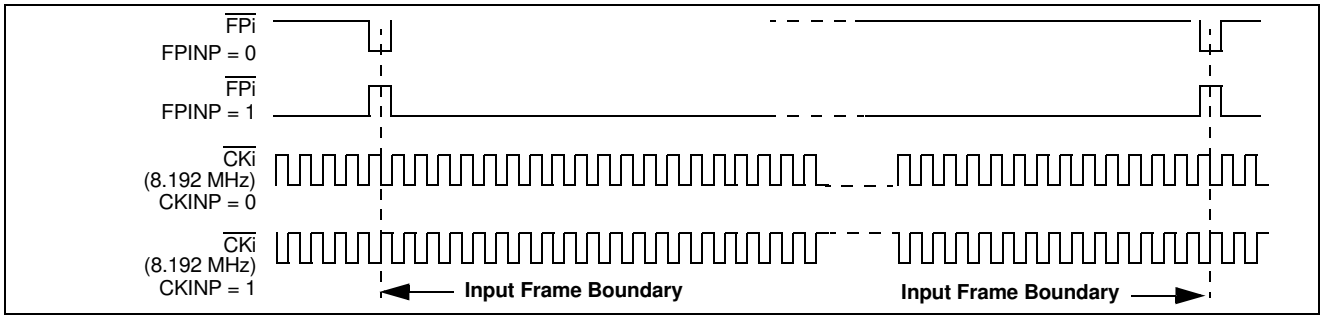

Figure 5 - Input Timing when (CKIN2 to CKIN0 bits = 001) in the Control Register

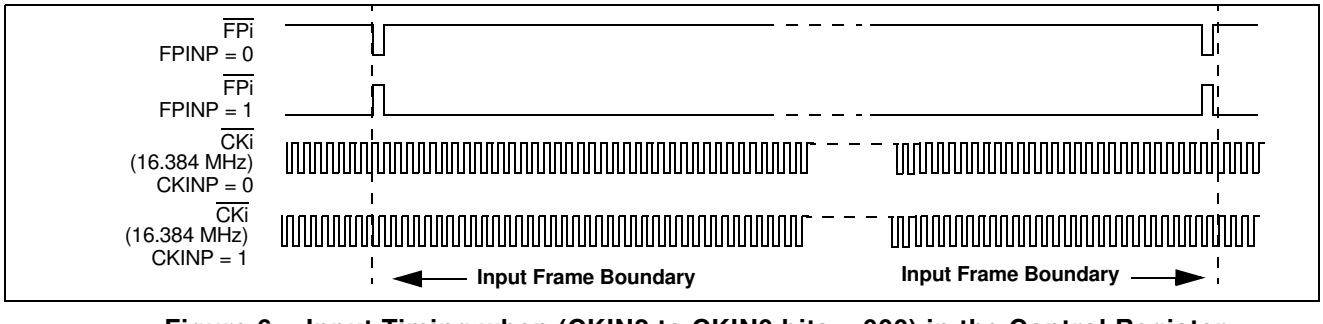

Figure 6 - Input Timing when (CKIN2 to CKIN0 bits = 000) in the Control Register

2.1.3 ST-BUS Input Timing

When the negative input frame pulse and negative input clock formats are used, the input frame boundary is defined by the falling edge of the $\overline{CKi}$ input clock while the $\overline{FPi}$ is low. When the input data rate is 2.048 Mbps, 4.096 Mbps or 8.192 Mbps, there are 32, 64 or 128 channels per every ST-BUS frame respectively. Figure 7 shows the details:

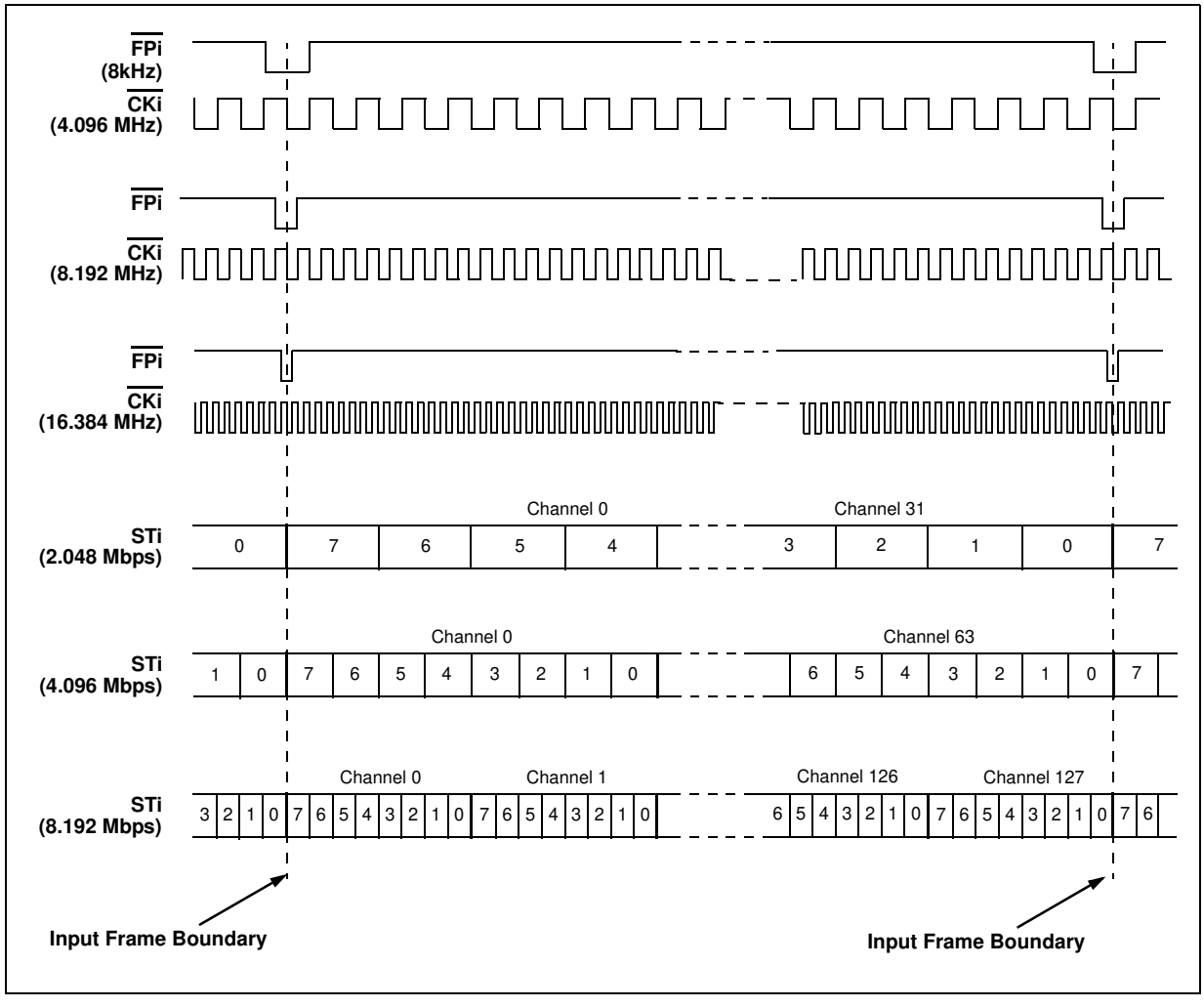

Figure 7 - ST-BUS Input Timing for Various Input Data Rates

2.1.4 Improved Input Jitter Tolerance with Frame Boundary Determinator

The ZL50011 has a Frame Boundary Determinator (FBD) allowing substantial increase of the CKi input clock jitter tolerance. The FBD circuit is enabled by setting the Control Register bits FBDEN and FBDMODE to HIGH. By default the FBD is disabled. Both the FBDEN and FBDMODE bits should be set HIGH during normal operation. The device can have 20 ns of input clock jitter tolerance (on CKi and FPi) when the FBD is fully enabled.

This jitter tolerance is related to the proper operation of the switch, and describes the amount of jitter that can be accepted on the CKi and FPi inputs. Do not confuse this with the DPLL jitter tolerance (Section 2.11.2) which describes the ability of the integrated DPLL to lock to an input reference (REF).

2.2 ST-BUS Output Data Rate and Output Timing

The device has 16 ST-BUS serial data outputs. Any of the 16 outputs can be programmed to deliver different data rates at 2.048 Mbps, 4.096 Mbps or 8.192 Mbps.

2.2.1 ST-BUS Output Operation Mode

Any ST-BUS output can be programmed to deliver the data at 2.048 Mbps, 4.096 Mbps or 8.192 Mbps mode using Bit 0 to 2 in the Stream Output Control Register, SOCR0 to SOCR15 as shown in Table 28 on page 60 and Table 29 on page 61.

2.2.2 Frame Pulse Output and Clock Output Timing

The device offers 3 frame pulse outputs, $\overline{FPo0}$, $\overline{FPo1}$ and $\overline{FPo2}$. All output frame pulses are 8 kHz output signals. By default, the output frame boundary is defined by the falling edge of the $\overline{CKo0}$, $\overline{CKo1}$ or $\overline{CKo2}$ output clocks while the $\overline{FPo0}$, $\overline{FPo1}$ or $\overline{FPo2}$ output frame pulse goes low respectively.

In addition to the default settings, users can also select different output frame pulse low cycles and output clock frequencies by programming the CKFP0, CKFP1 and CKFP2 bits in the Control Register. See Table 2, Table 3 and Table 4 for the bit usage in the Control Register:

CKFP0	$\overline{FPo0}$ Low Cycle	$\overline{CKo0}$
0	244 ns	4.096 MHz
1	122 ns	8.192 MHz

Table 2 - $\overline{FPo0}$ and $\overline{CKo0}$ Output Programming

CKFP1	$\overline{FPo1}$	$\overline{CKo1}$
0	61 ns	16.384 MHz
1	122 ns	8.192 MHz

Table 3 - $\overline{FPo1}$ and $\overline{CKo1}$ Output Programming

CKFP2	$\overline{FPo2}$	$\overline{CKo2}$
0	30 ns	32.768 MHz
1	61 ns	16.384 MHz

Table 4 - $\overline{FPo2}$ and $\overline{CKo2}$ Output Programming

The device also delivers positive or negative output frame pulse and ST-BUS output clock formats via the programming of the FP0P, FP1P, FP2P, CK0P, CK1P and CK2P bits in the Internal Mode Selection (IMS) register. By default, the device delivers the negative output frame pulse and negative output clock formats.

Figure 8 to Figure 13 describe the usage of the CKFP0, CKFP1, CKFP2, FP0P, FP1P, FP2P, CK0P, CK1P and CK2P in the Control Register and Internal Mode Selection Register:

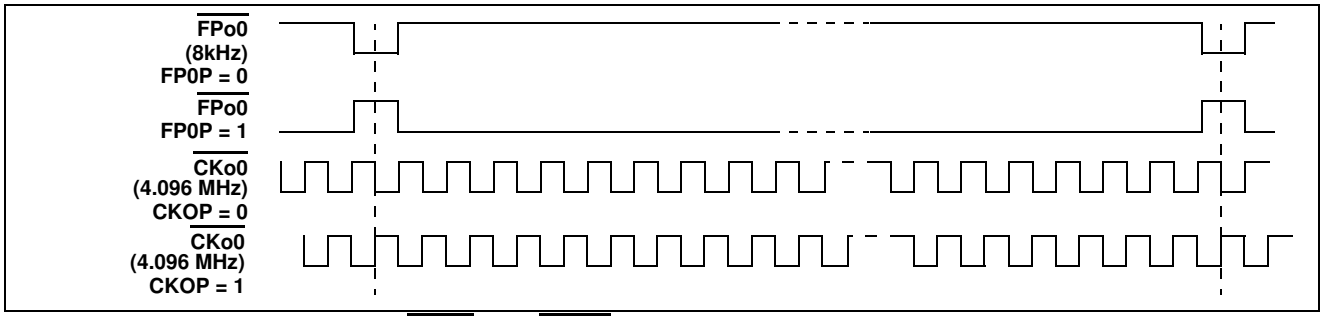

Figure 8 - FPo0 and CKo0 Output Timing when the CKFP0 Bit = 0

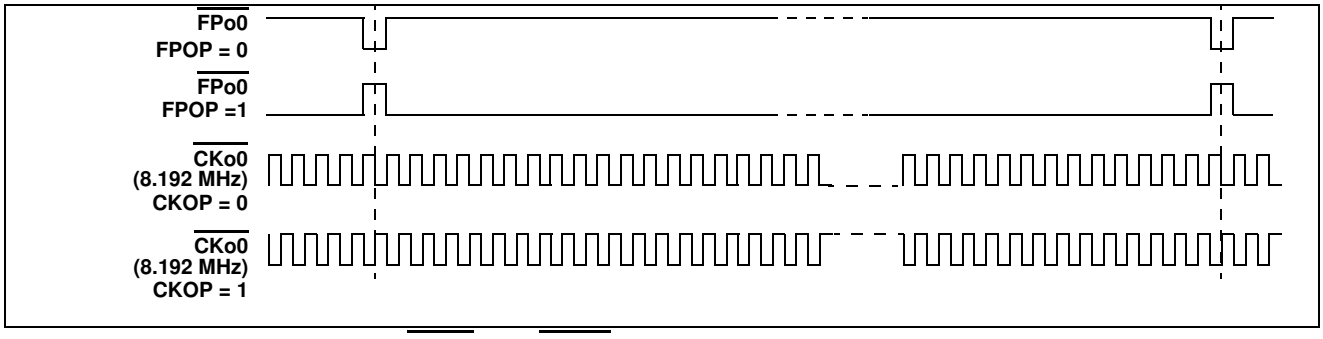

Figure 9 - FPo0 and CKo0 Output Timing when the CKFP0 Bit = 1

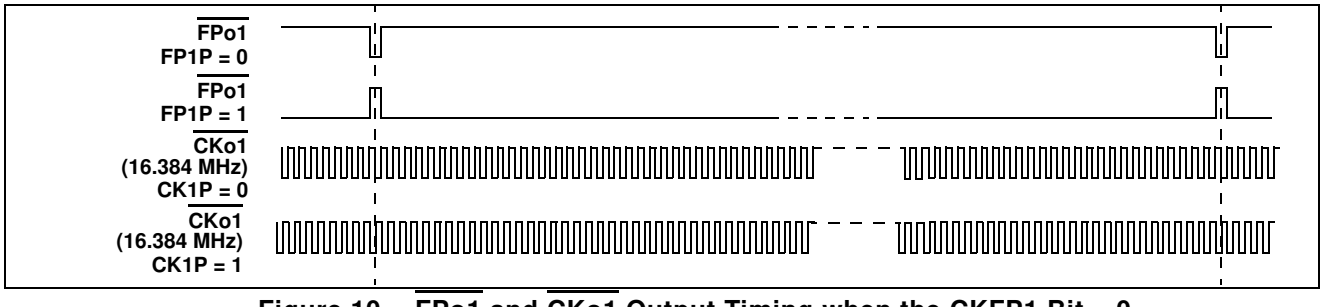

Figure 10 - FPo1 and CKo1 Output Timing when the CKFP1 Bit = 0

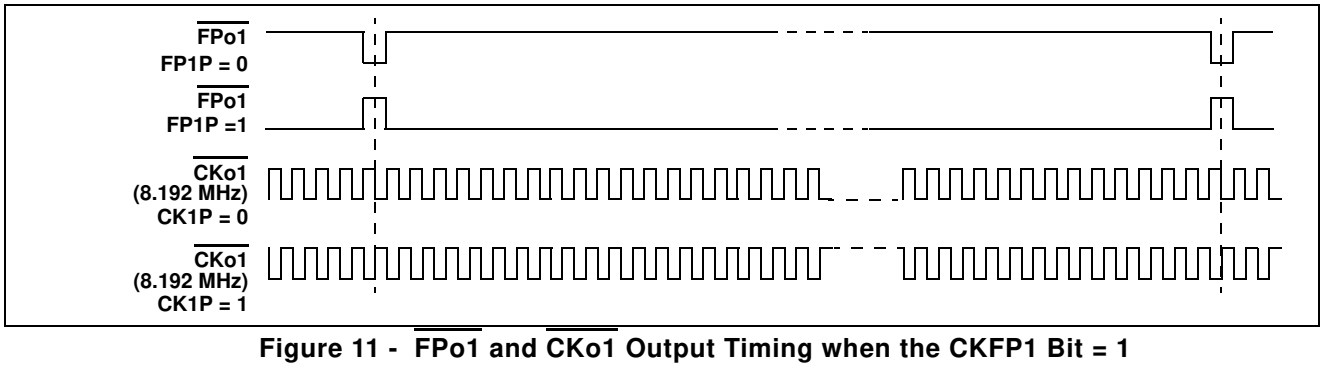

Figure 11 - FPo1 and CKo1 Output Timing when the CKFP1 Bit = 1

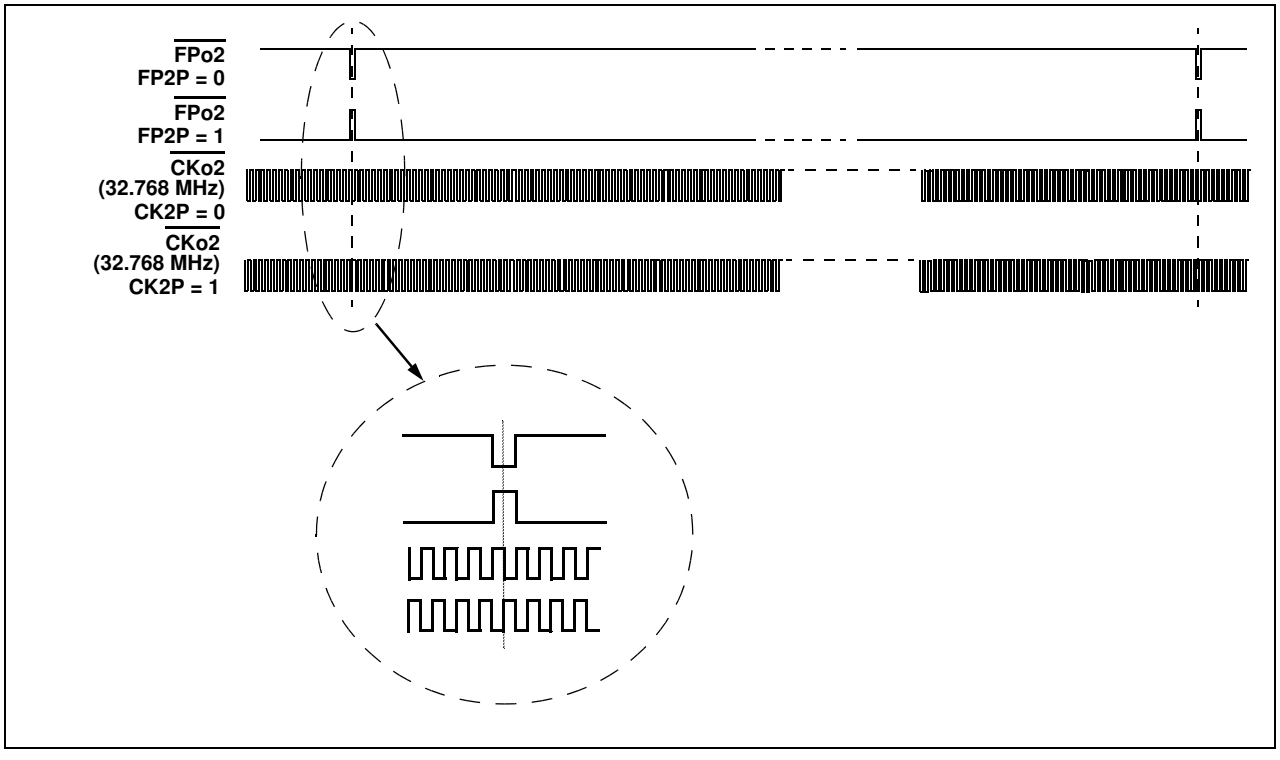

Figure 12 - $\overline{\text{FPo2}}$ and $\overline{\text{CKo2}}$ Output Timing when the CKFP2 Bit = 0

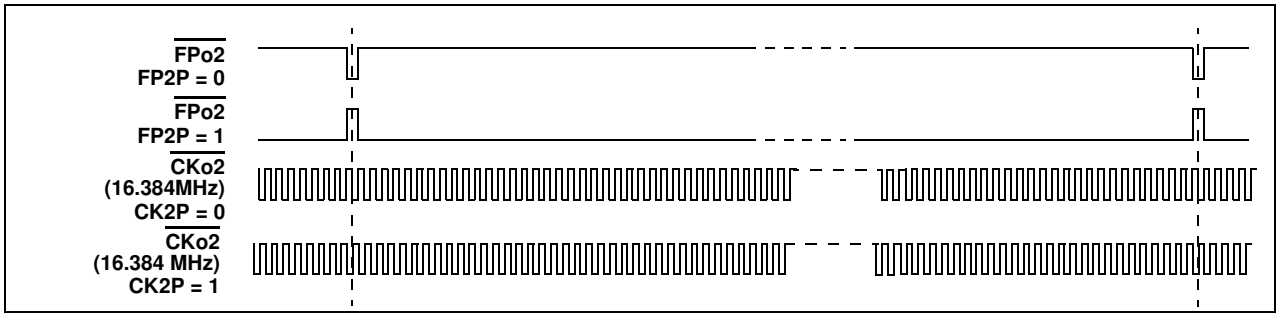

Figure 13 - $\overline{\text{FPo2}}$ and $\overline{\text{CKo2}}$ Output Timing when the CKFP2 Bit = 1

2.2.3 ST-BUS Output Timing

By default, the output frame boundary is defined by the falling edge of the $\overline{CKo0}$, $\overline{CKo1}$ or $\overline{CKo2}$ output clock while the $\overline{FPo0}$, $\overline{FPo1}$ or $\overline{FPo2}$ output frame pulse goes low respectively. When the output data rates are 2.048 Mbps, 4.096 Mbps and 8.192 Mbps, there are 32, 64 or 128 output channels per every ST-BUS frame respectively. Figure 14 describes the details.

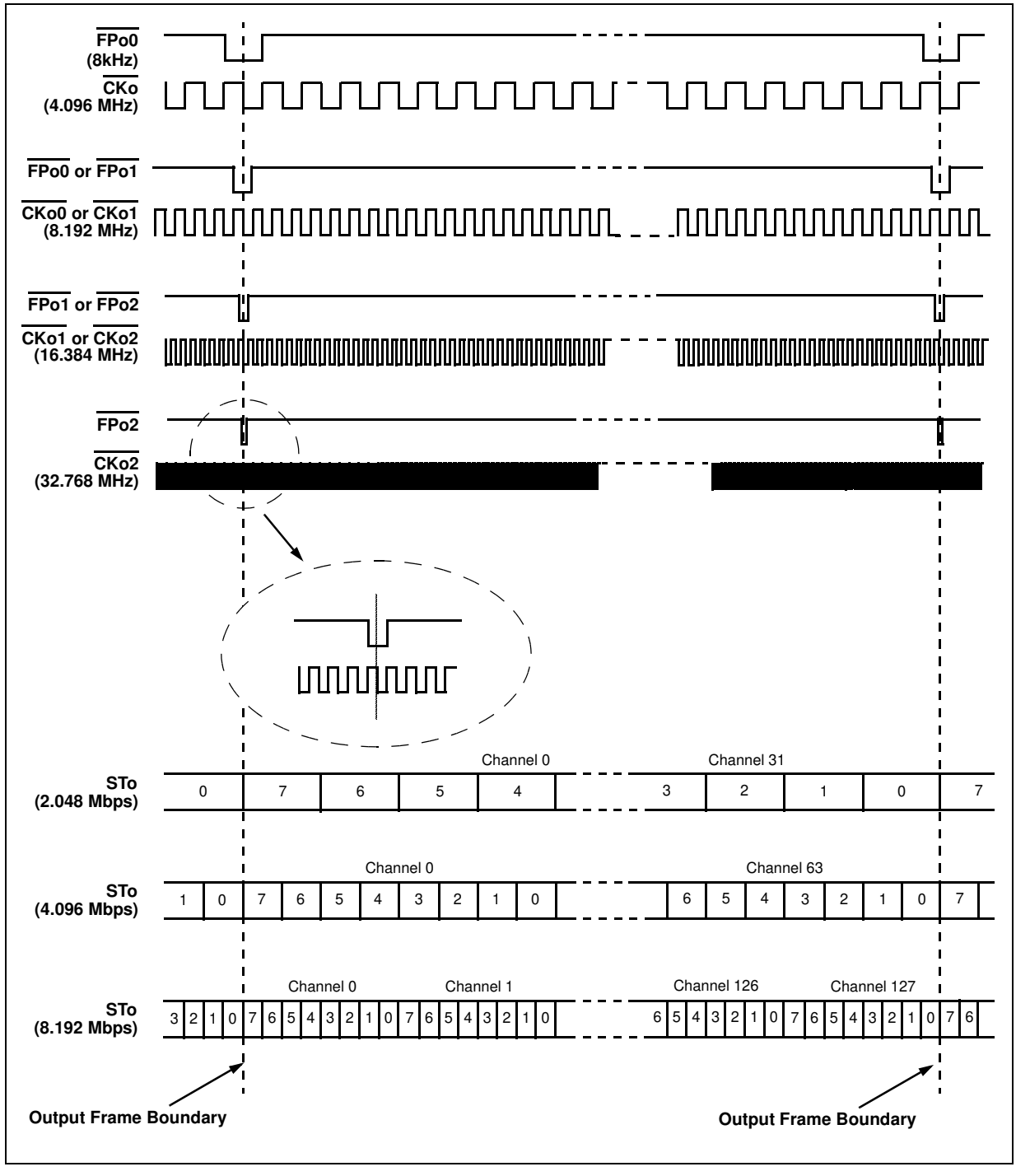

Figure 14 - ST-BUS Output Timing for Various Output Data Rates

2.3 Serial Data Input Delay and Serial Data Output Offset

Various registers are provided to adjust the input and output delays for every input and every output data stream. The input and output channel delay can vary from 0 to 31, 0 to 63 and 0 to 127 channel(s) for the 2.048 Mbps, 4.096 Mbps and 8.192 Mbps modes respectively.

The input and output bit delay can vary from 0 to 7 bits. The fractional input bit delay can vary from 1/4, 1/2, 3/4 to 4/4 bit. The fractional output bit advancement can vary from 0, 1/4, 1/2 to 3/4 bit.

2.3.1 Input Channel Delay Programming

This feature allows each input stream to have a different input frame boundary with respect to the input frame boundary defined by the $\overline{FPi}$ and $\overline{CKi}$. By default, all input streams have channel delay of zero such that Ch0 is the first channel that appears after the input frame boundary (see Figure 15).

The input channel delay programming is enabled by setting Bit 3 to 9 in the Stream Input Delay Register (SIDR). The input channel delay can vary from 0 to 31, 0 to 63 and 0 to 127 for the 2.048 Mbps, 4.096 Mbps and 8.192 Mbps modes respectively.

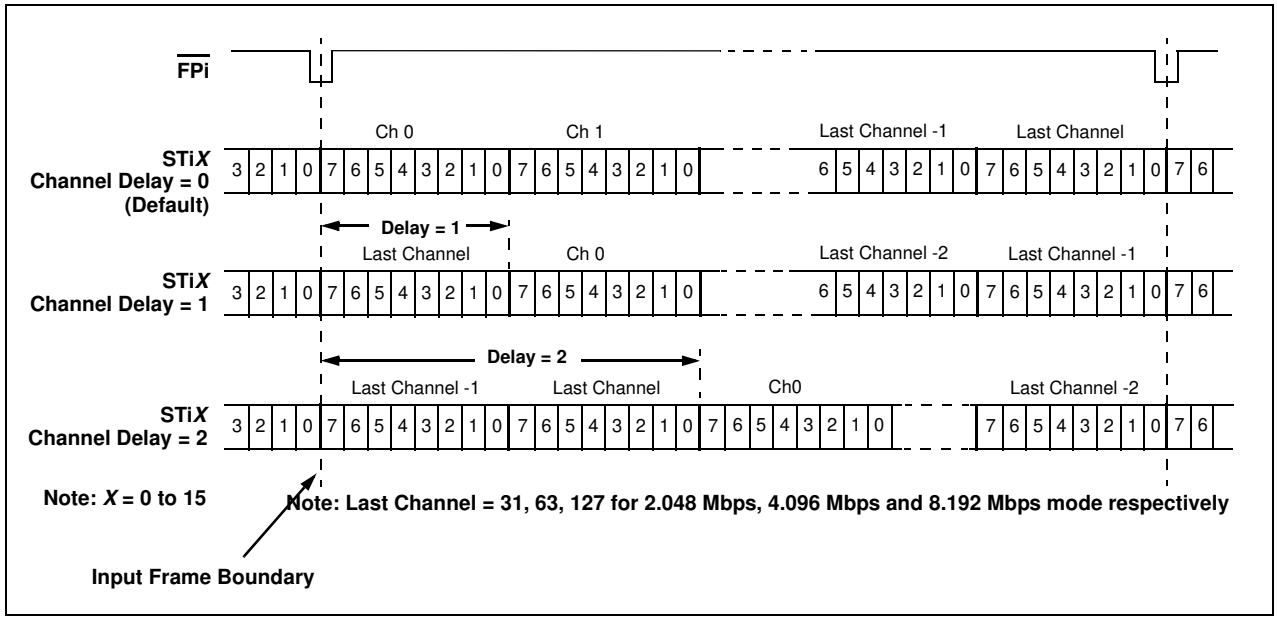

Figure 15 - Input Channel Delay Timing Diagram

2.3.2 Input Bit Delay Programming

In addition to the input channel delay programming, the input bit delay programming feature provides users with more flexibility when designing the switch matrices at high-speed, in which the delay lines are easily created on PCM highways which are connected to the switch matrix cards.

By default, all input streams have zero bit delay such that Bit 7 is the first bit that appears after the input frame boundary, see Figure 16. The input delay is enabled by Bit 0 to 2 in the Stream Input Delay Registers (SIDR). The input bit delay can vary from 0 to 7 bits.

2.3.3 Fractional Input Bit Delay Programming

In addition to the input bit delay feature, the device allows users to change the sampling point of the input bit. By default, the sampling point is at 3/4 bit. Users can change the sampling point to 1/4, 1/2, 3/4 or 4/4 bit position by programming Bit 3 and 4 of the Stream Input Control Registers (SICR).

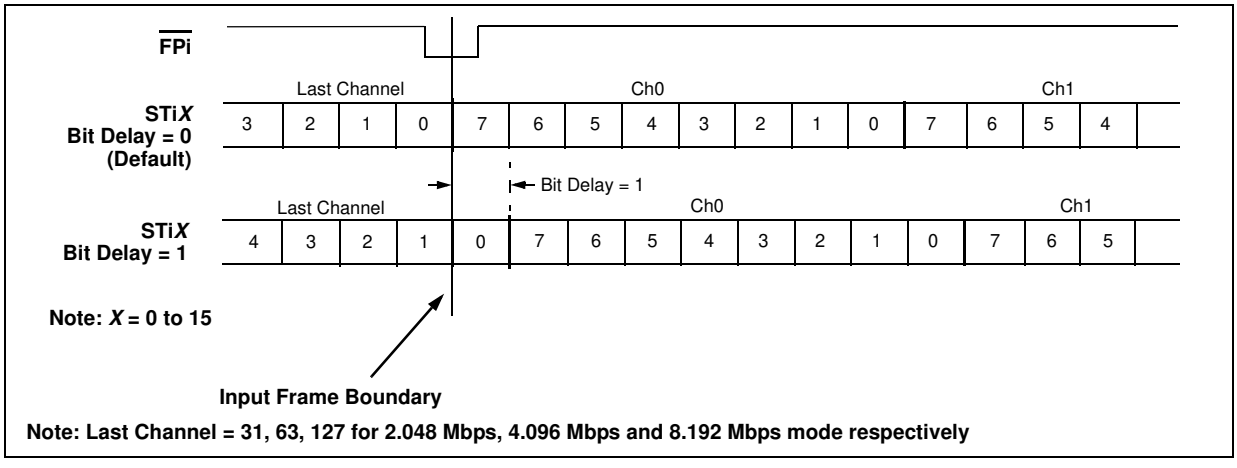

Figure 16 - Input Bit Delay Timing Diagram

2.3.4 Output Channel Delay Programming

This feature allows each output stream to have a different output frame boundary with respect to the output frame boundary defined by the output frame pulse ($\overline{FPo0}$, $\overline{FPo1}$ and $\overline{FPo2}$) and the output clock ($\overline{CKo0}$, $\overline{CKo1}$ or $\overline{CKo2}$). By default, all output streams have zero channel delay such that Ch 0 is the first channel that appears after the output frame boundary as shown in Figure 17. Different output channel delay can be set by programming Bit 5 to 11 in the Stream Output Offset Registers (SOOR). The output channel delay can vary from 0 to 31, 0 to 63 and 0 to 127 for the 2.048 Mbps, 4.096 Mbps and 8.192 Mbps modes respectively.

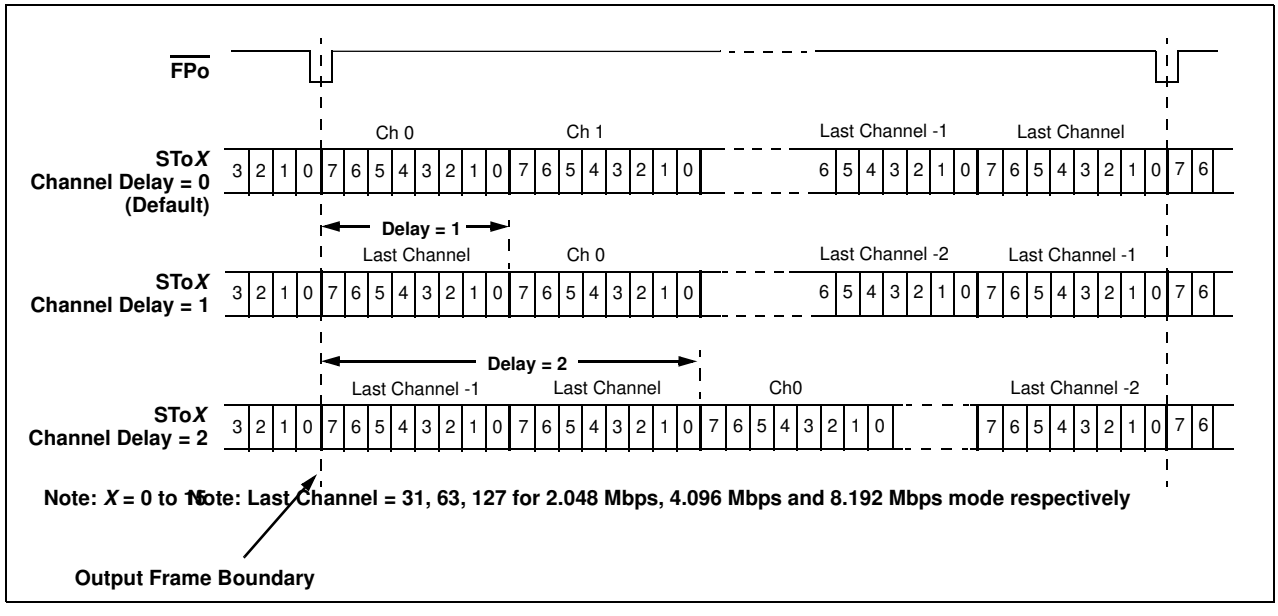

Figure 17 - Output Channel Delay Timing Diagram

2.3.5 Output Bit Delay Programming

This feature is used to delay the output data bit of individual output streams with respect to the output frame boundary. Each output stream can have its own bit delay value.

By default, all output streams have zero bit delay such that Bit 7 is the first bit that appears after the output frame boundary (see Figure 18 on page 25). Different output bit delay can be set by programming Bit 2 to 4 in the Stream Output Offset Registers. The output bit delay can vary from 0 to 7 bits.

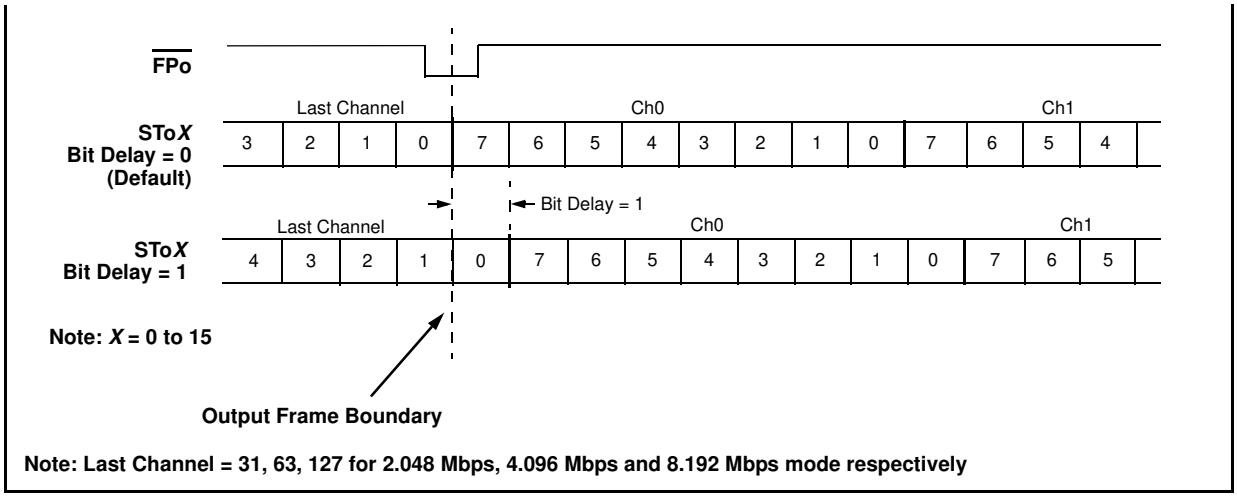

Figure 18 - Output Bit Delay Timing Diagram

2.3.6 Fractional Output Bit Advancement Programming

In addition to the output bit delay, the device is also capable of performing fractional output bit advancement. This feature offers a better resolution for the output bit delay adjustment. The fractional output bit advancement is useful in compensating for various parasitic loadings on the serial data output pins.

By default, all output streams have zero fractional bit advancement such that Bit 7 is the first bit that appears after the output frame boundary as shown in Figure 19. The fractional output bit advancement is enabled by Bit 0 to 1 in the Stream Output Offset Registers. The fractional bit advancement can vary from 0, 1/4, 1/2 or 3/4 bit.

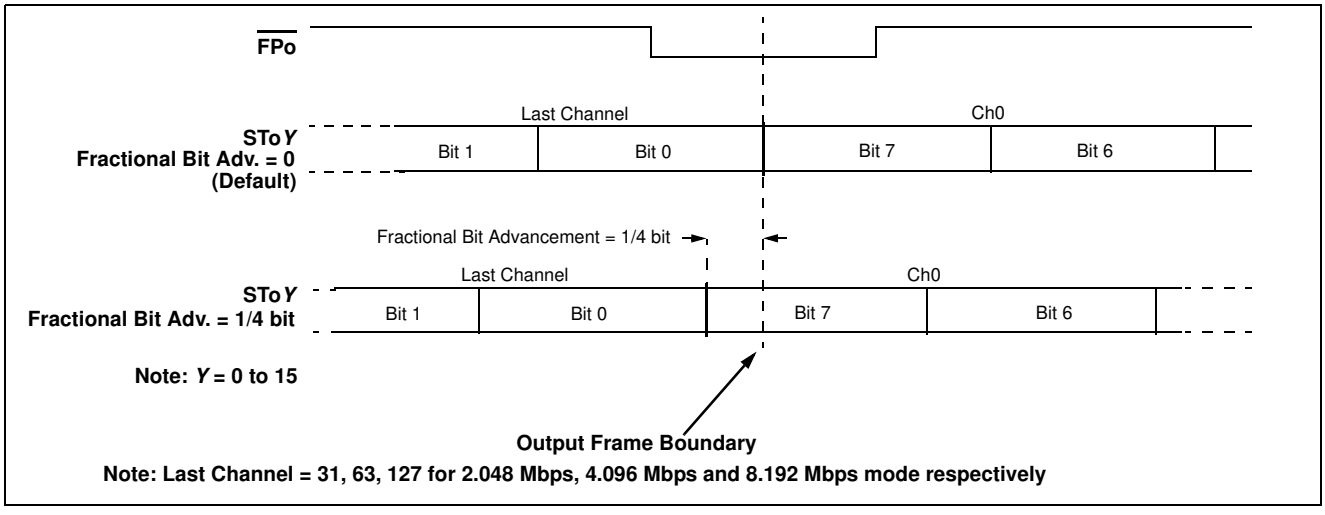

Figure 19 - Fractional Output Bit Advancement Timing Diagram