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Features

September 2011

- 2048 channel x 2048 channel non-blocking digital Time Division Multiplex (TDM) switch at 8.192 and 16.384 Mbps or using a combination of ports running at 2.048, 4.096, 8.192 and 16.384 Mbps
- 32 serial TDM input, 32 serial TDM output streams
- Integrated Digital Phase-Locked Loop (DPLL) exceeds Telcordia GR-1244-CORE Stratum 4E specifications
- Output clocks have less than 1 ns of jitter (except for the 1.544 MHz output)
- DPLL provides holdover, freerun and jitter attenuation features with four independent reference source inputs
- Exceptional input clock cycle to cycle variation tolerance (20 ns for all rates)
- Output streams can be configured as bi-directional for connection to backplanes

Ordering Information

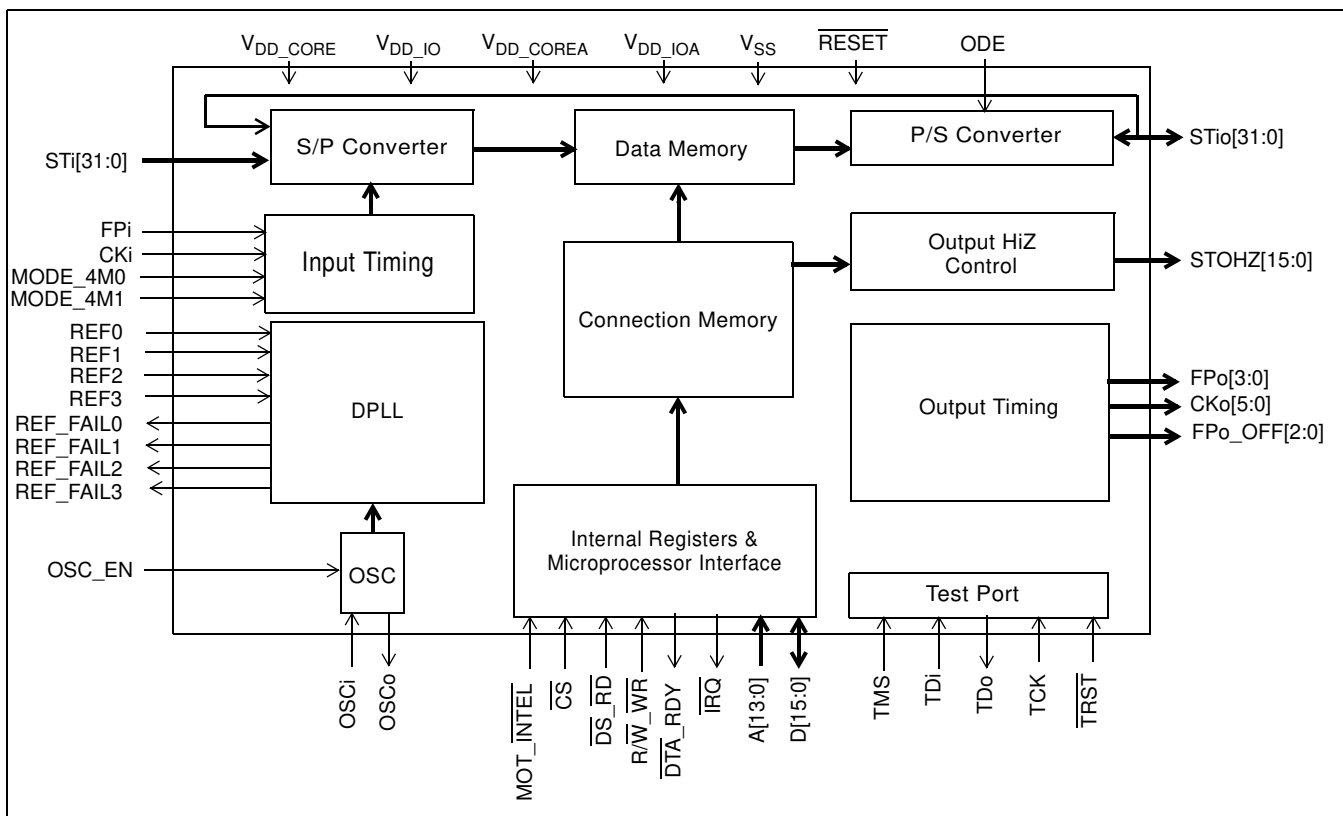
ZL50019GAC	256 Ball PBGA	Trays
ZL50019QCG1	256 Lead LQFP*	Trays, Bake & Drypack
ZL50019GAG2	256 Ball PBGA**	Trays, Bake & Drypack

*Pb Free Matte Tin

**Pb Free Tin/Silver/Copper

-40°C to +85°C

- Per-stream input and output data rate conversion selection at 2.048, 4.096, 8.192 or 16.384 Mbps. Input and output data rates can differ
- Per-stream high impedance control outputs (STOHZ) for 16 output streams
- Per-stream input bit delay with flexible sampling point selection
- Per-stream output bit and fractional bit advancement


Figure 1 - ZL50019 Functional Block Diagram

Zarlink Semiconductor US Patent No. 5,602,884, UK Patent No. 0772912,
 France Brevete S.G.D.G. 0772912; Germany DBP No. 69502724.7-08

- Per-channel ITU-T G.711 PCM A-Law/ μ -Law Translation
- Four frame pulse and six reference clock outputs
- Three programmable delayed frame pulse outputs
- Input clock: 4.096 MHz, 8.192 MHz, 16.384 MHz
- Input frame pulses: 61 ns, 122 ns, 244 ns
- Per-channel constant or variable throughput delay for frame integrity and low latency applications
- Per Stream (32) Bit Error Rate Test circuits complying to ITU-O.151
- Per-channel high impedance output control
- Per-channel message mode
- Control interface compatible with Intel and Motorola 16-bit non-multiplexed buses
- Connection memory block programming
- Supports ST-BUS and GCI-Bus standards for input and output timing
- IEEE-1149.1 (JTAG) test port
- 3.3 V I/O with 5 V tolerant inputs; 1.8 V core voltage

Applications

- PBX and IP-PBX
- Small and medium digital switching platforms
- Remote access servers and concentrators
- Wireless base stations and controllers
- Multi service access platforms
- Digital Loop Carriers
- Computer Telephony Integration

Description

The ZL50019 is a maximum 2,048 x 2,048 channel non-blocking digital Time Division Multiplex (TDM) switch. It has thirty-two input streams (STi0 - 31) and thirty-two output streams (STio0 - 31). The device can switch 64 kbps and Nx64 kbps TDM channels from any input stream to any output stream. Each of the input and output streams can be independently programmed to operate at any of the following data rates: 2.048, 4.096, 8.192 or 16.384 Mbps. The ZL50019 provides up to sixteen high impedance control outputs (STOHZ0 - 15) to support the use of external tristate drivers for the first sixteen output streams (STio0 - 15). The output streams can be configured to operate in bi-directional mode, in which case STi0 - 31 will be ignored.

The device contains two types of internal memory - data memory and connection memory. There are four modes of operation - Connection Mode, Message Mode, BER mode and high impedance mode. In Connection Mode, the contents of the connection memory define, for each output stream and channel, the source stream and channel (the actual data to be output is stored in the data memory). In Message Mode, the connection memory is used for the storage of microprocessor data. Using Zarlink's Message Mode capability, microprocessor data can be broadcast to the data output streams on a per-channel basis. This feature is useful for transferring control and status information for external circuits or other TDM devices. In BER mode the output channel data is replaced with a pseudorandom bit sequence (PRBS) from one of 32 PRBS generators that generates a $2^{15}-1$ pattern. On the input side channels can be routed to one of 32 bit error detectors. In high impedance mode the selected output channel can be put into a high impedance state.

When the device is operating as a timing master, the internal digital PLL is in use. In this mode, an external 20.000 MHz crystal is required for the on-chip crystal oscillator. The DPLL is phase-locked to one of four input reference signals (which can be 8 kHz, 1.544 MHz, 2.048 MHz, 4.096 MHz, 8.192 MHz, 16.384 MHz or 19.44 MHz provided on REF0 - 3). The on-chip DPLL operates in normal, holdover or freerun mode and offers jitter attenuation. The jitter attenuation function exceeds the Stratum 4E specification.

The configurable non-multiplexed microprocessor port allows users to program various device operating modes and switching configurations. Users can employ the microprocessor port to perform register read/write, connection memory read/write and data memory read operations. The port is configurable to interface with either Motorola or Intel-type microprocessors.

The device also supports the mandatory requirements of the IEEE-1149.1 (JTAG) standard via the test port.

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Changes Summary

Changes from the November 2006 issue to the September 2011 issue.

Page	Item	Change
1	Ordering Information	Removed leaded packages as per PCN notice.

The following table captures the changes from January 2006 to November 2006.

Page	Item	Change
1		Updated Ordering Information.

The following table captures the changes from the October 2004 issue.

Page	Item	Change
38, 70, 71	12.1, "DPLL Timing Modes" on page 38 RCCR Register bits "FDM1 - 0" on page 70 RCSR Register bits "DPM1 - 0" on page 71	<ul style="list-style-type: none"> The on-chip DPLL's normal, holdover, automatic, and freerun modes are now collectively referred to as DPLL timing modes instead of operation modes. This change is to avoid confusion with the two main device operating modes; the master and slave modes.
39	12.1.3.1, "Automatic Reference Switching Without Preferences" on page 39 and 12.1.3.2, "Automatic Reference Switching With Preference" on page 40	<ul style="list-style-type: none"> Section 12.1.3.1 and Section 12.1.3.2 added to clarify the DPLL's automatic reference switching with and without preference operations in Automatic Timing Mode.
67	Table 33, Lock Detector Threshold Register (LDTR) Bits	<ul style="list-style-type: none"> Clarified threshold calculations.
69	Table 36, "Reference Change Control Register (RCCR) Bits" Bits "PRS1 - 0" and Bits "PMS2 - 0"	<ul style="list-style-type: none"> Added description to clarify that only two consecutive references can be used in automatic timing mode with a preferred reference.

1.0 Pinout Diagrams

1.1 BGA Pinout

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	V _{SS}	STi29	STi28	STi27	STi25	STi26	STi24	NC	NC	STi22	STi23	STi21	STi20	NC	NC	V _{SS}
B	STi31	STi10	STi5	STi4	CKo2	STi0	CKo0	REF2	V _{DD_COREA}	FPI	CKi	IC_OPEN	IC_OPEN	OSCi	ODE	STi19
C	STi30	STi9	V _{SS}	STi7	STi6	STi1	CKo1	REF_FAIL2	V _{SS}	IC_OPEN	IC_OPEN	OSCo	IC_GND	V _{SS}	STi15	STi18
D	STi17	STi11	V _{DD_IO}	STi3	STi2	CKo4	REF3	REF1	REF_FAIL0	V _{SS}	FPo_OFF1	OSC_EN	STi13	V _{DD_IO}	STi14	STi16
E	STi16	STi14	STi8	V _{DD_IO}	V _{SS}	V _{DD_CORE}	REF_FAIL3	REF_FAIL1	REF0	NC	V _{DD_CORE}	V _{SS}	V _{DD_IO}	STi12	FPo2	STi17
F	STi19	STi15	STi12	STi13	V _{DD_IO}	V _{DD_CORE}	V _{DD_CORE}	V _{SS}	V _{SS}	V _{DD_CORE}	V _{DD_CORE}	V _{DD_IO}	IC_OPEN	FPo3	FPo_OFF2	STOZH15
G	STi18	RESET	IC_GND	IC_OPEN	TDo	V _{DD_IO}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{DD_IO}	A12	A13	FPo1	FPo0	STOZH14
H	STi21	V _{SS}	V _{SS}	V _{DD_COREA}	CKo5	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	A7	A9	A10	FPo_OFF0	A11	STOZH12
J	STi20	V _{DD_IOA}	V _{DD_IOA}	V _{SS}	V _{SS}	CKo3	V _{SS}	V _{SS}	V _{SS}	V _{SS}	A3	A4	A5	A8	A6	STOZH13
K	STi22	V _{SS}	TMS	V _{SS}	V _{DD_COREA}	V _{DD_IO}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{DD_IO}	IC_OPEN	A0	A2	A1	STOZH11
L	STi23	V _{DD_COREA}	TRST	TCK	V _{DD_IO}	V _{DD_CORE}	V _{DD_CORE}	V _{SS}	V _{SS}	V _{DD_CORE}	V _{DD_CORE}	V _{DD_IO}	STi10	STi11	STi9	STOZH10
M	STi25	NC	TDi	D0	V _{SS}	V _{DD_CORE}	V _{DD_CORE}	D6	D10	V _{DD_CORE}	V _{DD_CORE}	V _{SS}	MOT_INTEL	MODE_4M0	STi8	STOZH9
N	STi24	NC	V _{DD_IO}	STi0	STOZH3	D1	D5	D7	D11	D13	R/W_WR	DTA_RDY	STi4	V _{DD_IO}	STOZH5	STOZH8
P	STi26	NC	V _{SS}	STi1	STi3	STOZH1	D3	D8	D14	IRQ	STi5	STOZH4	STOZH6	V _{SS}	STOZH7	NC
R	STi27	NC	STOZH0	STi2	STOZH2	D2	D4	D9	D12	D15	CS	DS_RD	MODE_4M1	STi6	STi7	NC
T	V _{SS}	STi28	STi29	STi31	STi30	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	V _{SS}
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

Note: A1 corner identified by metallized marking.
Note: Pinout is shown as viewed through top of package.

Figure 2 - ZL50019 256-Ball 17 mm x 17 mm PBGA (as viewed through top of package)

1.2 QFP Pinout

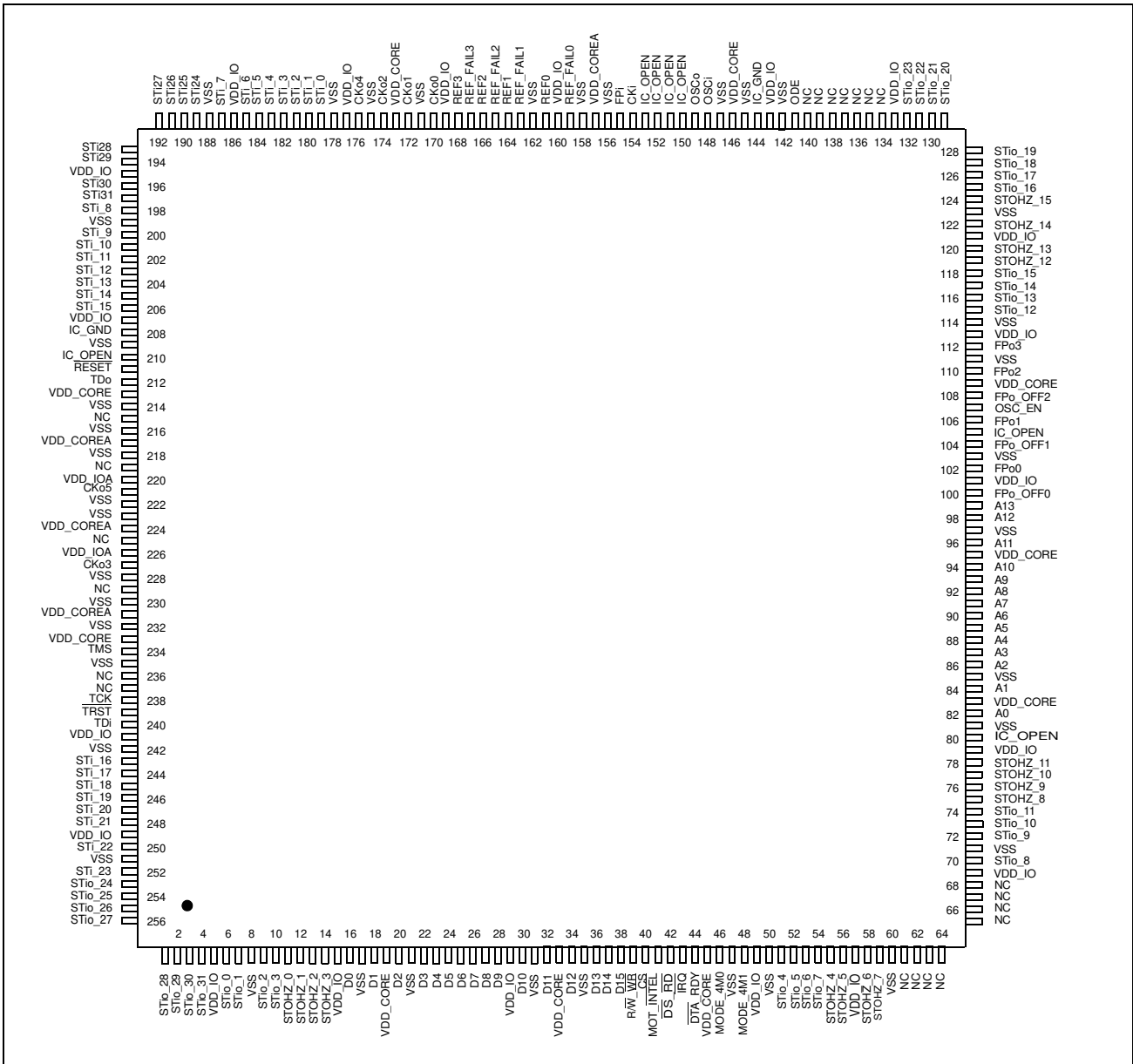


Figure 3 - ZL50019 256-Lead 28 mm x 28 mm LQFP (top view)

2.0 Pin Description

PBGA Pin Number	LQFP Pin Number	Pin Name	Description
E6, E11, F6, F7, F10, F11, L6, L7, L10, L11, M6, M7, M10, M11	19, 33, 45, 83, 95, 109, 146, 173, 213, 233	V_{DD_CORE}	Power Supply for the core logic: +1.8 V
H4, K5, B9, L2	217, 231, 157, 224	V_{DD_COREA}	Power Supply for analog circuitry: +1.8 V
D3, D14, E4, E13, F5, F12, G6, G11, K6, K11, L5, L12, N3, N14	5, 15, 29, 49, 57, 69, 79, 101, 113, 121, 133, 143, 160, 169, 177, 186, 195, 207, 241, 249	V_{DD_IO}	Power Supply for I/O: +3.3 V
J2, J3	220, 226	V_{DD_IOA}	Power Supply for the CKo5 and CKo3 outputs: +3.3 V
A1, A16, C3, C9, C14, D10, E5, E12, F8, F9, G7, G8, G9, G10, H2, H3, H6, H7, H8, H9, H10, J4, J5, J7, J8, J9, J10, K2, K4, K7, K8, K9, K10, L8, L9, M5, M12, P3, P14, T1, T16	8, 17, 21, 31, 35, 47, 50, 60, 71, 81, 85, 97, 103, 111, 114, 123, 142, 145, 147, 156, 158, 162, 171, 175, 178, 188, 199, 209, 214, 216, 218, 222, 223, 228, 230, 232, 235, 242, 251	V_{SS}	Ground

PBGA Pin Number	LQFP Pin Number	Pin Name	Description
K3	234	TMS	Test Mode Select (5 V-Tolerant Input with Internal Pull-up) JTAG signal that controls the state transitions of the TAP controller. This pin is pulled high by an internal pull-up resistor when it is not driven.
L4	238	TCK	Test Clock (5 V-Tolerant Schmitt-Triggered Input with Internal Pull-up) Provides the clock to the JTAG test logic.
L3	239	$\overline{\text{TRST}}$	Test Reset (5 V-Tolerant Input with Internal Pull-up) Asynchronously initializes the JTAG TAP controller by putting it in the Test-Logic-Reset state. This pin should be pulsed low during power-up to ensure that the device is in the normal functional mode. When JTAG is not being used, this pin should be pulled low during normal operation.
M3	240	TDi	Test Serial Data In (5 V-Tolerant Input with Internal Pull-up) JTAG serial test instructions and data are shifted in on this pin. This pin is pulled high by an internal pull-up resistor when it is not driven.
G5	212	TDo	Test Serial Data Out (5 V-Tolerant Three-state Output) JTAG serial data is output on this pin on the falling edge of TCK. This pin is held in high impedance state when JTAG is not enabled.
B12, B13, C10, C11, F13, G4, K12	80, 105, 150, 151, 152, 153, 210	IC_OPEN	Internal Test Mode (5 V-Tolerant Input with Internal Pull-down) These pins may be left unconnected.
C13, G3	144, 208	IC_GND	Internal Test Mode Enable (5 V-Tolerant Input) These pins MUST be low.
A8, A9, A14, A15, E10, M2, N2, P2, P16, R2, R16, T6, T7, T8, T9, T10, T11, T12, T13, T14, T15	61, 62, 63, 64, 65, 66, 67, 68, 134, 135, 136, 137, 138, 139, 140, 215, 219, 225, 229, 236, 237	NC	No Connect These pins MUST be left unconnected.

PBGA Pin Number	LQFP Pin Number	Pin Name	Description
M14, R13	46, 48	MODE_4M0, MODE_4M1	4M Input Clock Mode 0 to 1 (5 V-Tolerant Input with internal pull-down) These two pins should be tied together and are typically used to select CKi = 4.096 MHz operation. See Table 7, “ZL50019 Operating Modes” on page 37 for a detailed explanation. See Table 17, “Control Register (CR) Bits” on page 53 for CKi and FPi selection using the CKIN1 - 0 bits.
D12	107	OSC_EN	Oscillator Enable (5 V-Tolerant Input with Internal Pull-down) If tied high, this pin indicates that there is a 20 MHz external oscillator interfacing with the device. If tied low, there is no oscillator and CKi will be used for master clock generation. If the device is in master mode, an external oscillator is required and this pin MUST be tied high.
C12	149	OSCo	Oscillator Clock Output (3.3 V Output) If OSC_EN = ‘1’, this pin should be connected to a 20 MHz crystal (see Figure 23 on page 90) or left unconnected if a clock oscillator is connected to OSCi pin under normal operation (see Figure 24 on page 91). If OSC_EN = 0, this pin MUST be left unconnected.
B14	148	OSCi	Oscillator Clock Input (3.3 V Input) If OSC_EN = ‘1’, this pin should be connected to a 20 MHz crystal (see Figure 23 on page 90) or to a clock oscillator under normal operation (see Figure 24 on page 91). If OSC_EN = 0, this pin MUST be driven high or low by connecting either to V _{DD_IO} or to ground.
E9, D8, B8, D7	161, 164, 166, 168	REF0 - 3	DPLL Reference Inputs 0 to 3 (5 V-Tolerant Schmitt-Triggered Inputs) If the device is in Master mode, these input pins accept 8 kHz, 1.544 MHz, 2.048 MHz, 4.096 MHz, 8.192 MHz, 16.384 MHz or 19.44 MHz timing references independently. One of these inputs is defined as the preferred or forced input reference for the DPLL. The Reference Change Control Register (RCCR) selects the control of the preferred reference. These pins are ignored if the device is in slave mode unless SLV_DPLEN (bit 13) in the Control Register (CR) is set. When these input pins are not in use, they MUST be driven high or low by connecting either to V _{DD_IO} or to ground.
D9, E8, C8, E7	159, 163, 165, 167	REF_FAIL0 - 3	Failure Indication for DPLL References 0 to 3 (5 V-Tolerant Three-state Outputs) These output pins are used to indicate input reference failure when the device is in master mode. If REF0 fails, REF_FAIL0 will be driven high. If REF1 fails, REF_FAIL1 will be driven high. If REF2 fails, REF_FAIL2 will be driven high. If REF3 fails, REF_FAIL3 will be driven high. If the device is in slave mode, these pins are driven low, unless SLV_DPLEN (bit 13) in the Control Register (CR) is set.

PBGA Pin Number	LQFP Pin Number	Pin Name	Description
G15, G14, E15, F14	102, 106, 110, 112	FPo0 - 3	<p>ST-BUS/GCI-Bus Frame Pulse Outputs 0 to 3 (5 V-Tolerant Three-state Outputs)</p> <p>FPo0: 8 kHz frame pulse corresponding to the 4.096 MHz output clock of CKo0. FPo1: 8 kHz frame pulse corresponding to the 8.192 MHz output clock of CKo1. FPo2: 8 kHz frame pulse corresponding to 16.384 MHz output clock of CKo2. FPo3: Programmable 8 kHz frame pulse corresponding to 4.096 MHz, 8.192 MHz, 16.384 MHz, or 32.768 MHz output clock of CKo3. In Divided Slave modes, the frame pulse width of FPo0 - 3 cannot be narrower than the input frame pulse (FPi) width.</p>
H14, D11	100, 104	FPo_OFF0 - 1	<p>Generated Offset Frame Pulse Outputs 0 to 1 (5 V-Tolerant Three-state Outputs)</p> <p>Individually programmable 8 kHz frame pulses, offset from the output frame boundary by a programmable number of channels.</p>
F15	108	FPo_OFF2 or FPo5	<p>Generated Offset Frame Pulse Output 2 or 19.44 MHz Frame Pulse Output (5 V-Tolerant Three-state Output)</p> <p>As FPo_OFF2, this is an individually programmable 8 kHz frame pulse, offset from the output frame boundary by a programmable number of channels. By programming the FP19EN (bit 10) of FPOFF2 register to high, this signal becomes FPo5, a non-offset frame pulse corresponding to the 19.44 MHz clock presented on CKo5. FPo5 is only available in Master mode or when the SLV_DPLLEN bit in the Control Register is set high while the device is in one of the slave modes.</p>
B7, C7, B5, J6, D6, H5	170, 172, 174, 227, 176, 221	CKo0 - 5	<p>ST-BUS/GCI-Bus Clock Outputs 0 to 5 (5 V-Tolerant Three-state Outputs)</p> <p>CKo0: 4.096 MHz output clock. CKo1: 8.192 MHz output clock. CKo2: 16.384 MHz output clock. CKo3: 4.096 MHz, 8.192 MHz, 16.384 MHz or 32.768 MHz programmable output clock. CKo4: 1.544 MHz or 2.048 MHz programmable output clock. CKo5: 19.44 MHz output clock. See Section 6.0 on page 24 for details. In Divided Slave mode, the frequency of CKo0 - 3 cannot be higher than input clock (CKi). CKo4 and CKo5 are only available in Master mode or when the SLV_DPLLEN bit in the Control Register is set high while the device is in one of the slave modes.</p>

PBGA Pin Number	LQFP Pin Number	Pin Name	Description
B10	155	FPI	<p>ST-BUS/GCI-Bus Frame Pulse Input (5 V-Tolerant Schmitt-Triggered Input)</p> <p>This pin accepts the frame pulse which stays active for 61 ns, 122 ns or 244 ns at the frame boundary. The frame pulse frequency is 8 kHz. The frame pulse associated with the highest input or output data rate must be applied to this pin when the device is operating in Divided Slave mode or Master mode. The exception is if the device is operating in Master mode with loopback (i.e., CKi_LP is set in the Control Register). In that case, this input must be tied high or low externally. When the device is operating in Multiplied Slave mode, the frame pulse associated with the highest input data rate must be applied to this pin. For all modes (except Master mode with loopback), if the data rate is 16.384 Mbps, a 61 ns wide frame pulse must be used. By default, the device accepts a negative frame pulse in ST-BUS format, but it can accept a positive frame pulse instead if the FPINP bit is set high in the Control Register (CR). It can accept a GCI-formatted frame pulse by programming the FPINPOS bit in the Control Register (CR) to high.</p>
B11	154	CKi	<p>ST-BUS/GCI-Bus Clock Input (5 V-Tolerant Schmitt Triggered The Input)</p> <p>This pin accepts a 4.096 MHz, 8.192 MHz or 16.384 MHz clock. The clock frequency associated with twice the highest input or output data rate must be applied to this pin when the device is operating in either Divided Slave mode or Master mode. The exception is if the device is operating in Master mode with loopback (i.e., CKi_LP is set in the Control Register). In that case, this input must be tied high or low externally. The clock frequency associated with twice the highest input data rate must be applied to this pin when the device is operating in Multiplied Slave mode. In all modes of operation (except Master mode with loopback), when data is running at 16.384 Mbps, a 16.384 MHz clock must be used. By default, the clock falling edge defines the input frame boundary, but the device allows the clock rising edge to define the frame boundary by programming the CKINP bit in the Control Register (CR).</p>

PBGA Pin Number	LQFP Pin Number	Pin Name	Description
B6, C6, D5, D4, B4, B3, C5, C4, E3, C2, B2, D2, F3, F4, E2, F2, E1, D1, G1, F1, J1, H1, K1, L1, A7, A5, A6, A4, A3, A2, C1, B1	179, 180, 181, 182, 183, 184, 185, 187, 198, 200, 201, 202, 203, 204, 205, 206, 243, 244, 245, 246, 247, 248, 250, 252, 189, 190, 191, 192, 193, 194, 196, 197	STi0 - 31	Serial Input Streams 0 to 31 (5 V-Tolerant Inputs with Enabled Internal Pull-downs) The data rate of each input stream can be selected independently using the Stream Input Control Registers (SICR[n]). In the 2.048 Mbps mode, these pins accept serial TDM data streams at 2.048 Mbps with 32 channels per frame. In the 4.096 Mbps mode, these pins accept serial TDM data streams at 4.096 Mbps with 64 channels per frame. In the 8.192 Mbps mode, these pins accept serial TDM data streams at 8.192 Mbps with 128 channels per frame. In the 16.384 Mbps mode, these pins accept TDM data streams at 16.384 Mbps with 256 channels per frame.
N4, P4, R4, P5, N13, P11, R14, R15, M15, L15, L13, L14, E14, D13, D15, C15, D16, E16, C16, B16, A13, A12, A10, A11, N1, M1, P1, R1, T2, T3, T5, T4	6, 7, 9, 10, 51, 52, 53, 54, 70, 72, 73, 74, 115, 116, 117, 118, 125, 126, 127, 128, 129, 130, 131, 132, 253, 254, 255, 256, 1, 2, 3, 4	STio0 - 31	Serial Output Streams 0 to 31 (5 V-Tolerant Slew-Rate-Limited Three-state I/Os with Enabled Internal Pull-downs) The data rate of each output stream can be selected independently using the Stream Output Control Registers (SOCR[n]). In the 2.048 Mbps mode, these pins output serial TDM data streams at 2.048 Mbps with 32 channels per frame. In the 4.096 Mbps mode, these pins output serial TDM data streams at 4.096 Mbps with 64 channels per frame. In the 8.192 Mbps mode, these pins output serial TDM data streams at 8.192 Mbps with 128 channels per frame. In the 16.384 Mbps mode, these pins output serial TDM data streams at 16.384 Mbps with 256 channels per frame. These output streams can be used as bi-directionals by programming BDH (bit 7) and BDL (bit 6) of Internal Mode Selection (IMS) register.
R3, P6, R5, N5, P12, N15, P13, P15, N16, M16, L16, K16, H16, J16, G16, F16	11, 12, 13, 14, 55, 56, 58, 59, 75, 76, 77, 78, 119, 120, 122, 124	STOHZ0 - 15	Serial Output Streams High Impedance Control 0 to 15 (5 V-Tolerant Slew-Rate-Limited Three-state Outputs) These pins are used to enable (or disable) external three-state buffers. When an output channel is in the high impedance state, the STOHZ drives high for the duration of the corresponding output channel. When the STi0 channel is active, the STOHZ drives low for the duration of the corresponding output channel. STOHZ outputs are available for STi0 - 157 only.

PBGA Pin Number	LQFP Pin Number	Pin Name	Description
B15	141	ODE	Output Drive Enable (5 V-Tolerant Input with Internal Pull-up) This is the output enable control for STio0 - 31 and the output-driven-high control for STOHz0 - 15. When it is high, STio0 - 31 and STOHz0 - 15 are enabled. When it is low, STio0 - 31 are tristated and STOHz0 - 15 are driven high.
M4, N6, R6, P7, R7, N7, M8, N8, P8, R8, M9, N9, R9, N10, P9, R10	16, 18, 20, 22, 23, 24, 25, 26, 27, 28, 30, 32, 34, 36, 37, 38	D0 - 15	Data Bus 0 to 15 (5 V-Tolerant Slew-Rate-Limited Three-state I/Os) These pins form the 16-bit data bus of the microprocessor port.
N12	44	$\overline{\text{DTA_RDY}}$	Data Transfer Acknowledgment_Ready (5 V-Tolerant Three-state Output) This active low output indicates that a data bus transfer is complete for the Motorola interface. For the Intel interface, it indicates a transfer is completed when this pin goes from low to high. An external pull-up resistor MUST hold this pin at HIGH level for the Motorola mode. An external pull-down resistor MUST hold this pin at LOW level for the Intel mode.
R11	40	$\overline{\text{CS}}$	Chip Select (5 V-Tolerant Input) Active low input used by the Motorola or Intel microprocessor to enable the microprocessor port access.
N11	39	$\overline{\text{R/W_WR}}$	Read/Write_Write (5 V-Tolerant Input) This input controls the direction of the data bus lines (D0 - 15) during a microprocessor access. For the Motorola interface, this pin is set high and low for the read and write access respectively. For the Intel interface, a write access is indicated when this pin goes low.
R12	42	$\overline{\text{DS_RD}}$	Data Strobe_Read (5 V-Tolerant Input) This active low input works in conjunction with $\overline{\text{CS}}$ to enable the microprocessor port read and write operations for the Motorola interface. A read access is indicated when it goes low for the Intel interface.
K13, K15, K14, J11, J12, J13, J15, H11, J14, H12, H13, H15, G12, G13	82, 84, 86, 87, 88, 89, 90, 91, 92, 93, 94, 96, 98, 99	A0 - 13	Address 0 to 13 (5 V-Tolerant Inputs) These pins form the 14-bit address bus to the internal memories and registers.

PBGA Pin Number	LQFP Pin Number	Pin Name	Description
M13	41	MOT_INTEL	Motorola_Intel (5 V-Tolerant Input with Enabled Internal Pull-up) This pin selects the Motorola or Intel microprocessor interface to be connected to the device. When this pin is unconnected or connected to high, Motorola interface is assumed. When this pin is connected to ground, Intel interface should be used.
P10	43	IRQ	Interrupt (5 V-Tolerant Three-state Output) This programmable active low output indicates that the internal operating status of the DPLL has changed. An external pull-up resistor MUST hold this pin at HIGH level.
G2	211	RESET	Device Reset (5 V-Tolerant Input with Internal Pull-up) This input (active LOW) puts the device in its reset state that disables the STio0 - 31 drivers and drives the STOHz0 - 15 outputs to high. It also preloads registers with default values and clears all internal counters. To ensure proper reset action, the reset pin must be low for longer than 1 μ s. Upon releasing the reset signal to the device, the first microprocessor access cannot take place for at least 600 μ s due to the time required to stabilize the device and the crystal oscillator from the power-down state. Refer to Section Section 17.2 on page 46 for details.

3.0 Device Overview

The device has thirty-two ST-BUS/GCI-Bus inputs (STi0 - 31) and thirty-two ST-BUS/GCI-Bus outputs (STio0 - 31). STio0 - 31 can also be configured as bi-directional pins, in which case STi0 - 31 will be ignored. It is a non-blocking digital switch with 2048 64 kbps channels and is capable of performing rate conversion between ST-BUS/GCI-Bus inputs and ST-BUS/GCI-Bus outputs. The ST-BUS/GCI-Bus inputs accept serial input data streams with data rates of 2.048 Mbps, 4.096 Mbps, 8.192 Mbps and 16.384 Mbps on a per-stream basis. The ST-BUS/GCI-Bus outputs deliver serial data streams with data rates of 2.048 Mbps, 4.096 Mbps and, 8.192 Mbps and 16.384 Mbps on a per-stream basis. The device also provides sixteen high impedance control outputs (STOHz0 - 15) to support the use of external ST-BUS/GCI-Bus tristate drivers for the first sixteen ST-BUS/GCI-Bus outputs (STio0 -15).

By using Zarlink's message mode capability, microprocessor data stored in the connection memory can be broadcast to the output streams on a per-channel basis. This feature is useful for transferring control and status information for external circuits or other ST-BUS/GCI-Bus devices.

The device uses the ST-BUS/GCI-Bus input frame pulse (FPi) and the ST-BUS/GCI-Bus input clock (CKi) to define the input frame boundary and timing for sampling the ST-BUS/GCI-Bus input streams with various data rates. The output data streams will be driven by and have their timing defined by FPi and CKi in Divided Slave mode. In Multiplied Slave mode, the output data streams will be driven by an internally generated clock, which is multiplied from CKi internally. In Master mode, the on-chip DPLL will drive the output data streams and provide output clocks and frame pulses. Refer to Application Note ZLAN-120 for further explanation of the different modes of operation.

When the device is in Master mode, the DPLL is phase-locked to one of four DPLL reference signals, REF0 - 3, which are sourced by an external 8 kHz, 1.544 MHz, 2.048 MHz, 4.096 MHz, 8.192 MHz, 16.384 MHz or 19.44 MHz reference signal. The on-chip DPLL also offers jitter attenuation, reference switching, reference monitoring, freerun and holdover functions. The jitter performance exceeds the Stratum 4E specification. The intrinsic jitter of all output clocks is less than 1 ns (except for the 1.544 MHz output).

There are two slave modes for this device:

The first is the Divided Slave mode. In this mode, output streams are clocked by input CKi. Therefore the output streams have exactly the same jitter as the input streams. The output data rate can be the same as or lower than the input data rate, but the output data rate cannot be higher than what CKi can drive. For example, if CKi is 4.096 MHz, the output data rate cannot be higher than 2.048 Mbps. For the Divided Slave mode, the core master clock can be either 98.304 MHz, which is multiplied from CKi, or 100 MHz, which is multiplied from a 20 MHz oscillator. The Divided Slave mode with 98.304 MHz core master clock is called Divided Slave with CKi mode, and the mode with 100 MHz core master clock is called Divided Slave with OSC mode.

The second slave mode is called Multiplied Slave mode. In this mode, CKi is used to generate a 16.384 MHz clock internally, and output streams are driven by this 16.384 MHz clock. In Multiplied Slave mode, the data rate of output streams can be any rate, but output jitter may not be exactly the same as input jitter.

A Motorola or Intel compatible non-multiplexed microprocessor port allows users to program the device to operate in various modes under different switching configurations. Users can use the microprocessor port to perform internal register and memory read and write operations. The microprocessor port has a 16-bit data bus, a 14-bit address bus and six control signals (MOT_INTEL, CS, DS_RD, R/W_WR, IRQ and DTA_RDY).

The device supports the mandatory requirements of the IEEE-1149.1 (JTAG) standard via the test port.

4.0 Data Rates and Timing

The ZL50019 has 32 serial data inputs and 32 serial data outputs. Each stream can be individually programmed to operate at 2.048 Mbps, 4.096 Mbps, 8.192 Mbps or 16.384 Mbps. Depending on the data rate there will be 32 channels, 64 channels, 128 channels or 256 channels, respectively, during a 125 μ s frame.

The output streams can be programmed to operate as bi-directional streams. The output streams are divided into two groups to be programmed into bi-directional mode. By setting BDL (bit 6) in the Internal Mode Selection (IMS) register, input streams 0 - 15 (STi0 - 15) are internally tied low, and output streams 0 - 15 (STio0 - 15) are set to operate in a bi-directional mode. Similarly, when BDH (bit 7) in the Internal Mode Selection (IMS) register is set, input streams 16 - 31 (STi16 - 31) are internally tied low, and output streams 16 - 31 (STio16 - 31) are set to operate in bi-directional mode. The groups do not have to be set into the same mode. Therefore it is possible to have half of the streams operating in bi-directional mode while the other half is operating in normal input/output mode.

The input data rate is set on a per-stream basis by programming STIN[n]DR3 - 0 (bits 3 - 0) in the Stream Input Control Register 0 - 31 (SICR0 - 31). The output data rate is set on a per-stream basis by programming STO[n]DR3 - 0 (bits 3 - 0) in the Stream Output Control Register 0 - 31 (SOCR0 - 31). The output data rates do not have to match or follow the input data rates. The maximum number of channels switched is limited to 2048 channels. If all 32 input streams were operating at 16.384 Mbps (256 channels per stream), this would result in 8192 channels. Memory limitations prevent the device from operating at this capacity. A maximum capacity of 2048 channels will occur if eight of the streams are operating at 16.384 Mbps, half of the streams are operating at 8.192 Mbps or all streams operating at 4.096 Mbps. With all streams operating at 2.048 Mbps, the capacity will be reduced to 1024 channels. However, as each stream can be programmed to a different data rate, any combination of data rates can be achieved, as long as the total channel count does not exceed 2048 channels. It should be noted that only full stream can be programmed for use. The device does not allow fractional streams.

4.1 External High Impedance Control, STOHz0 - 15

There are 16 external high impedance control signals, STOHz0 - 15, that are used to control the external drivers for per-channel high impedance operations. Only the first sixteen ST-BUS/GCI-Bus (STio0 - 15) outputs are provided with corresponding STOHz signals. The STOHz outputs deliver the appropriate number of control timeslot channels based on the output stream data rate. Each control timeslot lasts for one channel time. When the ODE pin is high and the OSB (bit 2) of the Control Register (CR) is also high, STOHz0 - 15 are enabled. When the ODE pin, OSB (bit 2) of the Control Register (CR) or the RESET pin is low, STOHz0 - 15 are driven high, together with all the ST-BUS/GCI-Bus outputs being tristated. Under normal operation, the corresponding STOHz outputs of any

unused ST-BUS/GCI-Bus channel (high impedance) are driven high. Refer to Figure 18 on page 33 for a diagrammatical explanation.

4.2 Input Clock (CKi) and Input Frame Pulse (FPi) Timing

The input clock for the ZL50019 can be arranged in one of three different ways. These different ways will be explained further in Section 11.1 to Section 11.3 on page 38. Depending on the mode of operation, the input clock, CKi, will be based on the highest data rate of either the input or both the input and output data rates. The user has to program the CKIN1 - 0 (bits 6 - 5) in the Control Register (CR) to indicate the width of the input frame pulse and the frequency of the input clock supplied to the device.

In Master mode and Divided Slave mode, the input clock, CKi, must be at least twice the highest input or output data rate. For example, if the highest input data rate is 4.096 Mbps and the highest output data rate is 8.192 Mbps, the input clock, CKi, must be 16.384 MHz, which is twice the highest overall data rate. The only exception to this is for 16.384 Mbps input or output data. In this case, the input clock, CKi, is equal to the data rate. The input frame pulse, FPi, must always follow CKi.

In Master mode, CKo2 and FPo2 can be programmed to be used as CKi and FPi by setting CKi_LP (bit 10) in the Control Register (CR). This will internally loop back the CKo2 and FPo2 timing. When this bit is set, CKi and FPi must be tied low or high externally.

Highest <i>Input or Output</i> Data Rate	CKIN 1-0 Bits	Input Clock Rate (CKi)	Input Frame Pulse (FPi)
16.384 Mbps or 8.192 Mbps	00	16.384 MHz	8 kHz (61 ns wide pulse)
4.096 Mbps	01	8.192 MHz	8 kHz (122 ns wide pulse)
2.048 Mbps	10	4.096 MHz	8 kHz (244 ns wide pulse)

Table 1 - CKi and FPi Configurations for Master and Divided Slave Modes

In Multiplied Slave mode, the input clock, CKi, must be at least twice the highest input data rate, regardless of the output data rate. Following the example above, if the highest input data rate is 4.096 Mbps, the input clock, CKi, must be 8.192 MHz, regardless of the output data rate. The only exception to this is for 16.384 Mbps input data. In this case, the input clock, CKi, is equal to the data rate. The input frame pulse, FPi, must always follow CKi.

Highest <i>Input</i> Data Rate	CKIN 1-0 Bits	Input Clock Rate (CKi)	Input Frame Pulse (FPi)
16.384 Mbps or 8.192 Mbps	00	16.384 MHz	8 kHz (61 ns wide pulse)
4.096 Mbps	01	8.192 MHz	8 kHz (122 ns wide pulse)
2.048 Mbps	10	4.096 MHz	8 kHz (244 ns wide pulse)

Table 2 - CKi and FPi Configurations for Multiplied Slave Mode

The ZL50019 accepts positive and negative ST-BUS/GCI-Bus input clock and input frame pulse formats via the programming of CKINP (bit 8) and FPINP (bit 7) in the Control Register (CR). By default, the device accepts the negative input clock format and ST-BUS format frame pulses. However, the switch can also accept a positive-going clock format by programming CKINP (bit 8) in the Control Register (CR). A GCI-Bus format frame pulse can be used by programming FPINPOS (bit 9) and FPINP (bit 7) in the Control Register (CR).

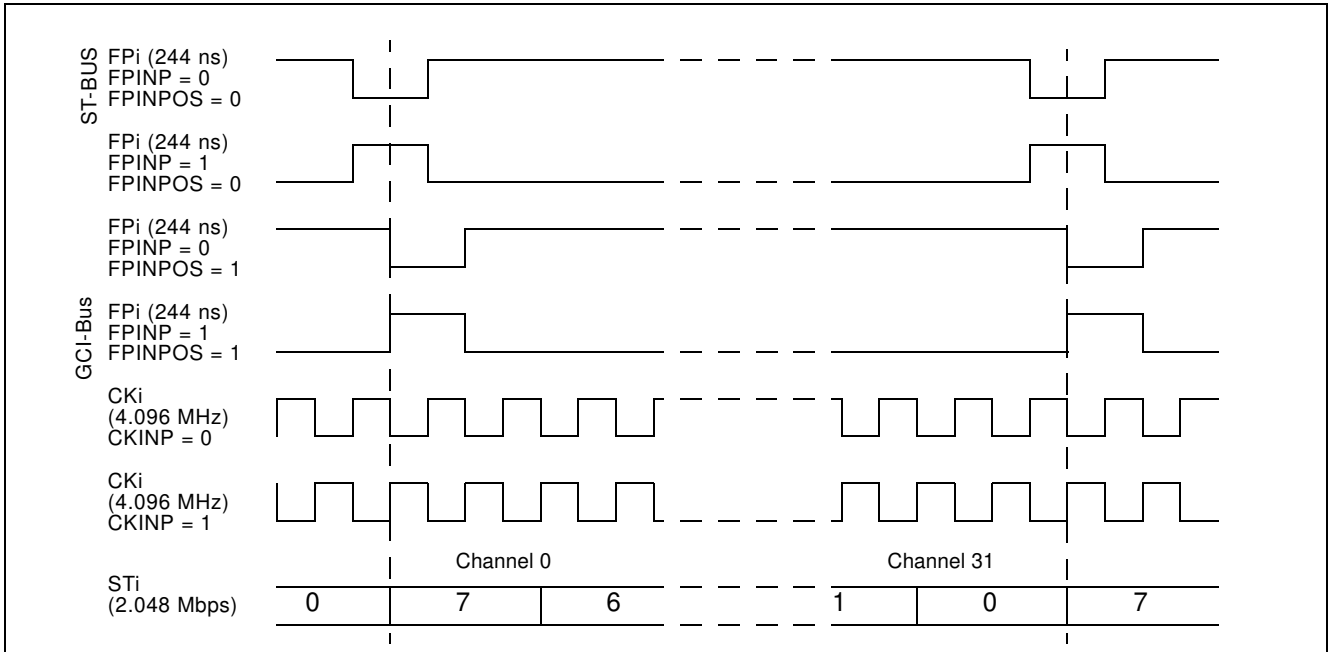


Figure 4 - Input Timing when CKIN1 - 0 bits = "10" in the CR

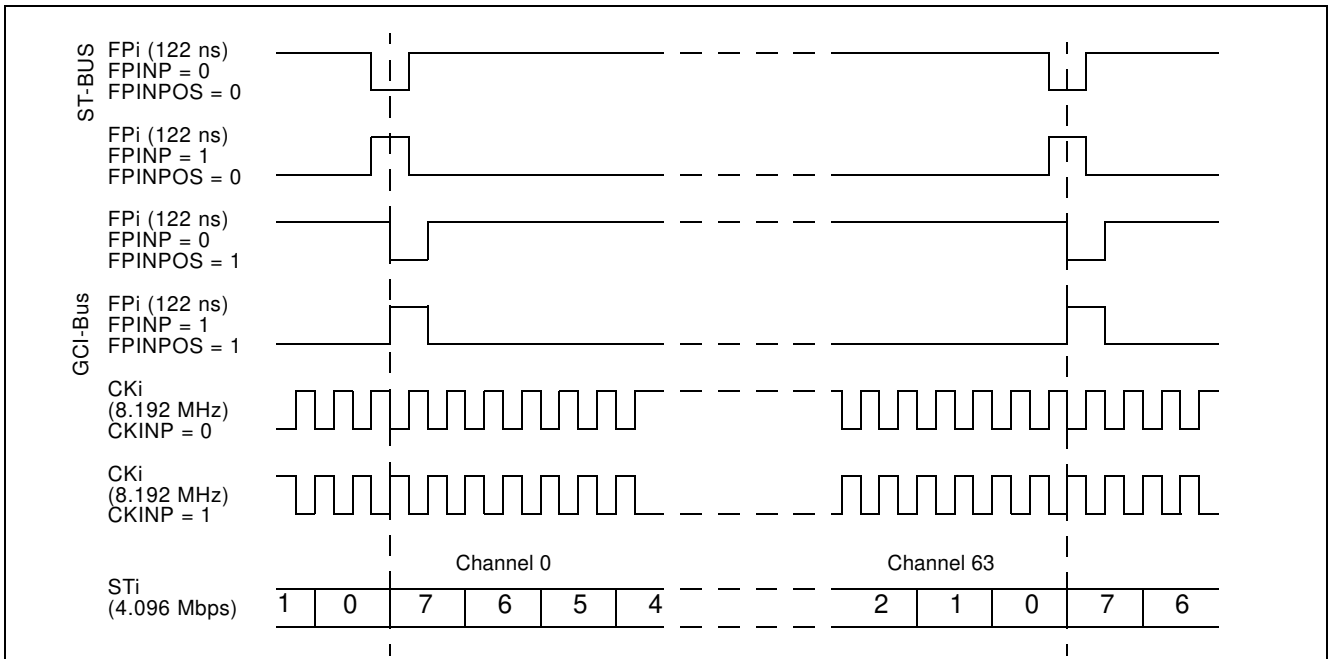


Figure 5 - Input Timing when CKIN1 - 0 bits = "01" in the CR

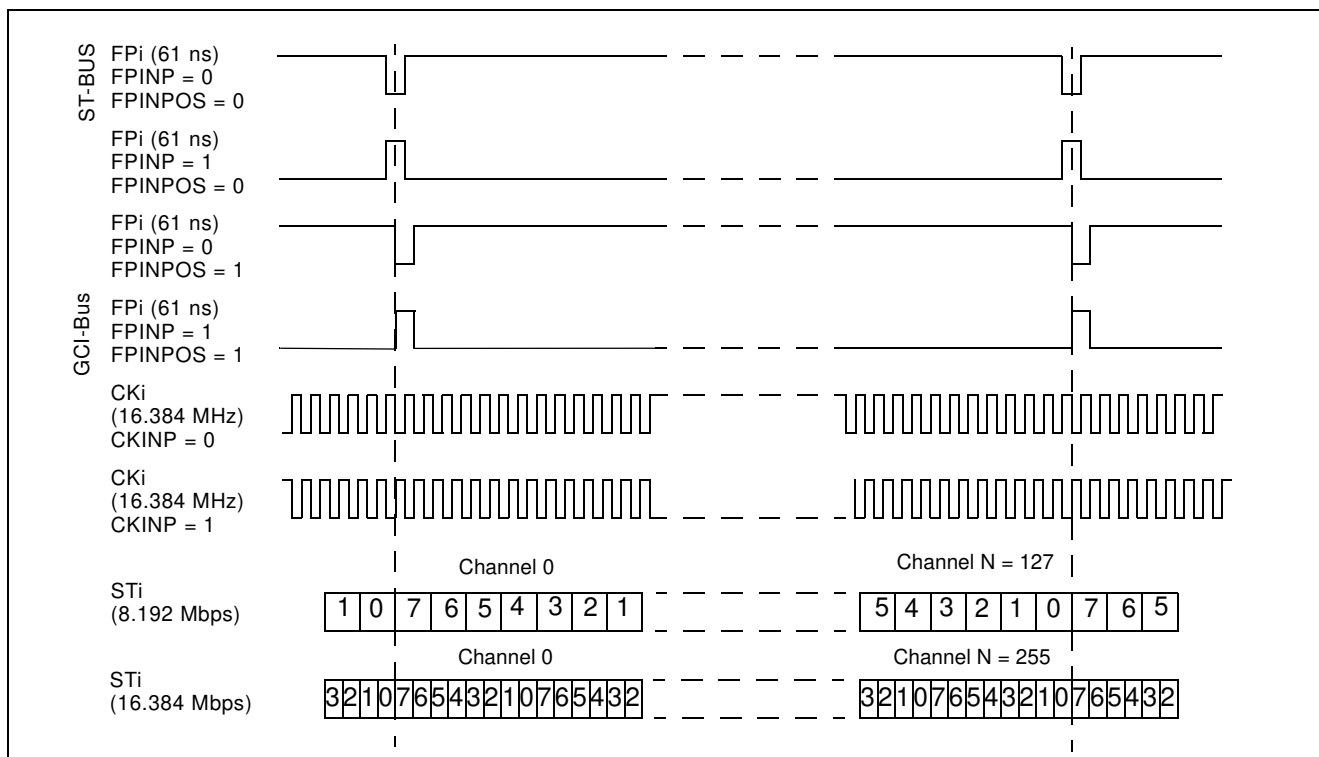


Figure 6 - Input Timing when CKIN1 - 0 = “00” in the CR

5.0 ST-BUS and GCI-Bus Timing

The ZL50019 is capable of operating using either the ST-BUS or GCI-Bus standards. The output timing that the device generates is defined by the bus standard. In the ST-BUS standard, the output frame boundary is defined by the falling edge of CKo while FPo is low. In the GCI-Bus standard, the frame boundary is defined by the rising edge of CKo while FPo goes high. The data rates define the number of channels that are available in a 125 μs frame pulse period.

By default, the ZL50019 is configured for ST-BUS input and output timing. To set the input timing to conform to the GCI-Bus standard, FPINPOS (bit 9) and FPINP (bit 7) in the Control Register (CR) must be set. To set output timing to conform to the GCI-Bus standard, FPO[n]P and FPO[n]POS must be set in the Output Clock and Frame Pulse Selection Register (OCFSR). The CKO[n]P bits in the Output Clock and Frame Pulse Selection Register control the polarity (positive-going or negative-going) of the output clocks.

6.0 Output Timing Generation

The ZL50019 generates frame pulse and clock timing. There are five output frame pulse pins (FPo0 - 3, 5) and six output clock pins (CKo0 - 5). All output frame pulses are 8 kHz output signals. By default, the output frame boundary is defined by the falling edge of the CKo0, while FPo0 is low. At the output frame boundary, the CKo1, CKo2 and CKo3 output clocks will by default have a falling edge, while FPo1, FPo2 and FPo3 will be low. At the output frame boundary, CKo4 will by default have a falling edge while FPo0 is low (CKo4 has no corresponding output frame pulse). At the output frame boundary, CKo5 will by default have a rising edge while FPo5 (FPo_OFF2) will be low. The duration of the frame pulse low cycle and the frequency of the corresponding output clock are shown in Table 3 on page 25. Every frame pulse and clock output can be tristated by programming the enable bits in the Internal Mode Selection (IMS) register.

Pin Name	Output Timing Rate	Output Timing Unit
FPo0 pulse width	244	ns
CKo0	4.096	MHz
FPo1 pulse width	122	ns
CKo1	8.192	MHz
FPo2 pulse width	61	ns
CKo2	16.384	MHz
FPo3 pulse width	244, 122, 61 or 30	ns
CKo3	4.096, 8.192, 16.384 or 32.768	MHz
CKo4	1.544 or 2.048	MHz
FPo5 pulse width	51	ns
CKo5	19.44	MHz

Table 3 - Output Timing Generation

The output timing is dependent on the operation mode that is selected. When the device is in Divided Slave mode, the frequencies on CKo0 - 3 cannot be greater than the input clock, CKi. For example, if the input clock is 8.192 MHz, the CKo2 pin will not produce a valid output clock and the CKo3 pin can only be programmed to output a 4.096 MHz or 8.192 MHz clock signal. The output clocks CKo4 - 5 will not generate valid outputs unless the SLV_DPLEN (bit 13) of the Control Register (CR) is set.

In Master mode there are programmable output frame pulse, FPo3, and clock pins, CKo3 and CKo4. The outputs from FPo3 and CKo3 are programmed by the CKOFPO3SEL1 - 0 (bits 13 - 12) in the Output Clock and Frame Pulse Selection (OCFSR) register. The output clock pin, CKo4, is controlled by setting the CKO4SEL (bit 14) in the OCFSR register.

In Multiplied Slave mode, CKo4 and CKo5 are not available unless SLV_DPLEN is set in the Control Register. All other clocks and frame pulses correspond to the timing shown in Table 3 above.

The device also delivers positive or negative output frame pulse and ST-BUS/GCI-Bus output clock formats via the programming of various bits in the Output Clock and Frame Pulse Selection Register (OCFSR). By default, the device delivers the negative output clock format. The ZL50019 can also deliver GCI-Bus format output frame pulses by programming bits of the Output Clock and Frame Pulse Selection Register (OCFSR). As there is a separate bit setting for each frame pulse output, some of the outputs can be set to operate in ST-BUS mode and others in GCI-Bus mode.

The following figures describe the usage of the FPO0P, FPO1P, FPO2P, FPO3P, CKO0P, CKO1P, CKO2P, CKO3P, CKO4P and CKO5P bits to generate the FPo0 - 3 and CKo0 - 5 timing. FPo_OFF2 is configured to provide the non-offset frame pulse corresponding to the 19.44 MHz clock on CKo5 by setting the FP19EN (bit 10) in the FPOFF2 register. In this instance, FPo_OFF2 can be labeled as FPo5.