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ZL50030

Flexible 4 K x 2 K Channel Digital Switch with H.110 Interface and 1 K x 1 K Local Switch

Data Sheet

January 2006

Features

- 4,096 x 2,048 blocking switching between backplane and local streams
- 1,024 x 1,024 non-blocking switching between local streams
- 2,048 x 2,048 non-blocking switching between backplane streams
- Rate conversion between backplane and local streams
- Backplane interface accepts data rates of 8.192 Mbps or 16.384 Mbps
- Local interface accepts data rates of 2.048 Mbps, 4.096 Mbps or 8.192 Mbps on a per group basis
- Meets all the key H.110 mandatory signal requirements including timing
- Per-channel variable or constant throughput delay
- Per-stream input delay, programmable for local streams on a per bit basis
- Per-stream output advancement, programmable for backplane and local streams
- Per-channel direction control for backplane streams and local streams
- Per-channel message mode for backplane and local streams
- Per-channel high impedance output control for backplane and local streams
- Compatible to Stratum 4 Enhanced clock switching standard
- Integrated PLL conforms to Telcordia GR-1244-CORE Stratum 4 Enhanced switching standard
  - Holdover Mode with holdover frequency stability of 0.07 ppm
  - Jitter attenuation from 1.52 Hz.
  - Time interval error (TIE) correction
  - Master and Slave mode operation
- Non-multiplexed microprocessor interface
- Connection memory block-programming for fast device initialization

Ordering Information

ZL50030GAC	220 Ball PBGA	Trays
ZL50030GAG2	220 Ball PBGA**	Trays

*Pb Free Tin/Silver/Copper

-40°C to +85°C

- Pseudo-Random Binary Sequence (PRBS) pattern generation and testing for backplane and local streams
- Conforms to the mandatory requirements of the IEEE-1149.1 (JTAG) standard
- 3.3 V operation with 5 V tolerant inputs and I/O's
- 5 V tolerant PCI driver on CT-Bus I/O's

Applications

- Carrier-grade VoIP Gateways
- IP-PBX and PABX
- Intregrated Access Devices
- Access Servers
- CTI Applications/CompactPCI® Platforms
- H.110, H.100, ST-BUS and proprietary Backplane Applications

Description

The ZL50030 Digital Switch provides switching capacities of 4,096 x 2,048 channels between backplane and local streams, 1,024 x 1,024 channels among local streams, and 2,048 x 2,048 channels among backplane streams. The local connected serial inputs and outputs have 32, 64 and 128 64 kbps channels per frame with data rates of 2.048, 4.096 and 8.192 Mbps respectively. The backplane connected serial inputs and outputs have 128 and 256 64 kbps channels per frame with data rates of 8.192 and 16.384 Mbps respectively.

The device has features that are programmable on a per-stream or a per-channel basis including message mode, input delay offset, output advancement offset, and direction control.

Zarlink Semiconductor US Patent No. 5,602,884, UK Patent No. 0772912, France Brevete S.G.D.G. 0772912; Germany DBP No. 69502724.7-08

The ZL50030 supports all three of the H.110 specification required clocking modes: Primary Master, Secondary Master and Slave.

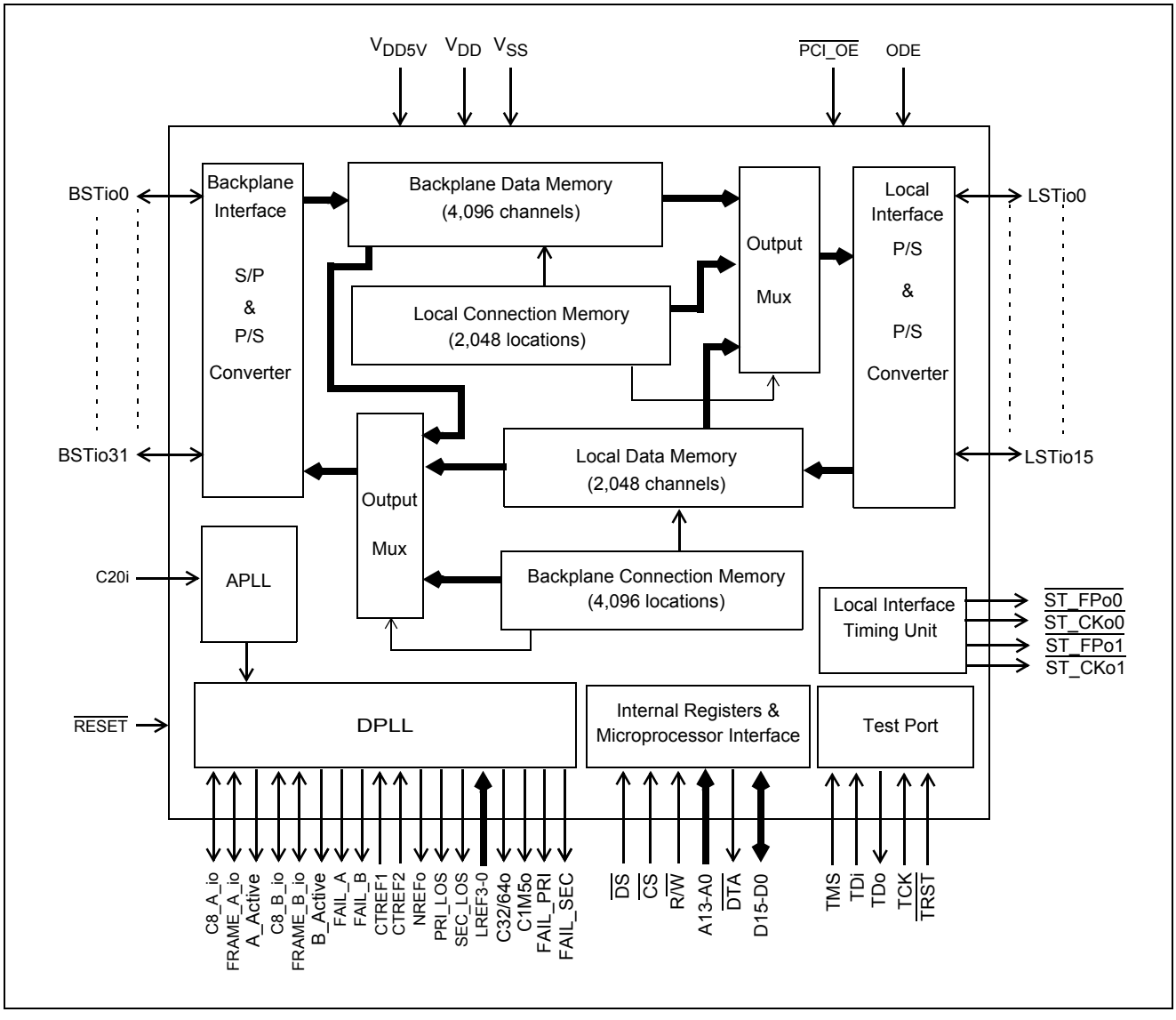


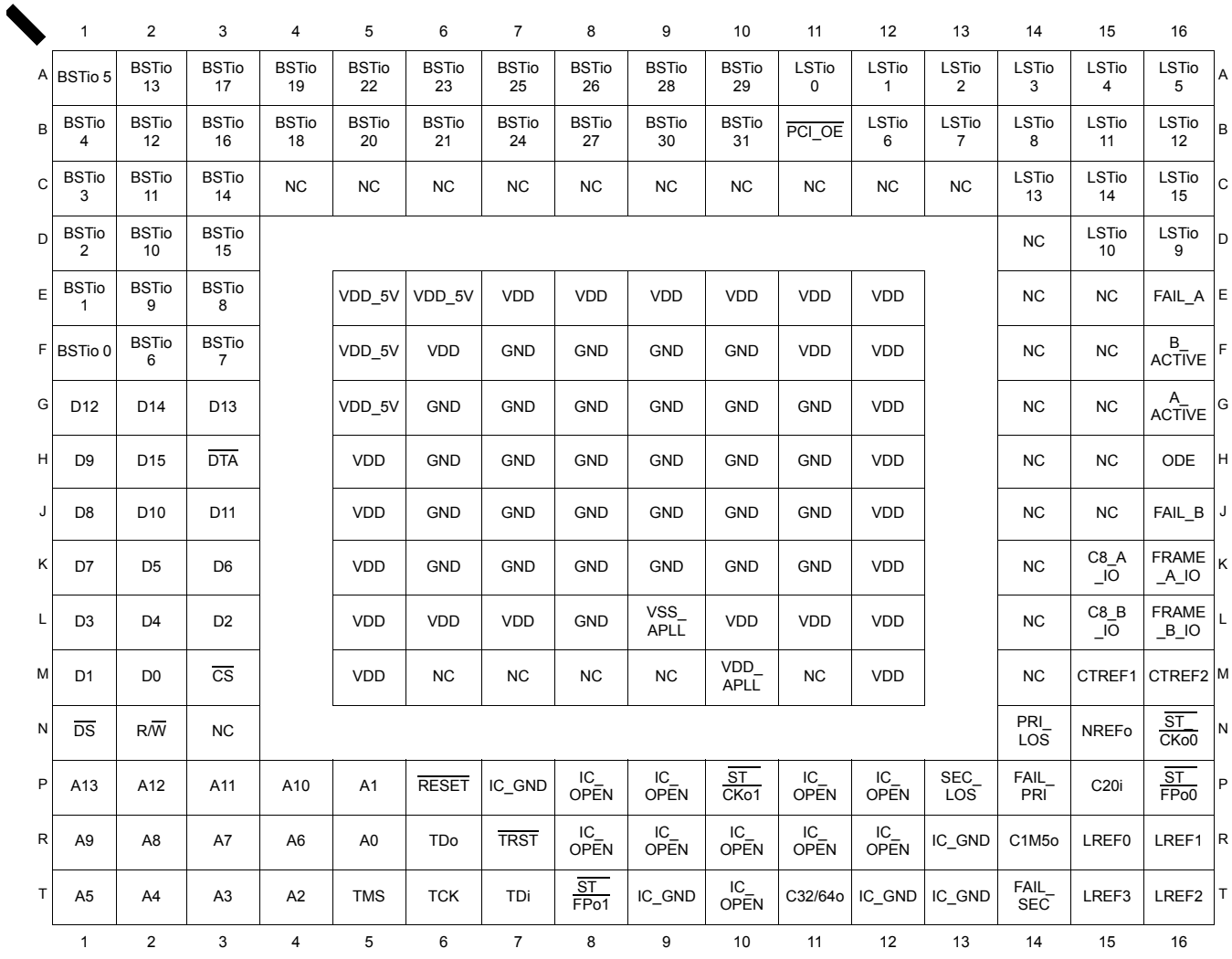
Figure 1 - Functional Block Diagram

Changes Summary

The following table captures the changes from the March 2004 issue.

Page	Item	Change
27, 47	Section 17.2 and Table 20	Added description clarifying that the MTIE reset must be set when the device is in the slave mode.
49	Table 21	Added MRST (bit 10) in Mode Selection table.
29, 30	Section 17.7 and Section 18.1	Deleted the intrinsic jitter descriptions in Section 17.7 and Section18.1, and replaced them with Table "AC Electrical Characteristics - Output Clock Jitter Generation (Unfiltered).
57	“AC Electrical Characteristics† - Output Frame Pulse and Output Clock Timing“	The parameter Delta, Δ, is replaced by actual numbers in all tables.
56	“AC Electrical Characteristics† - Input Frame Pulse and Input Clock Timing“	The Phase Correction, ϕ, is replaced by actual numbers.
65, 67	“AC Electrical Characteristics† - Backplane Serial Streams with Data Rate of 8 Mbps“, “AC Electrical Characteristics† - Backplane Serial Streams with Data Rate of 16 Mbps“ and “AC Electrical Characteristics† - Local Serial Stream Input Timing“	Input data sampling timings were updated for clarity purposes.

Pinout Diagram (as viewed through top of package)



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	BSTio 5	BSTio 13	BSTio 17	BSTio 19	BSTio 22	BSTio 23	BSTio 25	BSTio 26	BSTio 28	BSTio 29	LSTio 0	LSTio 1	LSTio 2	LSTio 3	LSTio 4	LSTio 5	A
B	BSTio 4	BSTio 12	BSTio 16	BSTio 18	BSTio 20	BSTio 21	BSTio 24	BSTio 27	BSTio 30	BSTio 31	$\overline{\text{PCI\_OE}}$	LSTio 6	LSTio 7	LSTio 8	LSTio 11	LSTio 12	B
C	BSTio 3	BSTio 11	BSTio 14	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	LSTio 13	LSTio 14	LSTio 15	C
D	BSTio 2	BSTio 10	BSTio 15											NC	LSTio 10	LSTio 9	D
E	BSTio 1	BSTio 9	BSTio 8		VDD_5V	VDD_5V	VDD	VDD	VDD	VDD	VDD	VDD		NC	NC	FAIL_A	E
F	BSTio 0	BSTio 6	BSTio 7		VDD_5V	VDD	GND	GND	GND	GND	VDD	VDD		NC	NC	B_ ACTIVE	F
G	D12	D14	D13		VDD_5V	GND	GND	GND	GND	GND	GND	VDD		NC	NC	A_ ACTIVE	G
H	D9	D15	$\overline{\text{DTA}}$		VDD	GND	GND	GND	GND	GND	GND	VDD		NC	NC	ODE	H
J	D8	D10	D11		VDD	GND	GND	GND	GND	GND	GND	VDD		NC	NC	FAIL_B	J
K	D7	D5	D6		VDD	GND	GND	GND	GND	GND	GND	VDD		NC	C8_A _IO	FRAME _A_IO	K
L	D3	D4	D2		VDD	VDD	VDD	GND	VSS_ APLL	VDD	VDD	VDD		NC	C8_B _IO	FRAME _B_IO	L
M	D1	D0	$\overline{\text{CS}}$		VDD	NC	NC	NC	NC	VDD_ APLL	NC	VDD		NC	CTREF1	CTREF2	M
N	$\overline{\text{DS}}$	R/$\overline{\text{W}}$	NC											PRI_ LOS	NREFo	$\overline{\text{ST\_ CKo0}}$	N
P	A13	A12	A11	A10	A1	$\overline{\text{RESET}}$	IC_GND	IC_ OPEN	IC_ OPEN	$\overline{\text{ST\_ CKo1}}$	IC_ OPEN	IC_ OPEN	SEC_ LOS	FAIL_ PRI	C20i	$\overline{\text{ST\_ FPo0}}$	P
R	A9	A8	A7	A6	A0	TDo	$\overline{\text{TRST}}$	IC_ OPEN	IC_ OPEN	IC_ OPEN	IC_ OPEN	IC_ OPEN	IC_GND	C1M5o	LREF0	LREF1	R
T	A5	A4	A3	A2	TMS	TCK	TDi	$\overline{\text{ST\_ FPo1}}$	IC_GND	IC_ OPEN	C32/64o	IC_GND	IC_GND	FAIL_ SEC	LREF3	LREF2	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

A1 corner identified by metalized marking.

Pin Description

PBGA Ball Number	Name	Description
E7, E8, E9, E10, E11, E12, F6, F11, F12, G12, H5, H12, J5, J12, K5, K12, L5, L6, L7, L10, L11, L12, M5, M12	V_{DD}	**+3.3 Volt Power Supply**
E5, E6, F5, G5	V_{DD5V}	**+5.0 V/+3.3 V Power Supply**. If 5 V power supply is tied to these pins, BSTio0-31 pins will meet 5 V PCI requirements. If 3.3 V power supply is tied to these pins, BSTio0-31 pins will meet 3.3 V PCI requirements.
F7, F8, F9, F10, G6, G7, G8, G9, G10, G11, H6, H7, H8, H9, H10, H11, J6, J7, J8, J9, J10, J11, K6, K7, K8, K9, K10, K11, L8	V_{SS}	**Ground**
M10	V_{DD_APLL}	**+3.3 Volt Analog PLL Power Supply**. No special filtering is required for this pin.
L9	V_{SS_APLL}	**Analog PLL Ground**
P6	$\overline{\text{RESET}}$	**Device Reset (5 V Tolerant Input).** This input (active low) puts the device in its reset state; this state clears the device's internal counters and registers. To ensure proper reset action, the reset pin must be low for longer than 400ns. To ensure proper operation, a delay of 100µs must be applied before the first microprocessor access is performed after the $\overline{\text{RESET}}$ pin is set high. The device reset also tristates LSTio0-15 and BSTio0-31. When in a $\overline{\text{RESET}}$ condition, the C8_A_io, FRAME_A_io, C8_B_io, and FRAME_B_io signals are tri-stated.
F1, E1, D1, C1, B1, A1, F2, F3, E3, E2, D2, C2, B2, A2, C3, D3	BSTio0-15	**Backplane Serial Input/Output Streams 0 - 15 (5 V Tolerant PCI I/Os).** In H.110 mode, these pins accept or output (selectable on a per channel basis) serial TDM data streams at 8.192 Mbps with 128 channels per stream. In the 16 Mbps mode, these pins accept or output serial TDM data streams at 16.384 Mbps with 256 channels per stream.
B3, A3, B4, A4, B5, B6, A5, A6, B7, A7, A8, B8, A9, A10, B9, B10	BSTio16 - 31	**Backplane Serial Input/Output Streams 16 - 31 (5 V Tolerant PCI I/Os).** In H.110 mode, these pins accept or output (selectable on a per channel basis) serial TDM data streams at 8.192 Mbps with 128 channels per stream. In the 16 Mbps mode, these pins are tristated internally and should be connected to ground.
A11, A12, A13, A14	LSTio0-3	**Group 0 Local Serial Bi-directional Streams 0 - 3 (5 V Tolerant I/Os).** In 2 Mbps, 4 Mbps or 8 Mbps mode, these pins accept or output (selectable on a per channel basis) data rates of 2.048, 4.096 or 8.192 Mbps with 32, 64 or 128 channels per stream respectively.

Pin Description (continued)

PBGA Ball Number	Name	Description
A15, A16, B12, B13	LSTio4 - 7	**Group 1 Local Serial Bi-directional Streams 4 - 7 (5 V Tolerant I/Os).** In 2 Mbps, 4 Mbps or 8 Mbps mode, these pins accept or output (selectable on a per channel basis) data rates of 2.048, 4.096 or 8.192 Mbps with 32, 64 or 128 channels per stream respectively.
B14, D16, D15, B15	LSTio8 - 11	**Group 2 Local Serial Bi-directional Streams 8 - 11 (5 V Tolerant I/Os).** In 2 Mbps, 4 Mbps or 8 Mbps mode, these pins accepts or output (selectable on a per channel basis) data rates of 2.048, 4.096 or 8.192 Mbps with 32, 64 or 128 channels per stream respectively.
B16, C14, C15, C16	LSTio12 - 15	**Group 3 Local Serial Bi-directional Streams 12 - 15 (5 V Tolerant I/Os).** In 2 Mbps, 4 Mbps or 8 Mbps mode, these pins accept or output (selectable on a per channel basis) data rates of 2.048, 4.096 or 8.192 Mbps with 32, 64 or 128 channels per stream respectively.
H16	ODE	**Output Drive Enable (5 V Tolerant Input).** When this pin is low, LSTio0-15, BSTio0-31, C1M5o, C32/64o, ST_CKo0, ST_CKo1, ST_FPo0 and ST_FPo1 outputs are all in high-impedance state. When ODE is high all of the aforementioned pins are active.
P15	C20i	**Master Clock (5 V Tolerant Input).** This pin accepts a 20.000 MHz clock.
K15	C8_A_io	**Clock A (5 V Tolerant I/O).** This is an 8.192 MHz clock with 50% duty cycle.
K16	FRAME_A_io	**Frame Reference A (5 V Tolerant I/O).** This is a 122ns wide, negative pulse, with 125us period.
G16	A_Active	**A Clock Active Indicator (5 V Tolerant Output):** This pin indicates whether the C8_A_io and the FRAME_A_io pins are inputs or outputs. When Bit 13 of the DOM1 register is low, this pin drives low and the C8_A_io and FRAME_A_io output drivers are disabled. When Bit 13 of the DOM1 register is high, this pin drives high and the C8_A_io and FRAME_A_io output drivers are enabled.
L15	C8_B_io	**Clock B (5 V Tolerant I/O).** This is an 8.192 MHz clock with 50% duty cycle.
L16	FRAME_B_io	**Frame Reference B (5 V Tolerant I/O).** This is a 122 ns wide, negative pulse, with 125us period.
F16	B_Active	**B Clock Active Indicator (5 V Tolerant Output):** This pin indicates whether the C8_B_io and the FRAME_B_io pins are inputs or outputs. When Bit 14 of the DOM1 register is low, this pin drives low and the C8_B_io and FRAME_B_io output drivers are disabled. When Bit 14 of the DOM1 register is high, this pins drives high and the C8_B_io and FRAME_B_io output drivers are enabled.
E16	FAIL_A	**A Failure (Output).** When the C8_A_io or the FRAME_A_io signal fails, this signal goes to high.
J16	FAIL_B	**B Failure (Output).** When the C8_B_io or the FRAME_B_io signal fails, this signal goes to high.
M15	CTREF1	**CT-Bus Reference 1 (5 V Tolerant Input).** This pin accepts 8 kHz, 1.544 MHz or 2.048 MHz network timing reference.

Pin Description (continued)

PBGA Ball Number	Name	Description
M16	CTREF2	**CT-Bus Reference 2 (5 V Tolerant Input).** This pin accepts 8 kHz, 1.544 MHz or 2.048 MHz network timing reference.
R15, R16, T16, T15	LREF0 - 3	**Local Reference (5 V Tolerant Inputs).** These pins accept 8 kHz, 1.544 MHz or 2.048 MHz local timing reference.
N15	NREFo	**Network Reference Output (Output).** Any local reference can be switched to this output. The output data rate can be either the same as the selected reference input data rate or divided to be 8 kHz.
N14	PRI_LOS	**Primary Reference Lost (5 V Tolerant Input).** When this signal is high, it indicates that PRIMARY REFERENCE is not valid. Combined with SEC_LOS input, this input pin is used in the External Reference Switching Mode of the DPLL.
P13	SEC_LOS	**Secondary Reference Lost (5 V Tolerant Input).** When this signal is high, it indicates that SECONDARY REFERENCE is not valid. Combined with the PRI_LOS input, this input pin is used in the External Reference Switching Mode of the DPLL.
P14	FAIL_PRI	**Primary Reference Failure (5 V Tolerant Output)**. This pin reflects the logic status of the PLS bit of the DPLL House Keeping Register (DHKR). When the primary reference fails, this signal goes to 1.
T14	FAIL_SEC	**Secondary Reference Failure (5 V Tolerant Output)**. This pin reflects the logic status of the SLS bit of the DPLL House Keeping Register (DHKR). When the secondary reference fails, this signal goes to 1.
T11	C32/64o	**C32/64o Clock (5 V Tolerant Output).** A 32.768 MHz output clock when the DPLL Clock Monitor register bit (CKM) is low. A 65.536 MHz clock when the DPLL Clock Monitor register bit (CKM) is high.
R14	C1M5o	**C1.5o Clock (5 V Tolerant Output).** A 1.544 MHz output clock.
P16	$\overline{\text{ST\_FPo0}}$	**ST-BUS Frame Pulse Output (5 V Tolerant Output).** The width of this output ST-BUS frame pulse can be 244 ns, 122 ns or 61 ns. The frequency is 8 kHz.
N16	$\overline{\text{ST\_CKo0}}$	**ST-BUS Clock Output (5 V Tolerant Output).** The frequency of this output ST-BUS clock can be 4.096 MHz, 8.192 MHz or 16.384 MHz.
T8	$\overline{\text{ST\_FPo1}}$	**ST-BUS Frame Pulse Output (5 V Tolerant Output)**. The width of this output ST-BUS frame pulse can be 244 ns, 122 ns or 61 ns. The frequency is 8 kHz.
P10	$\overline{\text{ST\_CKo1}}$	**ST-BUS Clock Output (5 V Tolerant Output)**. The frequency of this output ST-BUS clock can be 4.096 MHz, 8.192 MHz or 16.384 MHz.
M3	$\overline{\text{CS}}$	**Chip Select (5 V Tolerant Input).** This active low input is used by the microprocessor to access the microport.
N1	$\overline{\text{DS}}$	**Data Strobe (5 V Tolerant Input).** This active low input works in conjunction with $\overline{\text{CS}}$ to initiate the read and write cycles.
N2	R/$\overline{\text{W}}$	**Read/Write (5 V Tolerant Input).** This input controls the direction of the data bus lines (D0 - D15) during the microprocessor access.

Pin Description (continued)

PBGA Ball Number	Name	Description
R5, P5, T4, T3, T2, T1, R4, R3, R2, R1, P4, P3, P2, P1	A0 - A13	**Address 0 - 13 (5 V Tolerant Inputs).** These are the address lines to the internal memories and registers.
M2, M1, L3, L1, L2, K2, K3, K1, J1, H1, J2, J3, G1, G3, G2, H2	D0 - D15	**Data Bus 0 - 15 (5 V Tolerant I/Os)**. These pins form the 16-bit data bus of the microport.
H3	$\overline{\text{DTA}}$	**Data Transfer Acknowledge (5 V Tolerant Output)**. This active low output indicates that a data bus transfer is completed. A pull-up resistor is required to hold a high level.
B11	$\overline{\text{PCI\_OE}}$	**PCI Output Enable (3.3 V Tolerant Input)**. This active low input is the control signal used to tristate the BSTio0 - 31 pins during hot-swapping. During normal operation this signal should be low.
P7, R13, T9, T12, T13	IC_GND	**Internal Connection.** These pins **MUST** be connected to ground for normal operation.
P8, P9, P11, P12, R8, R9, R10, R11, R12, T10	IC_OPEN	**Internal Connection.** These pins **MUST** be left open for normal operation.
C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, D14, E14, E15, F14, F15, G14, G15, H14, H15, J14, J15, K14, L14, M6, M7, M8, M9, M11, M14, N3,	NC	**No Connection.** These pins **MUST** be left unconnected for normal operation.
T7	TDi	**Test Serial Data In (3.3 V Input with Internal pull-up)**. JTAG serial test instructions and data are shifted in on this pin. This pin is pulled high by an internal pull-up when not driven.
R6	TDo	**Test Serial Data Out (3.3 V Tolerant Tri-state Output)**. JTAG serial data is output on this pin on the falling edge of TCK. This pin is held in high impedance state when JTAG is not enabled.
T6	TCK	**Test Clock (5 V Tolerant Input).** Provides the clock to the JTAG test logic. This pin should be low when JTAG is not enabled.
R7	$\overline{\text{TRST}}$	**Test Reset (3.3 V Input with Internal pull-up).** Asynchronously initializes the JTAG TAP Controller by putting it in the Test-Logic-Reset state. This pin should be pulled low to ensure that the ZL50030 is in normal functional mode.
T5	TMS	**Test Mode Select (5 V-Tolerant Input with Enabled Internal Pull-up)** JTAG signal that controls the state transitions of the TAP controller. This pin is pulled high by an internal pull-up resistor when it is not driven.

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1.0 Device Overview

The ZL50030 can switch up to 4,096 × 2,048 channels while providing a rate conversion capability. It is designed to switch 64 kbps PCM or N X 64 kbps data between the backplane and local switching applications. The device maintains frame integrity in data applications and minimum throughput delay for voice applications on a per-channel basis.

The backplane interface can operate at 8.192 Mbps in CT-Bus mode or 16.384 Mbps in ST-BUS mode and is arranged in 125 µs wide frames that contain 128 or 256 channels respectively. A built-in rate conversion circuit allows users to interface between the backplane and the local interface which operates at 2.048 Mbps, 4.096 Mbps or 8.192 Mbps.

By using Zarlink's message mode capability, the microprocessor can access input and output time slots on a per channel basis. This feature is useful for transferring control and status information for external circuits or other TDM devices.

2.0 Functional Description

A Functional Block Diagram of the ZL50030 is shown in Figure 1 on page 2. It is designed to interface CT-Bus and ST-BUS serial streams from a backplane source and ST-BUS serial streams from a local source.

3.0 Frame Alignment Timing

In the ST-BUS or the CT-Bus mode, the C8_A_io or C8_B_io pin accepts an 8.192 MHz clock for the frame pulse alignment. The FRAME_A_io or FRAME_B_io is the frame pulse signal which goes low at the frame boundary for 122 ns. The frame boundary is defined by the rising edge of the C8_A_io or C8_B_io clock during the low cycle of the frame pulse. Figure 2 shows the CT-Bus timing for the backplane 8.192 Mbps data streams and Figure 3 shows the ST-BUS timing for the 16.384 Mbps backplane data streams.

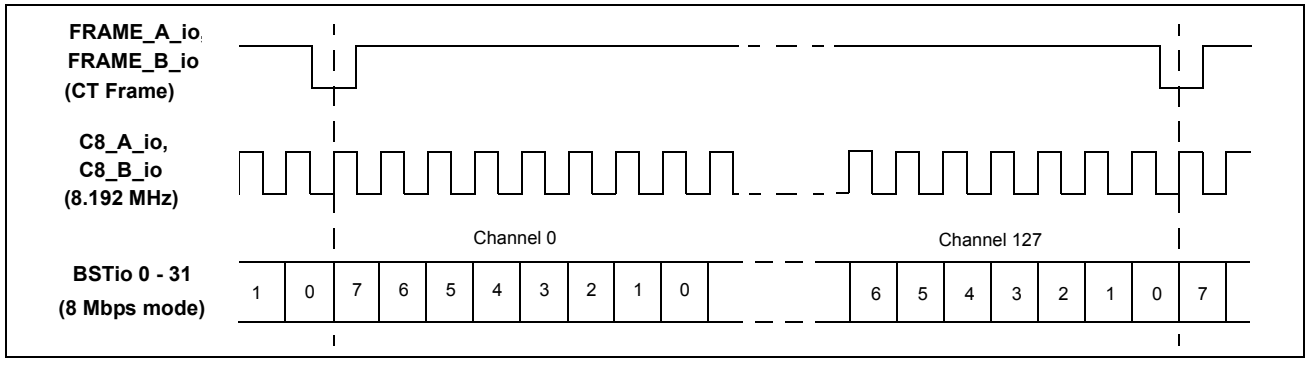

Figure 2 - CT-Bus Timing for 8 Mbps Backplane Data Streams

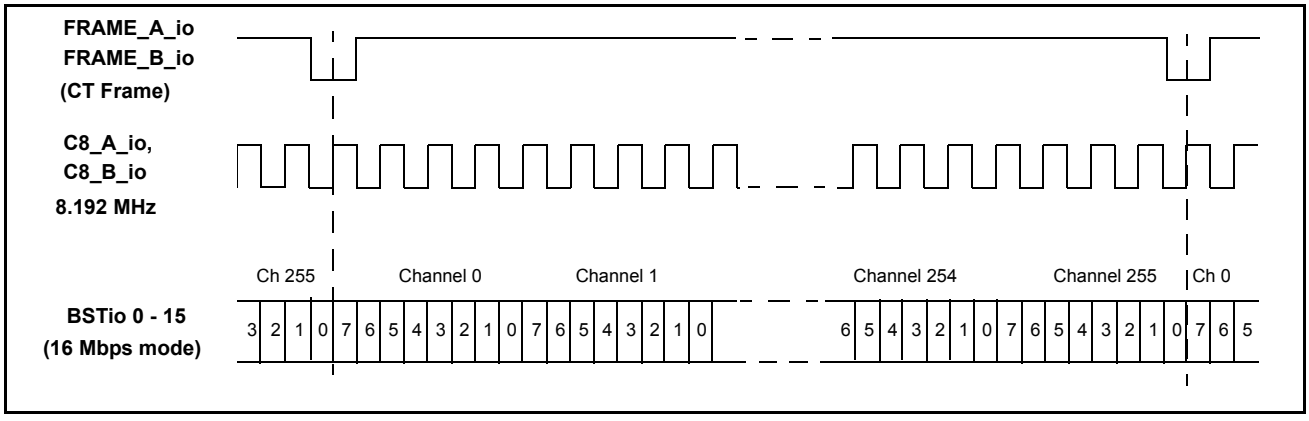

Figure 3 - ST-BUS Timing for 16 Mbps Backplane Data Streams

4.0 Switching Configuration

The device has two operation modes at different data rates for the backplane interface and three operation modes for the local interface. These modes can be programmed via the Device Mode Selection (DMS) register. Mode selections between the backplane and local interfaces are independent.

4.1 Backplane Interface

The backplane interface can be programmed to accept data streams of 8 Mbps or 16 Mbps. When H.110 mode is enabled, BSTio0 to BSTio31 have a data rate of 8.192 Mbps. When ST-BUS mode is enabled, BSTio0 to BSTio15 have a data rate of 16.384 Mbps; BSTio16 to BSTio31are tristated internally and should be connected to ground. Table 1 describes the data rates and mode selections for the backplane interface.

BMS bit of the DMS Register	Modes	Backplane Interface
0	8.192 Mbps	BSTio0 - 31
1	16.384 Mbps	BSTio0 - 15

Table 1 - Mode Selection for Backplane Streams

4.2 Local Interface

The local side of the ZL50030 is divided up into 4 groups. Group 0 contains LSTio0-3, Group 1 contains LSTio4-7, Group 2 contains LSTio8-11 and Group 3 contains LSTio12-15. Each group can be selected to operate in one of three data rates, 2.048 Mbps, 4.094 Mbps and 8.192 Mbps. The per-group data rate is selected through the Device Mode Selection (DMS) register. Streams belonging to the same group have the same operation at the same data rate. See Table 2 on page 15 for a description of the data rates and mode selection for the local ST-BUS interface.

DMS Register Bits		Modes	Usable Streams
LG01	LG00		
0	0	8.192 Mbps	LSTio0 - 3
0	1	4.096 Mbps	
1	0	2.048 Mbps	
1	1	Reserved	

Table 2 - Mode Selection for Local LSTio0 - 3 Streams, Group 0

DMS Register Bits		Modes	Usable Streams
LG11	LG10		
0	0	8.192 Mbps	LSTio4 - 7
0	1	4.096 Mbps	
1	0	2.048 Mbps	
1	1	Reserved	

Table 3 - Mode Selection for Local LSTio4 - 7 Streams, Group 1

DMS Register Bits		Modes	Usable Streams
LG21	LG20		
0	0	8.192 Mbps	LSTio8 - 11
0	1	4.096 Mbps	
1	0	2.048 Mbps	
1	1	Reserved	

Table 4 - Mode Selection for Local LSTio8 - 11 Streams, Group 2

DMS Register Bits		Modes	Usable Streams
LG31	LG30		
0	0	8.192 Mbps	LSTio12-15
0	1	4.096 Mbps	
1	0	2.048 Mbps	
1	1	Reserved	

Table 5 - Mode Selection for Local LSTio12 - 15 Streams, Group 3

5.0 Local Input Delay Selection

The local input delay selection allows individual local input streams to be aligned and shifted against the input frame pulse (FRAME_A_io or FRAME_B_io). This feature compensates for the variable path delays in the local interface. Such delays can occur in large centralized and distributed switching systems.

Each local input stream can have its own bit delay offset value by programming the local input bit delay selection registers (LIDR0 to LIDR5). See Table 11, "Local Input Bit Delay Registers (LIDR0 to LIDR5) Bits" on page 39, for the contents of these registers. Possible bit adjustment can range up to +7 3/4 bit periods forward with resolution of 1/4 bit period. See Table 12 on page 39 and Figure 12 on page 40 for local input delay programming.

6.0 Output Advancement Selection

The ZL50030 allows users to advance individual backplane or local output streams with respect to the frame boundary. This feature is useful in compensating for variable output delays caused by various output loading conditions. Each output stream can have its own advancement value programmed by the output advancement registers. The backplane output advancement registers (BOAR0 to BOAR3) are used to program the backplane output advancement. The local output advancement registers (LOAR0 to LOAR1) are used to program the local output advancement. Possible adjustment for local and backplane output data streams is 22.5 ns with a resolution of 7.5 ns. The advancement is independent of the output data rate. Table 13 on page 41 and Figure 13, "Example of Backplane Output Advancement Timing" on page 41, and Table 14 on page 42 and Figure 14, "Local Output Advancement Timing" on page 42 describe the details of the output advancement programming for the backplane and local interfaces respectively.

7.0 Local Output Timing Considerations

The output data of the ZL50030's local side is slightly advanced with respect to the frame and bit boundary as defined by the local output clocks and frame pulses (ST_FPo0, ST_CKo0, ST_FPo1, ST_CKo1). The advancement is in the range of 5 ns to 17 ns. Despite this advancement, the ZL50030 will operate within the parameters specified in the datasheet because input data are usually sampled at the 3/4 or 1/2 point of the bit cell. However, the user should be cautious when introducing additional delay to the clock signals only (e.g., by passing them through glue logic, FPGA, or CPLD), which will introduce a few nanoseconds of delay relative to the data. If the clock signal is delayed, data will be advanced from the receiver device's point of view. This may cause errors in sampling the data. Using an example where a 3/4 sampling point is used, there is about 30 ns from the sampling point to the end of the bit cell. With a worst-case of 17 ns advancement, the timing margin will be approximately 13 ns. Any additional delays applied to the local output clocks (ST_CKo0 and ST_CKo1) must not exceed 13 ns minus the hold time of the receiving device. Delays applied to both clocks and data equally will not impact the device operation.

8.0 Memory Block Programming

The ZL50030 block programming mode (BPM) register provides users with the capability of initializing the local and backplane connection memories in two frames. Bit 13 - bit 15 of every backplane connection memory location will be programmed with the pattern stored in bit 6 - bit 8 of the BPM register. Bit 13 - bit 15 of every local connection memory location will be programmed with the pattern stored in bits 3 to 5 of the BPM register. The other bit positions of the backplane connection memory and the local connection memory are loaded with zeros. See Figure 4 on page 17 for the connection memory contents when the device is in block programming mode.

The block programming mode is enabled by setting the memory block program (MBP) bit of the Control Register to high. After the block programming enable (BPE) bit of the BPM register is set to high, the block programming data will be loaded into bits 13 to 15 of every backplane connection memory location and bits 13 to 15 of every local connection memory location. The other connection memory bits are loaded with zeros. When the memory block programming is completed, the device resets the BPE bit to low. See Table 10 on page 37 for the bit assignment of the BPM register.

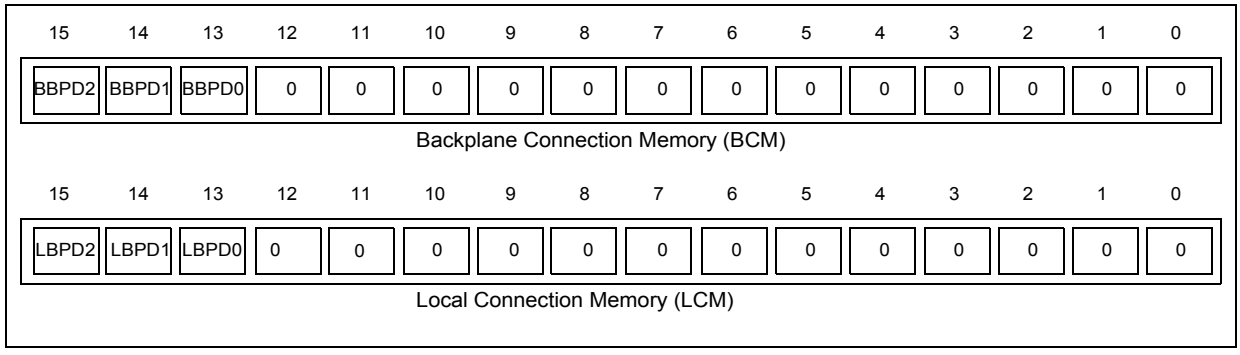

Figure 4 - Block Programming Data in the Connection Memories

9.0 Delay Through the ZL50030

The switching of information from the input serial streams to the output serial streams results in a throughput delay. The device can be programmed to perform time slot interchange functions with different throughput delay capabilities on a per-channel basis. For voice applications it is recommended to select variable throughput delay to ensure minimum delay between input and output data. In wideband data applications it is recommended to select constant throughput delay to maintain the frame integrity of the information through the switch.

The delay through the device varies according to the type of throughput delay selected in the BTM2 - BTM0 bits of the backplane connection memory or LTM0 - LTM2 bits of the local connection memory as described in Table 24 on page 51 and Table 27 on page 53, respectively.

9.1 Variable Delay Mode

The delay in this mode is dependent only on the combination of source and destination channels and is independent of input and output streams. The minimum delays achievable in the ZL50030 device are 3-channel delay, 5-channel delay, and 10-channel delay for the 2 Mbps, 4 Mbps, and 8 Mbps data rates respectively. The maximum delay is one frame plus 3 channels, one frame plus 5 channels, and one frame plus 10 channels for the 2 Mbps, 4 Mbps and 8 Mbps modes respectively.

For the backplane interface, the variable delay mode can be programmed through the backplane connection memory bits, BTM2 - BTM0. When BTM2 - BTM0 are programmed to “000”, it is a per-channel variable delay from local input to the backplane output. When BTM2 - BTM0 are set to “010”, it is a per-channel variable delay from backplane input to backplane output.

For the local interface, the variable delay mode can be programmed through the local connection memory bits, LTM2 - LTM0. When LTM2 - LTM0 are programmed to “000”, it is a per-channel variable delay from local input to local output. When LTM2 - LTM0 are set to “010”, it is a per-channel variable delay from backplane input to local output.

9.2 Constant Delay Mode

In this mode, a multiple page data memory buffer is used to maintain frame integrity in all switching configurations such that a channel written during frame N is always read out during frame N+2.

For the backplane interface, when BTM2 - BTM0 are programmed to “001”, it is a per-channel constant delay mode from local input to backplane output. When BTM2 - BTM0 are set to “011”, it is a per-channel constant delay mode from backplane input to backplane output.

For the local interface, when LTM2 - LTM0 are programmed to “001”, it is a per-channel constant delay mode from local input to local output. When LTM2 - LTM0 are set to “011”, it is a per-channel constant delay mode from backplane input to local output.

10.0 Microprocessor Interface

The ZL50030 provides a parallel microprocessor interface for non-multiplexed bus structures. This interface is compatible with Motorola non-multiplexed bus structures. The required microprocessor signals are the 16-bit data bus (D15-D0), 14-bit address bus (A13-A0) and 4 control lines ($\overline{CS}$, $\overline{DS}$, R/$\overline{W}$ and $\overline{DTA}$). See Figure 37, "Motorola Non-Multiplexed Bus Timing" on page 70 for the Motorola non-multiplexed bus timing.

The ZL50030 microprocessor port provides access to the internal registers, the connection and data memories. All locations provide read/write access except for the Local and Backplane Bit Error Rate registers (LBERR and BBERR) and Data Memory which can only be read by the users.

10.1 $\overline{DTA}$ Data Transfer Acknowledgment Pin

The $\overline{DTA}$ pin of the microprocessor is driven LOW by internal logic to indicate that a data bus transfer is completed. When the bus cycle ends, this pin switches to the high impedance state. An external pull-up of between 1kΩ and 10kΩ is required at this output.

11.0 Address Mapping of Memories and Registers

The address bus on the microprocessor interface selects the internal registers and memories of the ZL50030. If the address bit A13 is low, the registers are addressed by A12 to A0 as shown in Table 6 on page 18.

A13 - A0	Location
0000_H	Control Register, CR
0001_H	Device Mode Selection Register, DMS
0002_H	Block Programming Mode Register, BPM
0003_H	Reserved
0004_H	Local Input Bit Delay Register 0, LIDR0
0005_H	Local Input Bit Delay Register 1, LIDR1
0006_H	Local Input Bit Delay Register 2, LIDR2
0007_H	Local Input Bit Delay Register 3, LIDR3
0008_H	Local Input Bit Delay Register 4, LIDR4
0009_H	Local Input Bit Delay Register 5, LIDR5
$000A_H$ to $001B_H$	Reserved
$001C_H$	Backplane Output Advancement Register 0, BOAR0
$001D_H$	Backplane Output Advancement Register 1, BOAR1
$001E_H$	Backplane Output Advancement Register 2, BOAR2
$001F_H$	Backplane Output Advancement Register 3, BOAR3
0020_H	Local Output Advancement Register 0, LOAR0
0021_H	Local Output Advancement Register 1, LOAR1
0022_H to 0026_H	Reserved

Table 6 - Address Map For Internal Registers (A13 = 0)

A13 - A0	Location
0027_H	Local BER Input Selection Register, LBIS
0028_H	Local BER Register, LBERR
0029_H	Backplane BER Input Selection Register, BBIS
$002A_H$	Backplane BER Register, BBERR
$002B_H$	DPLL Operation Mode Register 1, DOM1
$002C_H$	DPLL Operation Mode Register 2, DOM2
$002D_H$	DPLL Output Adjustment Register, DPOA
$002E_H$	DPLL House Keeping Register, DHKR

Table 6 - Address Map For Internal Registers (A13 = 0) (continued)

If A13 is high, the remaining address input lines are used to select the data and connection memory positions corresponding to the serial input or output data streams as shown in Table 7 on page 20.

The Control register (CR), the Device Mode Selection register (DMS) and the Block Programming Mode register (BPM) control all the major functions of the device. The DMS and BPM should be programmed immediately after system power up to establish the desired switching configuration. The Control register is used to select Data or Connection Memory for microport operations, ST-BUS output frame and clock modes, and to set Memory Block Programing and Bit Error Rate Testing.

The Control register (CR) consists of the memory block programming bit (MBP) and the memory select bits (MS2-0). The memory block programming bit allows users to program the entire connection memory in two frames (see Section 8.0, “Memory Block Programming“ on page 16). The memory select bits control the selection of the connection memories or the data memories. See Table 8 on page 35 for contents of the Control register.

The DMS register consists of the backplane and the local mode selection bits (BMS, LG31 - LG30, LG21 - LG20, LG11 - LG10 and LG01 - LG00) that are used to enable various switching modes for the backplane and the local interfaces respectively. See Table 9 on page 36 for the content of the DMS register.

The BPM register consists of the block programming data bits (LBPD2-0 and BBPD2-0) and the block programming enable bit (BPE). The block programming enable bit allows users to program the entire backplane and local connection memories in two frames (see Section 8.0, “Memory Block Programming“ on page 16). If the ODE pin is low, the backplane CT-Bus is in input mode and the local output drivers are in high impedance state. If the ODE pin is high, all the backplane CT-Bus and local ST-BUS I/O drivers are controlled on a per-channel basis by backplane and local connection memories, respectively. By programming BTM2-0 bits to “110” in the backplane connection memory, the user can control the per-channel input (can be used for high impedance) on the backplane interface. For the local interface, users can program LTM2 -0 bits to “110” in the local connection memory to control the per-channel input (can be used for high impedance). See Table 10 on page 37 for the content of the BPM register.

A13 (Note 1)	Stream Address (ST0-31)						Channel Address (Ch0-255)								
	A12	A11	A10	A9	A8	Stream #	A7	A6	A5	A4	A3	A2	A1	A0	Channel #
1	0	0	0	0	0	Stream 0	0	0	0	0	0	0	0	0	Ch 0
1	0	0	0	0	1	Stream 1	0	0	0	0	0	0	0	1	Ch 1
1	0	0	0	1	0	Stream 2	.	.	.	.	.	.	.	.	.
1	0	0	0	1	1	Stream 3	.	.	.	.	.	.	.	.	.
1	0	0	1	0	0	Stream 4	0	0	0	1	1	1	1	0	Ch 30
1	0	0	1	0	1	Stream 5	0	0	0	1	1	1	1	1	Ch 31 (Note 2)
1	0	0	1	1	0	Stream 6	0	0	1	0	0	0	0	0	Ch 32
1	0	0	1	1	1	Stream 7	0	0	1	0	0	0	0	1	Ch 33
1	0	1	0	0	0	Stream 8	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	0	0	1	1	1	1	1	0	Ch 62
.	0	1.	1	1	1	Stream 15	0	0	1	1	1	1	1	1	Ch 63 (Note 3)
.	.	.	.	.	.	(Note 6).	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	0	1	1	1	1	1	1	0	Ch 126
.	.	.	.	.	.	.	0	1	1	1	1	1	1	1	Ch 127 (Note 4)
1	1	1	0	1	1	Stream 27	.	.	.	.	.	.	.	.	.
1	1	1	1	0	0	Stream 28	.	.	.	.	.	.	.	.	.
1	1	1	1	0	1	Stream 29	.	.	.		.	.	.	.	.
1	1	1	1	1	0	Stream 30	1	1	1	1	1	1	1	0	Ch 254
1	1	1	1	1	1	Stream 31	1	1	1	1	1	1	1	1	Ch 255 (Note 5)

Notes:
1. A13 must be high for access to data and connection memory positions. A13 must be low for access to registers.
2. Channels 0 to 31 are used when serial stream is at 2 Mbps.
3. Channels 0 to 63 are used when serial stream is at 4 Mbps.
4. Channels 0 to 127 are used when serial stream is at 8 Mbps.
5. Channels 0 to 255 are used when serial stream is at 16 Mbps.
6. The local side uses Streams 0 to 15 only while the backplane uses streams 0 to 31.

Table 7 - Address Map for Memory Locations (A13 = 1)

12.0 Backplane Connection Memory

The backplane connection memory controls the switching configuration of the backplane interface. Locations in the backplane connection memory are associated with particular BSTio streams.

The BTM2 - 0 bits of each backplane connection memory entry allow the per-channel selection from message mode, connection mode (constant delay or variable delay), high impedance mode, or bit error rate test mode. The backplane connection memory is also where the BSTio channels are set to be either inputs or outputs. See Table 24 on page 51 for the per-channel control functions.

In the switching mode, the contents of the backplane connection memory stream address bits (BSAB4-0) and channel address bits (BCAB7-0) define the source information (stream and channel) of the time slot that will be switched to the backplane BSTio streams. During message mode, the 8 least significant bits of the backplane connection memory will be transferred to the BSTio pins.

13.0 Local Connection Memory

The local connection memory controls the local interface switching configuration. Locations in the local connection memory are associated with particular LSTio streams.

The LTM2 - 0 bits of each local connection memory entry allow the per-channel selection from message mode, connection mode (constant delay or variable delay), high impedance mode, or bit error rate test mode. The local connection memory is also where the LSTio channels are set to be either inputs or outputs. See Table 27 on page 53 for the per-channel control functions.

In the switching mode, the contents of the local connection memory stream address bits (LSAB4-0) and the channel address bits (LCAB7-0) define the source information (stream and channel) of the time slot that will be switched to the local LSTio streams. During message mode, only the 8 least significant bits of the local connection memory bits are transferred to the LSTio pins.

14.0 Bit Error Rate Test

The ZL50030 offers users a Bit Error Rate (BER) test feature for the backplane and the local interfaces. The circuitry of the BER test consists of a transmitter and a receiver on both interfaces that can transmit and receive the BER patterns independently. The transmitter can output a pseudo-random pattern of the form 2^{15} - 1 to any channel and any stream within a frame. For the test, users can program the output channel and stream through the backplane or local connection memory and the input channel and stream using Local or Backplane BER Input Selection (BIS) registers. See Table 15 on page 43 and Table 17 on page 43 for the LBIS and the BBIS registers contents, respectively.

The receiver receives the BER pattern and does an internal BER pattern comparison. For backplane interface, the comparison result is stored in the Backplane BER register (BBERR). For local interface, the result is stored in the Local BER register (LBERR).

15.0 DPLL

The Digital Phase Locked Loop (DPLL) accepts selectable 2.048 MHz, 1.544 MHz or 8 kHz input reference signals. It accepts reference inputs from independent sources and provides bit-error-free reference switching. The DPLL meets phase slope and MTIE requirements defined by the Telcordia GR-1244-CORE standard.

The DPLL also provides the timing for the rest of the ZL50030 Digital Switch, generating several network clocks with the appropriate quality. Clocks are synchronized to one of two input reference clocks and meet the requirements of the H.110 clock specification.

15.1 ZL50030 Modes of Operation

The DPLL, and consequently the ZL50030, can, as required by the H.110 standard, operate in three different modes: Primary Master, Secondary Master and Slave. See Figure 5, "Typical Timing Control Configuration" on page 22.

To configure the DPLL, there are two Operation Mode registers: DOM1 and DOM2. See Table 19 on page 44 and Table 20 on page 47 for the contents of these registers.

In all modes the ZL50030 monitors both the “A Clocks” (C8_A_io and FRAME_A_io) and the “B Clocks” (C8_B_io and FRAME_B_io). The Fail_A and the Fail_B signals indicate the quality of the “A Clocks” and “B Clocks” respectively.

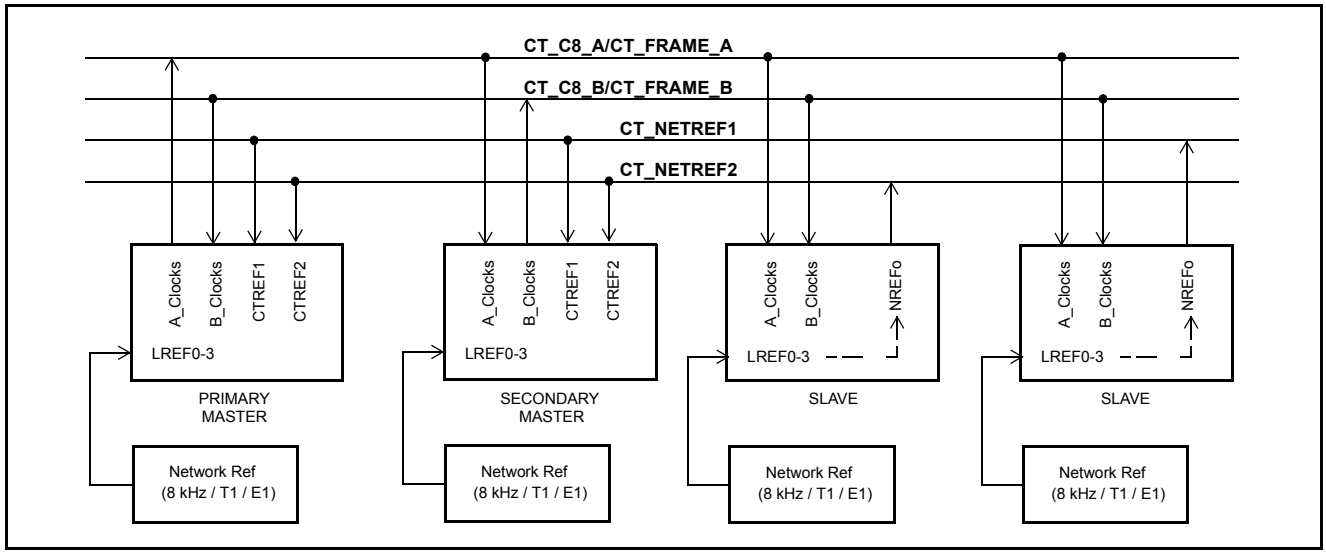

Figure 5 - Typical Timing Control Configuration

15.1.1 Primary Master Mode

In the Primary Master Mode, the ZL50030 drives the “A Clocks” (C8_A_io and FRAME_A_io), by locking to the primary reference (PRI_REF). The PRI_REF can be provided by one of the locally derived network reference sources (LREF0-3), the CTREF1 input or the CTREF2 input. In this mode the ZL50030 has the ability to monitor the primary reference. If the primary reference becomes unreliable, the device continues driving “A Clocks” in stable Holdover Mode until it makes a Stratum 4 Enhanced compatible switch to the secondary reference (SEC_REF) for its network timing. The secondary reference can be provided by one of the local network references (LREF0-3), CTREF1 or CTREF2.

If the primary reference comes back or recovers, the ZL50030 makes a Stratum 4 Enhanced compatible switch back to the original primary reference and the system returns to normal operation state.

If necessary, the ZL50030 can be prevented from switching back to the original primary reference by programming the RPS bit in DOM1 register to give preference to the secondary reference.

While in the Primary Master mode, the ZL50030 attenuates jitter and wander above 1.52 Hz from the selected input reference clock and generates all output clocks according to the DPLL jitter transfer function diagram on Figure 10 on page 31 and Figure 11 on page 32.

For the Primary Master mode selection, see Table 21, "ZL50030 Mode Selection - By Programming DOM1 and DOM2 Registers" on page 49.

15.1.2 Secondary Master Mode

In the Secondary Master Mode, the ZL50030 drives the “B Clocks” (C8_B_io and FRAME_B_io), by locking to the “A Clocks”. As required by the H.110 standard, the “B Clocks” are edge-synchronous with the “A Clocks”, as long as jitter on the “A Clocks” meets Telcordia GR-1244-CORE specifications.

If the “A Clocks” become unreliable, system software is notified and the ZL50030 continues driving the “B Clocks” in stable Holdover Mode until it makes a Stratum 4 Enhanced compatible switch to the secondary reference (SEC_REF) for its network timing. The secondary reference can be a local network reference (LREF0-3), CTREF1 or CTREF2. If the “A Clocks” cannot recover, the designated secondary master can be promoted to primary master by system software. This promotion will cause the “B Clocks” to assume the role of the “A Clocks”.

For the Secondary Master mode selection, see Table 21, "ZL50030 Mode Selection - By Programming DOM1 and DOM2 Registers" on page 49.

15.1.3 Slave Mode

In the Slave Mode, the ZL50030 is phase locked to the “A Clocks”. If the “A Clocks” become unreliable, the device goes to stable Holdover Mode until it makes a Stratum 4 Enhanced compatible switch to the “B Clocks”. The ZL50030 will perform all required functionality as long as the “A Clocks” and the “B Clocks” conform to the Telcordia GR-1244-CORE jitter specifications.

In addition, the device can be used to generate a NREFo reference from its network references, LREF0-3. In most systems NREFo is connected to either CT_REF1 or CT_REF2.

While the device is in Slave Mode and the “A Clocks” or the “B Clocks” do not recover, the designated slave can be promoted to secondary master by system software. In that case, the network reference can be used as the secondary reference.

Table 21 on page 49 shows how to program the DOM1 and DOM2 registers to enable the Slave Mode of the ZL50030.

16.0 DPLL Functional Description

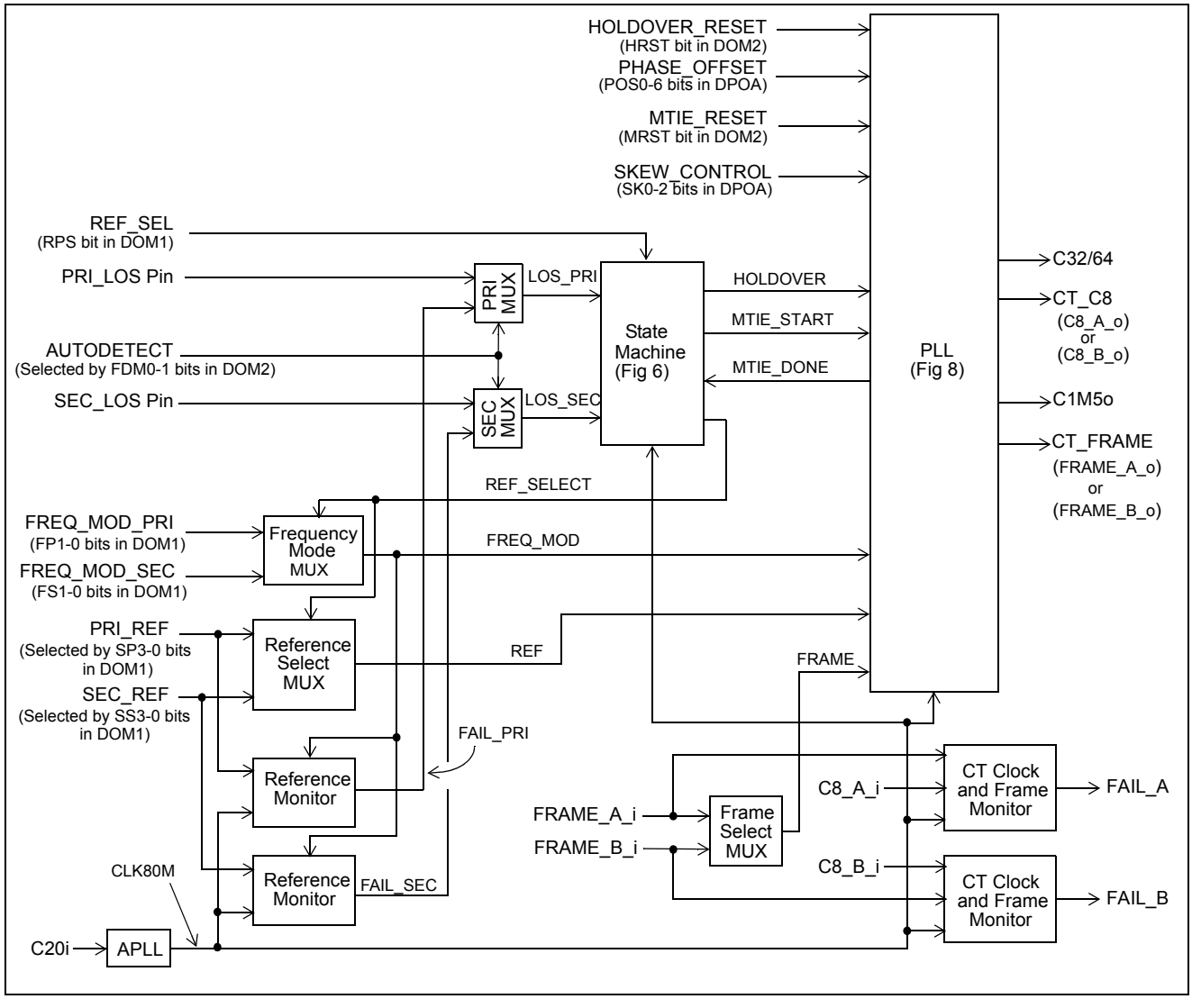

Figure 6 - DPLL Functional Block Diagram

16.1 Reference Select and Frequency Mode MUX Circuits

The DPLL accepts two simultaneous reference input signals and operates on their rising edges. Either the primary reference (PRI_REF) signal or the secondary reference (SEC_REF) signal can be selected to be the reference signal (REF) to the PLL circuit. The appropriate frequency mode input (either FREQ_MOD_PRI or FREQ_MOD_SEC) is selected to be the input of the PLL circuit. The selection is done by the State Machine Circuit based on the current state.

The FREQ_MOD_PRI and the FREQ_MOD_SEC are 2-bit wide inputs which reflect the value in the FP1-0 and FS1-0 bits of the DOM1 register. The primary and the secondary references operate independently from each other and can have different frequencies. Switching the reference from one frequency to another does not require the device reset to be applied. Table 19 on page 44 shows input frequency selection for the primary and secondary reference respectively.

16.2 PRI and SEC MUX Circuits

The DPLL has four different modes to handle reference failure. These modes are selected by the FDM0 and FDM1 bits of the DOM2 Register. If FDM1-0 is ’10’ then the Primary reference is always used regardless of failures. If FDM1-0 is ’11’ then the Secondary reference is always used regardless of failures. Otherwise the DPLL operates in one of two failure detection modes: Autodetect or Manual detection mode. When the FDM0 and FDM1 bits are set to low in the DOM2 register (‘00’), the DPLL is in the Autodetect Mode. In this mode, the outputs from the Reference Monitor Circuits LOS_PRI and LOS_SEC are used by the State Machine Circuit. When the FDM0 bit is set to high and FDM1 bit is set to low (‘01’), the DPLL is in the Manual Detection Mode and the LOS_PRI and LOS_SEC signals are selected from the PRI_LOS and SEC_LOS input pins to be used by the State Machine Circuit. See Table 20 on page 47 for selection of the Failure Detection Modes.

16.3 Frame Select MUX

When the “A Clocks” or the “B Clocks” are selected as the input reference, an 8.192 MHz clock (either C8_A_io or C8_B_io) is provided to be the input reference to the PLL circuit. Because the output frame pulse (CT_FRAME) must be aligned with the selected input frame pulse, the appropriate frame pulse (either FRAME_A_io or FRAME_B_io) is selected in the Frame Select MUX circuit to be the input of the PLL circuit.

16.4 CT Clock and Frame Monitor Circuits

The CT Clock and Frame Monitor circuits check the period of the C8_A_io and the C8_B_io clocks and the FRAME_A_io and FRAME_B_io frame pulses. According to the H.110 specification, the C8 period is 122 ns with a tolerance of +/-35 ns measured between rising edges. If C8 falls outside the range of [87 ns, 157 ns], the clock is rejected and the fail signal (FAIL_A or FAIL_B) becomes high. The Frame pulse period is measured with respect to the C8 clock. The frame pulse period must have exactly 1024 C8 cycles. Otherwise, the fail signal (FAIL_A or FAIL_B) becomes high. When the CT BUS clock and frame pulse signals return to normal, the FAIL_A or FAIL_B signal returns to logic low.

16.5 Reference Monitor Circuits

There are two Reference Monitor Circuits: one for the primary reference (PRI_REF) and one for the secondary reference (SEC_REF). These two circuits monitor the selected input reference signals and detect failures by setting up the appropriate fail outputs (FAIL_PRI and FAIL_SEC). These fail signals are used in the Autodetect mode as the LOS_PRI and LOS_SEC signals to indicate when the reference has failed. The method of generating a failure depends on the selected reference.

When the selected reference frequency is 8.192 MHz (“A Clocks” or “B Clocks”), the fail signals are passed through from the CT Clock and Frame Monitor circuit outputs FAIL_A and FAIL_B, and used directly as FAIL_PRI and FAIL_SEC, accordingly.

For all other reference frequencies (8 kHz, 1.544 MHz and 2.048 MHz), the following checks are performed:

- For all references, the “minimum 90 ns” check is done. This is required by the H.110 specifications - both low level and high level of the reference must last for minimum 90 ns each.
- The “period in the specified range” check is done for all references. The length of the period of the selected input reference is checked to verify if it is in the specified range. For the E1 (2.048 MHz clock) or the T1 (1.544 MHz clock) reference, the period of the clock can vary within the range of 1 +/- 1/4 of the defined clock period which is 488 ns for the E1 clock and 648 ns for T1 clock. For the 8 kHz reference, the variation is from 1 +/- 1/32 period.
- If the selected reference is E1 or T1, “64 periods in the specified range” check is done. The selected reference is observed for a long period (64 reference clock cycles) and checked to verify if it is within the specified range - from 62 to 66 clock periods.

These reference signal verifications include a complete loss or a large frequency shift of the selected reference signal. When the reference signal returns to normal, the LOS_PRI and LOS_SEC signals will return to logic low.

16.6 State Machine Circuit

The State Machine handles the reference selection. Depending on REF_SEL and LOS signals (selection between FAIL_PRI and PRI_LOS and between FAIL_SEC and SEC_LOS), the state machine selects PRI_REF or SEC_REF as the current input reference and dictates the PLL Circuit mode: Normal or Holdover Mode. In the Normal Mode, the DPLL output clocks are locked to the selected input reference (PRI_REF or SEC_REF). In the Holdover Mode, the DPLL clocks retain the phase and frequency values they had 32 to 64 ms prior to moving from the Normal to the Holdover Mode. When going from the Holdover to the Normal Mode, the State Machine activates the MTIE circuit and goes through the states MTIE PRI or MTIE SEC to prevent a phase shift of the output clocks during the DPLL reference switch (from PRI_REF to SEC_REF and vice versa). The state diagram is given in Figure 7, "State Machine Diagram" on page 25.

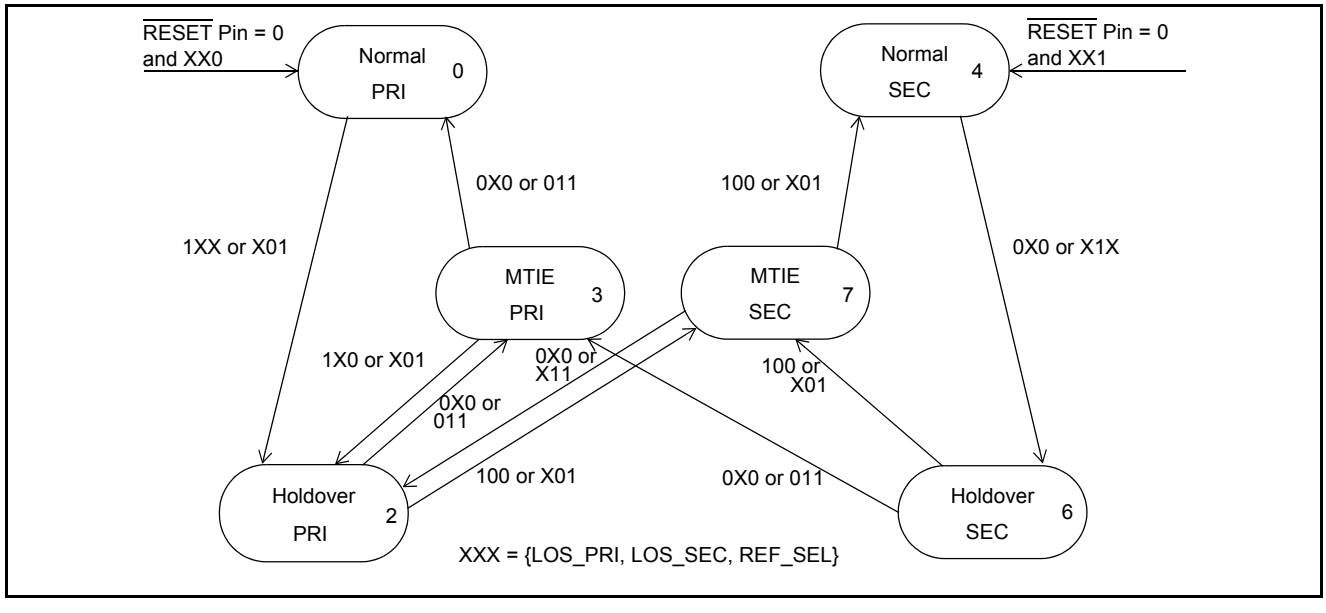

Figure 7 - State Machine Diagram