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ZL50050

8 K-Channel Digital Switch with High Jitter Tolerance, Per Stream Rate Conversion (2, 4, 8, 16, or 32 Mbps), and 32 Inputs and 32 Outputs

Data Sheet

January 2006

Features

- 8,192-channel x 8,192-channel non-blocking unidirectional switching.The Backplane and Local inputs and outputs can be combined to form a non-blocking switching matrix with 32 input streams and 32 output streams
- 4,096-channel x 4,096-channel non-blocking Backplane input to Local output stream switch
- 4,096-channel x 4,096-channel non-blocking Local input to Backplane output stream switch
- 4,096-channel x 4,096-channel non-blocking Backplane input to Backplane output switch
- 4,096-channel x 4,096-channel non-blocking Local input to Local output stream switch
- Rate conversion on all data paths, Backplane-to-Local, Local-to-Backplane, Backplane-to-Backplane and Local-to-Local streams
- Backplane port accepts 16 input and 16 output ST-BUS streams with data rates of 2.048 Mbps, 4.096 Mbps, 8.192 Mbps or 16.384 Mbps in any combination, or a fixed allocation of 8 input and 8 output streams at 32.768 Mbps
- Local port accepts 16 input and 16 output ST-BUS streams with data rates of 2.048 Mbps, 4.096 Mbps, 8.192 Mbps or 16.384 Mbps in any combination, or a fixed allocation of 8 input and 8 output streams at 32.768 Mbps
- Exceptional input clock jitter tolerance (17ns for 16Mbps or lower data rates, 14ns for 32 Mbps)
- Per-stream channel and bit delay for Local and Backplane input streams
- Per-stream advancement for Local and Backplane output streams
- Constant 2-frame throughput delay for frame integrity
- Per-channel high impedance output control for Local and Backplane streams
- Per-channel driven-high output control for Local and Backplane streams

Ordering Information

ZL50050GAC	196 Ball PBGA	Trays
ZL50050GAG2	196 Ball PBGA**	Trays

*Pb Free Tin/Silver/Copper

-40°C to +85°C

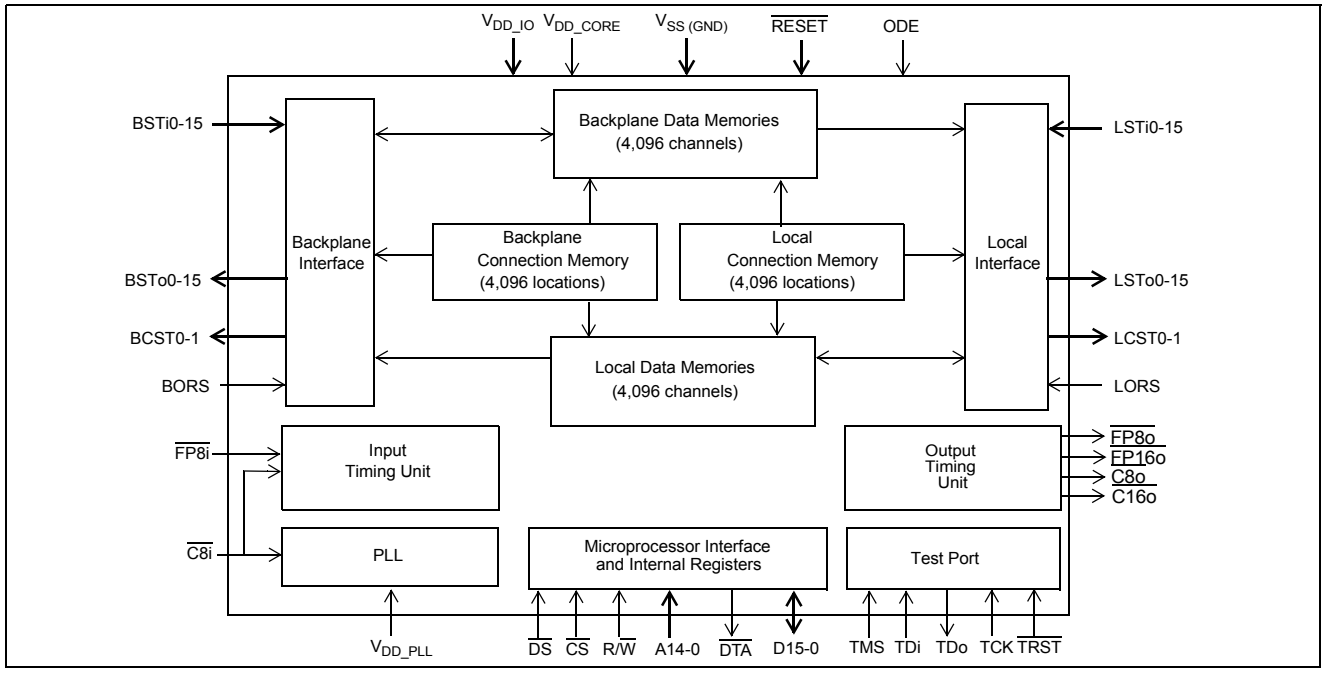

Figure 1 - ZL50050 Functional Block Diagram

- High impedance-control outputs for external drivers on Local and Backplane ports
- Per-channel message mode for Local and Backplane output streams
- Connection memory block programming for fast device initialization
- BER testing for Local and Backplane ports.
- Automatic selection between ST-BUS and GCI-Bus operation
- Non-multiplexed Motorola microprocessor interface
- Conforms to the mandatory requirements of the IEEE-1149.1 (JTAG) standard
- Memory Built-In-Self-Test (BIST), controlled via microprocessor register
- 1.8 V core supply voltage
- 3.3 V I/O supply voltage
- 5 V tolerant inputs, outputs and I/Os
- Pin-to-pin compatible with Zarlink's MT90871 device [1]

Note 1: For software compatibility between ZL50050 and MT90871, please refer to Section 2.6.

Applications

- Central Office Switches (Class 5)
- Media Gateways
- Class-independent switches
- Access Concentrators
- Scalable TDM-Based Architectures
- Digital Loop Carriers

Device Overview

The ZL50050 has two data ports, the Backplane and the Local port. Both the Backplane and Local ports have two independent modes of operation, either 16 input and 16 output streams operated at 2.048 Mbps, 4.096 Mbps, 8.192 Mbps or 16.384 Mbps, in any combination, or 8 input and 8 output streams operated at 32.768 Mbps.

The ZL50050 contains two data memory blocks (Backplane and Local) to provide the following switching path configurations:

- Input-to-Output Unidirectional, supporting 8 K x 8 K switching
- Backplane-to-Local Bi-directional, supporting 4 K x 4 K data switching,
- Local-to-Backplane Bi-directional, supporting 4 K x 4 K data switching,
- Backplane-to-Backplane Bi-directional, supporting 4 K x 4 K data switching.
- Local-to-Local Bi-directional, supporting 4 K x 4 K data switching.

The device contains two connection memory blocks, one for the Backplane output and one for the Local output. Data to be output on the serial streams may come from either of the data memories (Connection Mode) or directly from the connection memory contents (Message Mode).

In Connection Mode, the contents of the connection memory define, for each output stream and channel, the source stream and channel (stored in data memory) to be switched.

In Message Mode, microprocessor data can be written to the connection memory for broadcast on the output streams on a per channel basis. This feature is useful for transferring control and status information to external circuits or other ST-BUS devices.

The device uses a master frame pulse ($\overline{\text{FP8i}}$) and master clock ($\overline{\text{C8i}}$) to define the input frame boundary and timing for both the Backplane port and the Local port. The device will automatically detect whether an ST-BUS or a GCI-Bus style frame pulse is being used. There is a two-frame delay from the time $\overline{\text{RESET}}$ is de-asserted to the establishment of full switch functionality. During this period, the input frame pulse format is determined before switching begins.

The device provides $\overline{\text{FP8o}}$, $\overline{\text{FP16o}}$, $\overline{\text{C8o}}$ and $\overline{\text{C16o}}$ outputs to support external devices connected to the outputs of the Backplane and Local ports.

A non-multiplexed Motorola microprocessor port allows programming of the various device operation modes and switching configurations. The microprocessor port provides access for Register read/write, Connection Memory read/write and Data Memory read-only operations. The port has a 15-bit address bus, 16-bit data bus and 4 control signals. The microprocessor may monitor channel data in the Backplane and Local data memories.

The mandatory requirements of the IEEE-1149.1 (JTAG) standard are fully supported via a dedicated test port.

The ZL50050 is available in one package:

- a 15 mm x 15 mm body, 1mm ball-pitch, 196-PBGA.

Table of Contents

Table of Contents

List of Figures

List of Tables

List of Tables

Pinout Diagram: (as viewed through top of package)

A1 corner identified by metallized marking, mold indent, ink dot, or right-angled corner.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	BSTo1	BSTo2	A4	A5	A8	A9	A12	A13	R/W	$\overline{CS}$	TMS	TDo	BCSTo0	$\overline{TRST}$
B	A0	BSTo5	BSTo0	A1	A2	A7	A11	A14	ODE	TDi	TCK	LCSTo1	LSTo0	LSTo1
C	IC_GND	BSTo7	BSTo8	BSTo3	BSTo4	A6	A10	$\overline{DS}$	$\overline{RESET}$	BCSTo1	IC_GND	LCSTo0	IC_GND	LSTo3
D	IC_GND	BSTo6	BSTo10	GND	A3	VDD_IO	VDD_IO	VDD_IO	$\overline{DTA}$	VDD_IO	GND	LSTo4	LSTo6	LSTo2
E	BSTo12	BSTo11	BSTo13	VDD_IO	GND	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	GND	VDD_IO	LSTo8	LSTo7	LSTo5
F	BSTo9	BSTo14	BSTo15	VDD_IO	VDD_CORE	GND	GND	GND	GND	VDD_CORE	VDD_IO	LSTo12	LSTo13	LSTo9
G	BSTi0	BORS	VDD_CORE	VDD_IO	VDD_CORE	GND	GND	GND	GND	VDD_CORE	VDD_IO	LSTo11	LSTo15	LSTo10
H	BSTi1	BSTi2	BSTi3	VDD_IO	VDD_CORE	GND	GND	GND	GND	VDD_CORE	VDD_IO	VDD_CORE	LORS	LSTo14
J	BSTi4	BSTi5	BSTi7	VDD_IO	VDD_CORE	GND	GND	GND	GND	VDD_CORE	VDD_IO	LSTi5	LSTi1	LSTi2
K	BSTi6	BSTi9	BSTi13	VDD_IO	GND	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	GND	VDD_IO	LSTi15	LSTi3	LSTi0
L	BSTi8	BSTi11	BSTi14	GND	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	GND	LSTi14	LSTi8	LSTi6
M	BSTi10	BSTi15	D15	D14	D12	D5	IC_GND	IC_GND	$\overline{C16o}$	$\overline{FP8i}$	LSTi13	LSTi10	LSTi7	LSTi4
N	BSTi12	D13	D10	D11	D7	D3	D0	IC_GND	VDD_PLL	$\overline{C8o}$	$\overline{FP8o}$	LSTi11	LSTi12	LSTi9
P	GND	D9	D8	D6	D4	D2	D1	IC_GND	IC_OPEN	$\overline{C8i}$	IC_OPEN	$\overline{FP16o}$	GND	GND

Figure 2 - ZL50050 PBGA Connections (196 PBGA, 15 mm x 15 mm) Pin Diagram
(as viewed through top of package)

Pin Description

Pin Name	ZL50050 Package Coordinates (196-ball PBGA)	Description
Device Timing		
C8i	P10	**Master Clock (5 V Tolerant Schmitt-Triggered Input).** This pin accepts an 8.192 MHz clock. The internal frame boundary is aligned with the clock falling or rising edge, as controlled by the C8IPOL bit in the Control Register. Input data on both the Backplane and Local sides (BSTi0-15 and LSTi0-15) must be aligned to this clock and the accompanying input frame pulse, FP8i.
FP8i	M10	**Frame Pulse Input (5 V Tolerant Schmitt-Triggered Input)**. When the Frame Pulse Width bit (FPW) of the Control Register is LOW (default), this pin accepts a 122 ns-wide frame pulse. When the FPW bit is HIGH, this pin accepts a 244 ns-wide frame pulse. The device will automatically detect whether an ST-BUS or GCI-Bus style frame pulse is applied. Input data on both the Backplane and Local sides (BSTi0-15 and LSTi0-15) must be aligned to this frame pulse and the accompanying input clock, C8i.
C8o	N10	**C8o Output Clock (5 V Tolerant Three-state Output).** This pin outputs an 8.192 MHz clock generated within the device. The clock falling edge or rising edge is aligned with the output frame boundary presented on FP8o; this edge polarity alignment is controlled by the COPOL bit of the Control Register. Output data on both the Backplane and Local sides (BSTo0-15 and LSTo0-15) will be aligned to this clock and the accompanying output frame pulse, FP8o.
FP8o	N11	**Frame Pulse Output (5 V Tolerant Three-state Output).** When the Frame Pulse Width bit (FPW) of the Control Register is LOW (default), this pin outputs a 122ns-wide frame pulse. When the FPW bit is HIGH, this pin outputs a 244 ns-wide frame pulse. The frame pulse, running at 8 kHz rate, will have the same format (ST-BUS or GCI-Bus) as the input frame pulse (FP8i). Output data on both the Backplane and Local sides (BSTo0-15 and LSTo0-15) will be aligned to this frame pulse and the accompanying output clock, C8o.
C16o	M9	**C16o Output Clock (5 V Tolerant Three-state Output).** This pin outputs a 16.384 MHz clock generated within the device. The clock falling edge or rising edge is aligned with the output frame boundary presented on FP16o; this edge polarity alignment is controlled by the COPOL bit of the Control Register. Output data on both the Backplane and Local sides (BSTo0-15 and LSTo0-15) will be aligned to this clock and the accompanying output frame pulse, FP16o.
FP16o	P12	**Frame Pulse Output (5 V Tolerant Three-state Output).** When the Frame Pulse Width bit (FPW) of the Control Register is LOW (default), this pin outputs a 61 ns-wide frame pulse. When the FPW bit is HIGH, this pin outputs a 122 ns-wide frame pulse. The frame pulse, running at 8 kHz rate, will have the same format (ST-BUS or GCI-Bus) as the input frame pulse (FP8i). Output data on both the Backplane and Local sides (BSTo0-15 and LSTo0-15) will be aligned to this frame pulse and the accompanying output clock, C16o.

Pin Description (continued)

Pin Name	ZL50050 Package Coordinates (196-ball PBGA)	Description
Backplane and Local Inputs		
BSTi0-7	G1, H1, H2, H3, J1, J2, K1, J3	Backplane Serial Input Streams 0 to 7 (5 V Tolerant Inputs with Internal Pull-downs). In Backplane Non-32 Mbps Mode, these pins accept serial TDM data streams at a data rate of: 16.384 Mbps (with 256 channels per stream), 8.192 Mbps (with 128 channels per stream), 4.096 Mbps (with 64 channels per stream) or 2.048 Mbps (with 32 channels per stream). The data rate is independently programmable for each input stream. In Backplane 32 Mbps Mode, these pins accept serial TDM data streams at a fixed data rate of 32.768 Mbps (with 512 channels per stream).
BSTi8-15	L1, K2, M1, L2, N1, K3, L3, M2	**Backplane Serial Input Streams 8 to 15 (5 V Tolerant Inputs with Internal Pull-downs).** In Backplane Non-32 Mbps Mode, these pins accept serial TDM data streams at a data rate of: 16.384 Mbps (with 256 channels per stream), 8.192 Mbps (with 128 channels per stream), 4.096 Mbps (with 64 channels per stream) or 2.048 Mbps (with 32 channels per stream). The data rate is independently programmable for each input stream. In Backplane 32 Mbps Mode, these pins are unused and should be externally connected to a defined logic level.
LSTi0-7	K14, J13, J14, K13, M14, J12, L14, M13	**Local Serial Input Streams 0 to 7 (5 V Tolerant Inputs with Internal Pull-downs).** In Local Non-32 Mbps Mode, these pins accept serial TDM data streams at a data rate of: 16.384 Mbps (with 256 channels per stream), 8.192 Mbps (with 128 channels per stream), 4.096 Mbps (with 64 channels per stream) or 2.048 Mbps (with 32 channels per stream). The data rate is independently programmable for each input stream. In Local 32 Mbps Mode, these pins accept serial TDM data streams at a fixed data rate of 32.768 Mbps (with 512 channels per stream).

Pin Description (continued)

Pin Name	ZL50050 Package Coordinates (196-ball PBGA)	Description
LSTi8-15	L13, N14, M12, N12, N13, M11, L12, K12	**Local Serial Input Streams 8 to 15 (5 V Tolerant Inputs with Internal Pull-downs).** In Local Non-32 Mbps Mode, these pins accept serial TDM data streams at a data rate of: 16.384 Mbps (with 256 channels per stream), 8.192 Mbps (with 128 channels per stream), 4.096 Mbps (with 64 channels per stream) or 2.048 Mbps (with 32 channels per stream). The data rate is independently programmable for each input stream. In Local 32 Mbps Mode, these pins are unused and should be externally connected to a defined logic level.
Backplane and Local Outputs and Control		
ODE	B9	**Output Drive Enable (5 V Tolerant Input with Internal Pull-up)**. An asynchronous input providing Output Enable control to the BSTo0-15, LSTo0-15, BCSTo0-1, and LCSTo0-1 outputs. When LOW, the BSTo0-15 and LSTo0-15 outputs are driven HIGH or high impedance (dependent on the **BORS** and **LORS** pin settings respectively) and the outputs BCSTo0-1 and LCSTo0-1 are driven low. When HIGH, the outputs BSTo0-15, LSTo0-15, BCSTo0-1, and LCSTo0-1 are enabled.
BORS	G2	**Backplane Output Reset State (5 V Tolerant Input with Internal Pull-down)**. When this input is LOW, the device will initialize with the BSTo0-15 outputs driven high, and the BCSTo0-1 outputs driven low. Following initialization, the Backplane stream outputs are always active and a high impedance state, if required on a per-channel basis, may be implemented with external buffers controlled by outputs BCSTo0-1. When this input is HIGH, the device will initialize with the BSTo0-15 outputs at high impedance and the BCSTo0-1 outputs driven low. Following initialization, the Backplane stream outputs may be set active or high impedance using the **ODE** pin or on a per-channel basis with the **BE** bit in the Backplane Connection Memory.

Pin Description (continued)

Pin Name	ZL50050 Package Coordinates (196-ball PBGA)	Description
BSTo0-7	B3, A1, A2, C4, C5, B2, D2, C2	**Backplane Serial Output Streams 0 to 7 (5 V Tolerant, Three-state Outputs with Slew-Rate Control).** In Backplane Non-32 Mbps Mode, these pins output serial TDM data streams at a data rate of: 16.384 Mbps (with 256 channels per stream), 8.192 Mbps (with 128 channels per stream), 4.096 Mbps (with 64 channels per stream) or 2.048 Mbps (with 32 channels per stream). The data rate is independently programmable for each output stream. In Backplane 32 Mbps Mode, these pins output serial TDM data streams at a fixed data rate of 32.768 Mbps (with 512 channels per stream). Refer to the descriptions of the **BORS** and **ODE** pins for control of the output HIGH or high impedance state.
BSTo8-15	C3, F1, D3, E2, E1, E3, F2, F3	**Backplane Serial Output Streams 8 to 15 (5 V Tolerant, Three-state Outputs with Slew-Rate Control).** In Backplane Non-32 Mbps Mode, these pins output serial TDM data streams at a data rate of: 16.384 Mbps (with 256 channels per stream), 8.192 Mbps (with 128 channels per stream), 4.096 Mbps (with 64 channels per stream) or 2.048 Mbps (with 32 channels per stream). The data rate is independently programmable for each output stream. These pins are unused when the Backplane 32 Mbps Mode is selected. Therefore, the value output on these pins during Backplane 32 Mbps Mode (either driven-HIGH or high impedance) is dependent on the configuration of the BORS pin. Refer to the descriptions of the **BORS** and **ODE** pins for control of the output HIGH or high impedance state.
BCSTo0-1	A13, C10	**Backplane Output Channel High-Impedance Control (5 V Tolerant, Three-state Outputs).** These pins control external buffering individually for a set of Backplane output streams on a per-channel basis. When LOW, the external output buffer will be tri-stated. When HIGH, the external output buffer will be enabled. In Backplane Non-32 Mbps Mode (stream rates 2 Mbps to 16 Mbps): BCSTo0 is the output enable for BSTo0,2,4,6,8,10,12,14 BCSTo1 is the output enable for BSTo1,3,5,7,9,11,13,15 In Backplane 32 Mbps Mode (stream rate 32 Mbps): BCSTo0 is the output enable for BSTo0,2,4,6 BCSTo1 is the output enable for BSTo1,3,5,7 Refer to the descriptions of the **BORS** and **ODE** pins for control of the output LOW or active state.

Pin Description (continued)

Pin Name	ZL50050 Package Coordinates (196-ball PBGA)	Description
LORS	H13	**Local Output Reset State (5 V Tolerant Input with Internal Pull-down)**. When this input is LOW, the device will initialize with the LSTo0-15 outputs driven high, and the LCSTo0-1 outputs driven low. Following initialization, the Local stream outputs are always active and a high impedance state, if required on a per-channel basis, may be implemented with external buffers controlled by outputs LCSTo0-1. When this input is HIGH, the device will initialize with the LSTo0-15 outputs at high impedance and the LCSTo0-1 outputs driven low. Following initialization, the Local stream outputs may be set active or high impedance using the **ODE** pin or on a per-channel basis with the **LE** bit in the Local Connection Memory.
LSTo0-7	B13, B14, D14, C14, D12, E14, D13, E13	**Local Serial Output Streams 0 to 7 (5 V Tolerant Three-state Outputs with Slew-Rate Control).** In Local Non-32 Mbps Mode, these pins output serial TDM data streams at a data rate of: 16.384 Mbps (with 256 channels per stream), 8.192 Mbps (with 128 channels per stream), 4.096 Mbps (with 64 channels per stream) or 2.048 Mbps (with 32 channels per stream). The data rate is independently programmable for each output stream. In Local 32 Mbps Mode, these pins output serial TDM data streams at a fixed data rate of 32.768 Mbps (with 512 channels per stream). Refer to the descriptions of the **LORS** and **ODE** pins for control of the output HIGH or high impedance state.
LSTo8-15	E12, F14, G14, G12, F12, F13, H14, G13	**Local Serial Output Streams 8 to 15 (5 V Tolerant Three-state Outputs with Slew-Rate Control).** In Local Non-32 Mbps Mode, these pins output serial TDM data streams at a data rate of: 16.384 Mbps (with 256 channels per stream), 8.192 Mbps (with 128 channels per stream), 4.096 Mbps (with 64 channels per stream) or 2.048 Mbps (with 32 channels per stream). The data rate is independently programmable for each output stream. These pins are unused when the Local 32 Mbps Mode is selected. Therefore, the value output on these pins during Local 32 Mbps Mode (either driven-HIGH or high impedance) is dependent on the configuration of the LORS pin. Refer to the descriptions of the **LORS** and **ODE** pins for control of the output HIGH or high impedance state.

Pin Description (continued)

Pin Name	ZL50050 Package Coordinates (196-ball PBGA)	Description
LCSTo0-1	C12, B12	**Local Output Channel High-Impedance Control (5 V Tolerant Three-state Outputs).** These pins control external buffering individually for a set of Local output streams on a per-channel basis. When LOW, the external output buffer will be tri-stated. When HIGH, the external output buffer will be enabled. In Local Non-32 Mbps Mode (stream rate 2 Mbps to 16 Mbps): LCSTo0 is the output enable for LSTo0,2,4,6,8,10,12,14 LCSTo1 is the output enable for LSTo1,3,5,7,9,11,13,15 In Local 32 Mbps Mode (stream rate 32 Mbps): LCSTo0 is the output enable for LSTo0,2,4,8 LCSTo1 is the output enable for LSTo1,3,5,7 Refer to descriptions of the **LORS** and **ODE** pins for control of the output LOW or active state.
Microprocessor Port Signals		
A0 - A14	B1, B4, B5, D5, A3, A4, C6, B6, A5, A6, C7, B7, A7, A8, B8	**Address 0 - 14 (5 V Tolerant Inputs).** These pins form the 15-bit address bus to the internal memories and registers. A0 = LSB
D0 - D15	N7, P7, P6, N6, P5, M6, P4, N5, P3, P2, N3, N4, M5, N2, M4, M3	**Data Bus 0 - 15 (5 V Tolerant Inputs/Outputs with Slew-Rate Control).** These pins form the 16-bit data bus of the microprocessor port. D0 = LSB
$\overline{CS}$	A10	**Chip Select (5 V Tolerant Input).** Active LOW input used by the microprocessor to enable the microprocessor port access. **Note that a minimum of 30 ns must separate the de-assertion of DTA (to high) and the assertion of CS and/or DS to initiate the next access.**
$\overline{DS}$	C8	**Data Strobe (5 V Tolerant Input).** This active LOW input works in conjunction with $\overline{CS}$ to enable the microprocessor port read and write operations. **Note that a minimum of 30 ns must separate the de-assertion of DTA (to high) and the assertion of CS and/or DS to initiate the next access.**
R/$\overline{W}$	A9	**Read/$\overline{Write}$ (5 V Tolerant Input).** This input controls the direction of the data bus lines (D0-D15) during a microprocessor access.
$\overline{DTA}$	D9	**Data Transfer Acknowledgment (5 V Tolerant Three-state Output).** This active LOW output indicates that a data bus transfer is complete. A pull-up resistor is required to hold a HIGH level. **Note that a minimum of 30 ns must separate the de-assertion of DTA (to high) and the assertion of CS and/or DS to initiate the next access.**

Pin Description (continued)

Pin Name	ZL50050 Package Coordinates (196-ball PBGA)	Description
$\overline{\text{RESET}}$	C9	**Device Reset (5 V Tolerant Input with Internal Pull-up).** This input (active LOW) asynchronously applies reset and synchronously releases reset to the device. In the reset state, the outputs LSTo0-15 and BSTo0-15 are set to a HIGH or high impedance state, depending on the state of the LORS and BORS external control pins, respectively. The assertion of $\overline{\text{RESET}}$ causes the LCSTo0-1 and BCSTo0-1 pins to be driven LOW (refer to Table 2). The assertion of this pin also clears the device registers and internal counters. **Refer to Section 8.3 on page 44 for the timing requirements regarding this reset signal**.
JTAG Control Signals		
TCK	B11	**Test Clock (5 V Tolerant Input).** Provides the clock to the JTAG test logic.
TMS	A11	**Test Mode Select (5 V Tolerant Input with Internal Pull-up).** JTAG signal that controls the state transitions of the TAP controller.
TDi	B10	**Test Serial Data In (5 V Tolerant Input with Internal Pull-up).** JTAG serial test instructions and data are shifted in on this pin.
TDo	A12	**Test Serial Data Out (5 V Tolerant Three-state Output).** JTAG serial data is output on this pin on the falling edge of TCK. This pin is held in a high impedance state when JTAG is not enabled.
$\overline{\text{TRST}}$	A14	**Test Reset (5 V Tolerant Input with Internal Pull-up).** Asynchronously initializes the JTAG TAP controller to the Test-Logic-Reset state. This pin must be pulsed LOW during power-up for JTAG testing. This pin must be held LOW for normal functional operation of the device.
Power and Ground Pins		
V_{DD_IO}	D6, D7, D8, D10, E4, E11, F4, F11, G4, G11, H4, H11, J4, J11, K4, K11, L5, L6, L7, L8, L9, L10	**Power Supply for Periphery Circuits:** +3.3 V
V_{DD_CORE}	E6, E7, E8, E9, F5, F10, G3, G5, G10, H5, H10, H12, J5, J10, K6, K7, K8, K9	**Power Supply for Core Circuits:** +1.8 V
V_{DD_PLL}	N9	**Power Supply for Analog PLL:** +1.8 V

Pin Description (continued)

Pin Name	ZL50050 Package Coordinates (196-ball PBGA)	Description
V_{SS} (GND)	D4, D11, E5, E10, F6, F7, F8, F9, G6, G7, G8, G9, H6, H7, H8, H9, J6, J7, J8, J9, K5, K10, L4, L11, P1, P13, P14	Ground.
Unused Pins		
IC_OPEN	P9, P11	**Internal Connections - OPEN.** These pins must be left unconnected.
IC_GND	C1, C11, C13, D1, M7, M8, N8, P8	**Internal Connections - GND.** These pins must be tied LOW.

1.0 Unidirectional and Bi-directional Switching Applications

The ZL50050 has a maximum capacity of 8,192 input channels and 8,192 output channels. This is calculated from the maximum number of streams and channels: 32 input streams (16 Backplane, 16 Local) at 16.384 Mbps and 32 output streams (16 Backplane, 16 Local) at 16.384 Mbps.

A typical mode of operation is to separate the input and output streams to form a unidirectional switch, as shown in Figure 3 below.

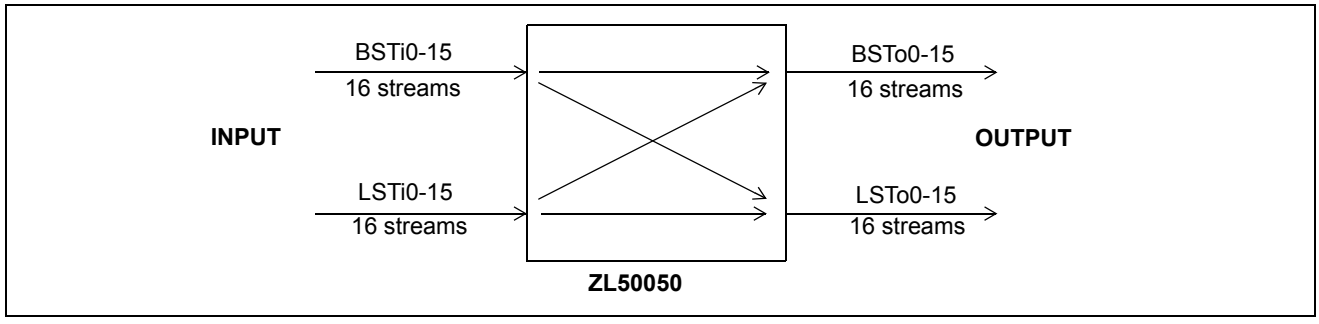

Figure 3 - 8,192 x 8,192 Channels (16 Mbps), Unidirectional Switching

In this system, the Backplane and Local input streams are combined, and the Backplane and Local output streams are combined, so that the switch appears as a 32 input stream by 32 output stream switch. This gives the maximum 8,192 x 8,192 channel capacity.

Often a system design needs to differentiate between a Backplane and a Local side, or it needs to put the switch in a bi-directional configuration. In this case, the ZL50050 can be used as shown in Figure 4 to give 4,096 x 4,096 channel bi-directional capacity.

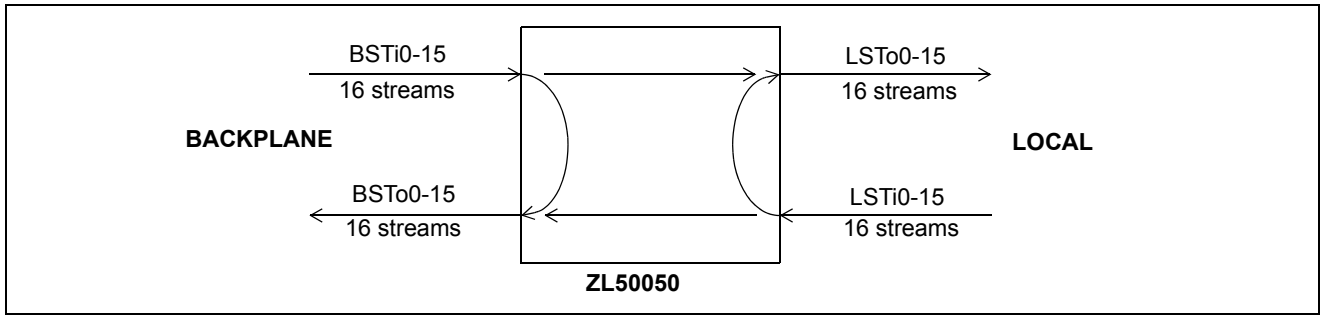

Figure 4 - 4,096 x 4,096 Channels (16 Mbps), Bi-directional Switching

In this system setup, the chip has a capacity of 4,096 input channels and 4,096 output channels on the Backplane side, as well as 4,096 input channels and 4,096 output channels on the Local side. Note that some or all of the output channels on one side can come from the other side, e.g., Backplane input to Local output switching.

Note that in either configuration, the Backplane port can be operated in the Backplane 32 Mbps Mode, providing 512 channels on each of the 8 available input and output streams (BSTi0-7 and BSTo0-7) operating at a data rate of 32.768 Mbps, in conjunction with the Local streams (LSTi0-15 and LSTo0-15) operating at 16.384 Mbps (Local Non-32 Mbps Mode) or in conjunction with the Local streams (LSTi0-7 and LSTo0-7) operating at 32.768 Mbps (Local 32 Mbps Mode). Similarly, the Local port can be operated in the Local 32 Mbps Mode, providing 512 channels on each of the 8 available input and output streams (LSTi0-7 and LSTo0-7) operating at a data rate of 32.768 Mbps, in conjunction with the Backplane streams (BSTi0-15 and BSTo0-15) operating at 16.384 Mbps (Backplane Non-32 Mbps Mode) or in conjunction with the Backplane streams (BSTi0-7 and BSTo0-7) operating at 32.768 Mbps (Backplane 32 Mbps Mode).

The modes in which one port operates in 32 Mbps Mode while the other port operates in Non-32 Mbps Mode allow data rate conversion between 32.768 Mbps and 16.384 Mbps without loss to the switching capacity.

1.1 Flexible Configuration

The ZL50050 can be configured as an 8 K by 8 K non-blocking unidirectional digital switch, a 4 K by 4 K non-blocking bi-directional digital switch, or as a blocking switch with various switching capacities.

1.1.1 Non-Blocking Unidirectional Configuration (Typical System Configuration)

Because the input and output drivers are synchronous, the user can combine input Backplane streams and input Local streams as well as output Backplane streams and output Local streams to increase the total number of input and output streams of the switch in a unidirectional configuration, as shown in Figure 3.

- 8,192-channel x 8,192-channel non-blocking switching from input to output streams

1.1.2 Non-Blocking Bi-directional Configuration

Another typical application is to configure the ZL50050 as a non-blocking 4 K by 4 K bi-directional switch, as shown in Figure 4:

- 4,096-channel x 4,096-channel non-blocking switching from Backplane input to Local output streams
- 4,096-channel x 4,096-channel non-blocking switching from Local input to Backplane output streams
- 4,096-channel x 4,096-channel non-blocking switching from Backplane input to Backplane output streams
- 4,096-channel x 4,096-channel non-blocking switching from Local input to Local output streams

1.1.3 Blocking Bi-directional Configuration

The ZL50050 can be configured as a blocking bi-directional switch if it is an application requirement. For example, it can be configured as a 6 K by 2 K bi-directional blocking switch, as shown in Figure 5:

- 6,144-channel x 2,048-channel blocking switching from Backplane input to Local output streams
- 2,048-channel x 6,144-channel blocking switching from Local input to Backplane output streams
- 6,144-channel x 6,144-channel non-blocking switching from Backplane input to Backplane output streams
- 2,048-channel x 2,048-channel non-blocking switching from Local input to Local output streams

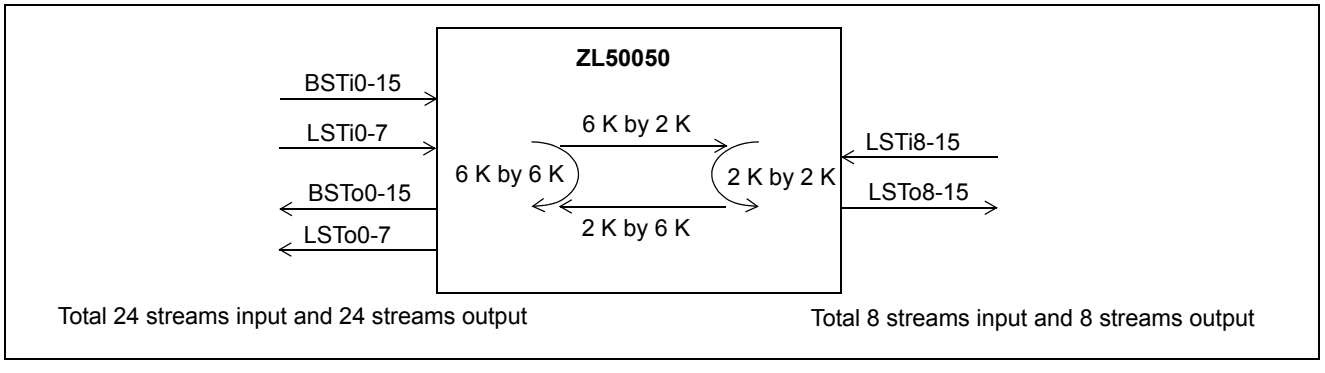

Figure 5 - 6,144 by 2,048 Channels Blocking Bi-directional Configuration

2.0 Functional Description

2.1 Switching Configuration

The device supports five switching configurations: (1) Unidirectional switch, (2) Backplane-to-Local, (3) Local-to-Backplane, (4) Backplane-to-Backplane, and (5) Local-to-Local. The following sections describe the switching paths in detail. Configurations (2) - (5) enable a non-blocking bi-directional switch with 4,096 Backplane input/output channels at Backplane stream data rates of 16.384 Mbps or 32.768 Mbps, and 4,096 Local input/output channels at Local stream data rates of 16.384 Mbps or 32.768 Mbps. The switching paths of configurations (2) to (5) may be operated simultaneously. When the lower data-rates of 8.192, 4.096 and 2.048 Mbps are included, there will be a corresponding reduction in switch capacity although conversion between differing rates will be maintained.

2.1.1 Unidirectional Switch

The device can be configured as a 8,192 x 8,192 unidirectional switch by grouping together all input streams and all output streams. All streams can be operated at a data rate of 16.384 Mbps or 32.768 Mbps, or a combination of 16.384 Mbps and 32.768 Mbps (i.e., one rate on the Local streams and the other rate on the Backplane streams). Lower data rates may be used with a corresponding reduction in switch capacity.

2.1.2 Backplane-to-Local Path

The device can provide data switching between the Backplane input port and the Local output port. The Local Connection Memory determines the switching configurations.

2.1.3 Local-to-Backplane Path

The device can provide data switching between the Local input port and the Backplane output port. The Backplane Connection Memory determines the switching configurations.

2.1.4 Backplane-to-Backplane Path

The device can provide data switching between the Backplane input and output ports. The Backplane Connection Memory determines the switching configurations.

2.1.5 Local-to-Local Path

The device can provide data switching between the Local input and output ports. The Local Connection Memory determines the switching configurations.

2.1.6 Port Data Rate Modes and Selection

The bit rate for each input stream is selected by writing to dedicated input bit rate registers, BIBRR0 to BIBRR15 for Backplane Input Bit Rate Registers (see Table 50) and LIBRR0 to LIBRR15 for Local Input Bit Rate Registers (see Table 46).

The bit rate for each output stream is selected by writing to dedicated output bit rate registers, BOBRR0 to BOBRR15 for Backplane Output Bit Rate Registers (see Table 52) and LOBRR0 to LOBRR15 for Local Output Bit Rate Registers (see Table 48).

If the Backplane 32Mbps Mode is selected by setting the Control Register bit MODE32B HIGH, the settings in BIBRRn and BOBRRn are ignored. Similarly, if the Local 32Mbps Mode is selected by setting the Control Register bit MODE32L HIGH, the settings in LIBRRn and LOBRRn are ignored.

Stream Numbers	Rate Selection Capability (for each individual stream)
Local Input streams - LSTi0-7	2.048, 4.096, 8.192 or 16.384 Mbps in Local Non-32 Mbps Mode. All streams at 32.768 Mbps in Local 32 Mbps Mode.
Local Input streams - LSTi8-15	2.048, 4.096, 8.192 or 16.384 Mbps in Local Non-32 Mbps Mode. Unused in Local 32 Mbps Mode.
Backplane Input streams - BSTi0-7	2.048, 4.096, 8.192 or 16.384 Mbps in Backplane Non-32 Mbps Mode. All streams at 32.768 Mbps in Backplane 32Mbps Mode.
Backplane Input streams - BSTi8-15	2.048, 4.096, 8.192 or 16.384Mbps in Backplane Non-32 Mbps Mode. Unused in Backplane 32 Mbps Mode.
Local Output streams - LSTo0-7	2.048, 4.096, 8.192 or 16.384 Mbps in Local Non-32 Mbps Mode. All streams at 32.768 Mbps in Local 32 Mbps Mode.
Local Output streams - LSTo8-15	2.048, 4.096, 8.192 or 16.384 Mbps in Local Non-32 Mbps Mode. Unused in Local 32 Mbps Mode.
Backplane Output streams - BSTo0-7	2.048, 4.096, 8.192 or 16.384 Mbps in Backplane Non-32 Mbps Mode. All streams at 32.768 Mbps in Backplane 32 Mbps Mode.
Backplane Output streams - BSTo8-15	2.048, 4.096, 8.192 or 16.384 Mbps in Backplane Non-32 Mbps Mode. Unused in Backplane 32 Mbps Mode.

Table 1 - Per-stream Input and Output Data Rate Selection: Backplane and Local, Non-32 Mbps Mode and 32 Mbps Mode

2.1.7 Local Port Rate Selection

The Local port has 16 input (LSTi0-15) and 16 output (LSTo0-15) data streams.

The Local streams can be operated in one of two modes, Local Non-32 Mbps Mode and Local 32 Mbps Mode. The Local stream data rates are not affected by the operating mode of the Backplane port. The operating mode of the Local side is determined by the state of the Control Register bit MODE32L. Setting this bit HIGH will invoke the Local 32 Mbps Mode. Setting the bit LOW will invoke the Non-32 Mbps Mode. The default value of this bit on device reset is LOW. The timing of the input and output clocks and frame pulses is shown in Figure 7, Input and Output (Generated) Frame Pulse Alignment for Different Data Rates.

Local Non-32 Mbps Mode: Each of the Local streams (LSTi0-15 and LSTo0-15) can be independently programmed for a data rate of 2.048 Mbps, 4.096 Mbps, 8.192 Mbps or 16.384 Mbps.

Local 32 Mbps Mode: 8 of the Local input streams (LSTi0-7) and 8 of the Local output streams (LSTo0-7) operate at a fixed rate of 32.768 Mbps. In this mode, the remaining input and output streams are unused.

2.1.7.1 Local Input Port

The input traffic on the Local streams are aligned based on the $\overline{\text{FP8i}}$ and $\overline{\text{C8i}}$ input timing signals. Each input stream, LSTi0-15, can be individually set to operate at 2.048 Mbps, 4.096 Mbps, 8.192 Mbps or 16.384 Mbps by programming the LIBR1-0 bits in the Local Input Bit Rate Register (LIBRR0-15). The Local streams can also be set to operate at 32.768 Mbps. When the MODE32L bit in the Control Register is set high, the first 8 input streams, LSTi0-7, operate at 32.768 Mbps and the remaining 16 streams, LSTi8-15, will not be used and must be connected to a defined logic level.

2.1.7.2 Local Output Port

The output traffic on the Local streams are aligned based on the $\overline{\text{FP8o}}$ and $\overline{\text{C8o}}$ output timing signals. Operation of stream data in Connection Mode or Message Mode is determined by the state of the LMM bit of the Local Connection Memory. The channel high impedance state is controlled by the LE bit of the Local Connection Memory. The data source (i.e., from the Local or Backplane Data Memory) is determined by the LSRC bit of the Local Connection Memory. Refer to Section 9.1, Local Connection Memory, and Section 12.3, Local Connection Memory Bit Definition for more details. Each output stream, LSTo0-15, can be individually set to operate at 2.048 Mbps, 4.096 Mbps, 8.192 Mbps or 16.384 Mbps by programming the LOBR1-0 bits in the Local Output Bit Rate Register (LOBRR0-15). The Local streams can also be set to operate at 32.768 Mbps. When the MODE32L bit in the Control Register is set high, the first 8 output streams, LSTo0-7, operate at 32.768 Mbps and the remaining 8 streams, LSTo8-15, will not be used and must be connected to a defined logic level.

2.1.8 Backplane Port Rate Selection

The Backplane port has 16 input (BSTi0-15) and 16output (BSTo0-15) data streams.

The Backplane streams can be operated in one of two modes, Backplane Non-32 Mbps Mode and Backplane 32 Mbps Mode. The Backplane stream data rates are not affected by the operating mode of the Local port. The operating mode of the Backplane side is determined by the state of the Control Register bit MODE32B. Setting this bit HIGH will invoke the Backplane 32 Mbps Mode. Setting the bit LOW will invoke the Non-32 Mbps Mode. The default value of this bit on device reset is LOW. The timing of the input and output clocks and frame pulses is shown in Figure 7, Input and Output (Generated) Frame Pulse Alignment for Different Data Rates.

Backplane Non-32 Mbps Mode: Each of the Backplane streams (BSTi0-15 and BSTo0-15) can be independently programmed for a data rate of 2.048 Mbps, 4.096 Mbps, 8.192 Mbps or 16.384 Mbps.

Backplane 32 Mbps Mode: 8 of the Backplane input streams (BSTi0-7) and 8 of the Backplane output streams (BSTo0-7) operate at a fixed rate of 32.768 Mbps. In this mode, the remaining input and output streams are unused.

2.1.8.1 Backplane Input Port

The input traffic on the Backplane streams are aligned based on the $\overline{\text{FP8i}}$ and $\overline{\text{C8i}}$ input timing signals. Each input stream, BSTi0-15, can be individually set to operate at 2.048 Mbps, 4.096 Mbps, 8.192 Mbps or 16.384 Mbps by programming the BIBR1-0 bits in the Backplane Input Bit Rate Register (BIBRR0-15). The Backplane streams can also be set to operate at 32.768 Mbps. When the MODE32B bit in the Control Register is set high, the first 8 input streams, BSTi0-7, operate at 32.768 Mbps and the remaining 8 streams, BSTi8-15, will not be used and must be connected to a defined logic level.

2.1.8.2 Backplane Output Port

The output traffic on the Backplane streams are aligned based on the $\overline{\text{FP8o}}$ and $\overline{\text{C8o}}$ output timing signals. Operation of stream data in Connection Mode or Message Mode is determined by the state of the BMM bit of the Backplane Connection Memory and the channel high impedance state is controlled by the BE bit of the Backplane Connection Memory. The data source (i.e. from the Local or Backplane Data Memory) is determined by the BSRC bit of the Backplane Connection Memory. Refer to Section 9.2, Backplane Connection Memory and Section 12.4, Backplane Connection Memory Bit Definition for more details. Each output stream, BSTo0-15, can be individually set to operate at 2.048 Mbps, 4.096 Mbps, 8.192 Mbps or 16.384 Mbps by programming the BOBR1-0 bits in the Backplane Output Bit Rate Register (BOBRR0-15). The Backplane streams can also be set to operate at 32.768 Mbps. When the MODE32B bit in the Control Register is set high, the first 8 output streams, BSTo0-7, operate at 32.768 Mbps and the remaining 8 streams, BSTo8-15, will not be used and must be connected to a defined logic level.

2.2 Frame Pulse Input and Master Input Clock Timing

The input frame pulse ($\overline{FP8i}$) is an 8 kHz input signal active for 122 ns or 244 ns at the frame boundary. The FPW bit in the Control Register must be set according to the applied pulse width. See Pin Description and Table 19, “Control Register Bits” on page 53, for details.

The active state and timing of $\overline{FP8i}$ can conform either to the ST-BUS or to the GCI-Bus as shown in Figure 6, ST-BUS and GCI-Bus Input Timing Diagram for Different Data Rates. The ZL50050 device will automatically detect whether an ST-BUS or a GCI-Bus style frame pulse is being used for the master frame pulse ($\overline{FP8i}$). The output frame pulses ($\overline{FP8o}$ and $\overline{FP16o}$) are always of the same style (ST-BUS or GCI-Bus) as the input frame pulse. The active edge of the input clock ($\overline{C8i}$) shall be selected by the state of the Control Register bit C8IPOL.

Note that the active edge of ST-BUS is falling edge, which is the default mode of the device, while GCI-Bus uses rising edge as the active edge. Although GCI frame pulse will be automatically detected, to fully conform to GCI-Bus operation, the device should be set to use $\overline{C8i}$ rising edge as the active edge (by setting bit C8IPOL HIGH) when GCI-Bus is used.

For the purposes of describing the device operation, the remaining part of this document assumes the ST-BUS frame pulse format with a single width frame pulse of 122 ns and a falling active clock-edge, unless explicitly stated otherwise.

In addition, the device provides $\overline{FP8o}$, $\overline{FP16o}$, $\overline{C8o}$ and $\overline{C16o}$ outputs to support external devices which connect to the output ports. The generated frame pulses ($\overline{FP8o}$, $\overline{FP16o}$) will be provided in the same format as the master frame pulse ($\overline{FP8i}$). The polarity of $\overline{C8o}$ and $\overline{C16o}$, at the frame boundary, can be controlled by the Control Register bit, COPOL. An analog phase lock loop (APLL) is used to multiply the input clock frequency on $\overline{C8i}$ to generate an internal clock signal operating at 131.072 MHz.

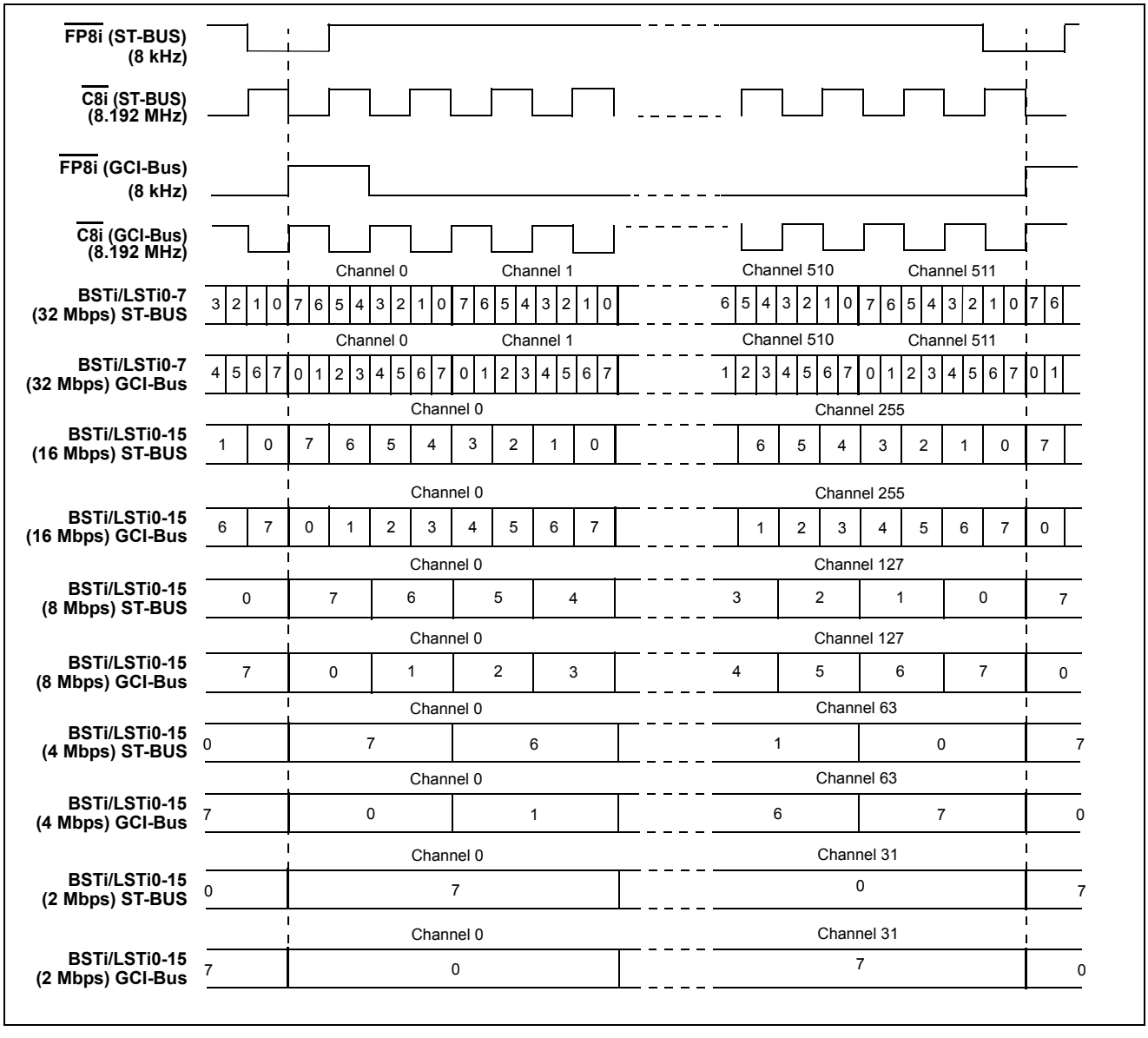

Figure 6 - ST-BUS and GCI-Bus Input Timing Diagram for Different Data Rates

2.3 Input Frame Pulse and Generated Frame Pulse Alignment

The ZL50050 accepts a frame pulse ($\overline{FP8i}$) and generates two frame pulse outputs, $\overline{FP8o}$ and $\overline{FP16o}$, which are aligned to the master frame pulse. There is a constant throughput delay for data being switched from the input to the output of the device such that data which is input during Frame N is output during Frame N+2.

For further details of frame pulse conditions and options, see Section 14.1, Control Register (CR), Figure 22, Frame Boundary Conditions, ST-BUS Operation, and Figure 23, Frame Boundary Conditions, GCI-Bus Operation.

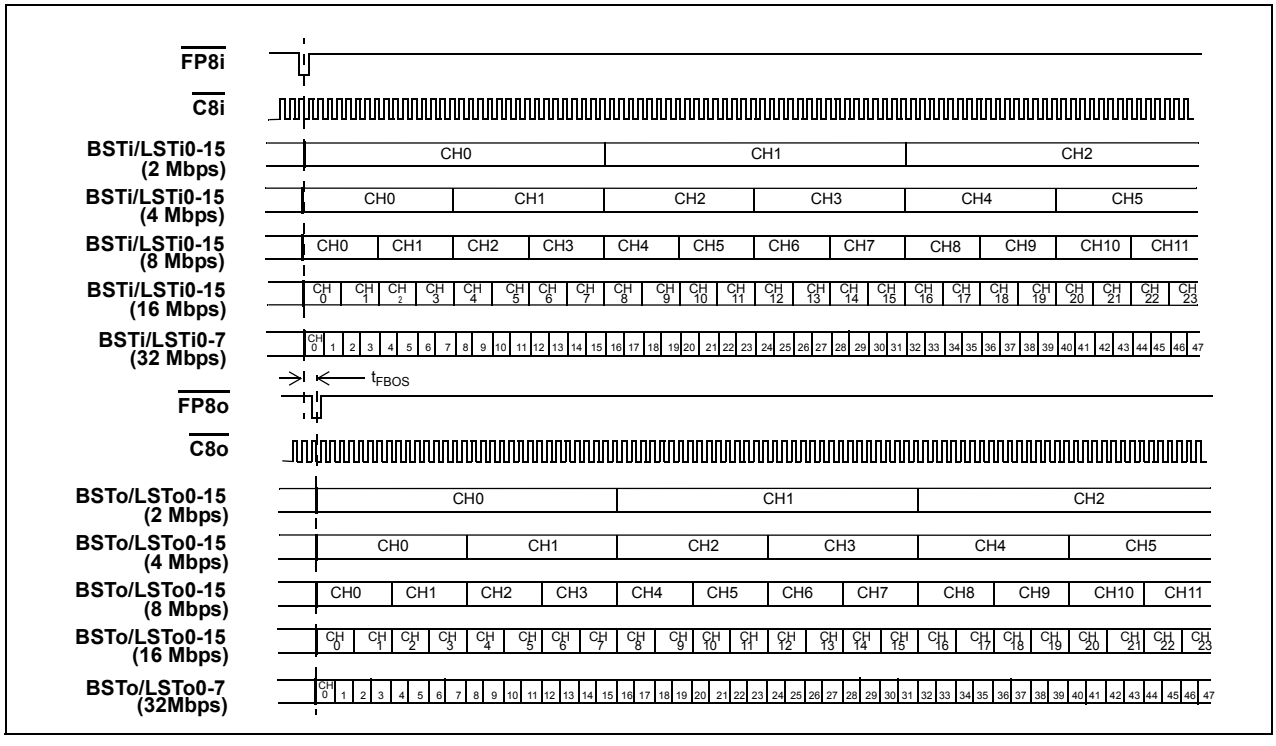

Figure 7 - Input and Output (Generated) Frame Pulse Alignment for Different Data Rates

The t_{FBOS} is the offset between the input frame pulse, $\overline{FP8i}$, and the generated output frame pulse, $\overline{FP8o}$. Refer to the “AC Electrical Characteristics,” on page 80. Note that although the figure above shows the traditional setups of the frame pulses and clocks for both ST-BUS and GCI-Bus configurations, the devices can be configured to accept/generate double-width frame pulses (if the FPW bit in the Control Register is set) as well as to use the opposite clock edge for frame-boundary determination (using the C8IPOL and COPOL bits in the Control Register). See the timing diagrams in “AC Electrical Characteristics,” on page 80 for all of the available configurations.

2.4 Jitter Tolerance Improvement Circuit - Frame Boundary Discriminator

To improve the jitter tolerance of the ZL50050, a Frame Boundary Discriminator (FBD) circuit was added to the device. This circuit is enabled by setting the Control Register bit FBDEN to HIGH. By default the FBD is disabled.

The FBD can operate in two modes, as controlled by the FBD_MODE[2:0] bits of the Control Register. When bits FBD_MODE[2:0] are set to 000_B, the FBD is set to handle lower frequency jitter only (<8 kHz). When bits FBD_MODE[2:0] are set to 111_B, the FBD can handle both low frequency and high frequency jitter. All other values are reserved. These bits are ignored when bit FBDEN is LOW. It is strongly recommended that if bit FBDEN is set HIGH, bits FBD_MODE[2:0] should be set to 111_B to improve the high frequency jitter handling capability.

To achieve the best jitter tolerance performance, it is also recommended that the input data sampling point be optimized. In most applications, the optimum sampling point is 1/2 instead of the default 3/4 (it can be changed by programming all the LIDR and BIDR registers). This will give more allowance for sampling point variations caused