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16 K-Channel Digital Switch with High Jitter Tolerance, Per Stream Rate Conversion (2, 4, 8, 16, or 32 Mbps), and 64 Inputs and 64 Outputs

Data Sheet

February 2006

Features

- 16,384-channel x 16,384-channel non-blocking unidirectional switching.The Backplane and Local inputs and outputs can be combined to form a non-blocking switching matrix with 64 input streams and 64 output streams
- 8,192-channel x 8,192-channel non-blocking Backplane input to Local output stream switch
- 8,192-channel x 8,192-channel non-blocking Local input to Backplane output stream switch
- 8,192-channel x 8,192-channel non-blocking Backplane input to Backplane output switch
- 8,192-channel x 8,192-channel non-blocking Local input to Local output stream switch
- Rate conversion on all data paths, Backplane-to-Local, Local-to-Backplane, Backplane-to-Backplane and Local-to-Local streams
- Backplane port accepts 32 input and 32 output ST-BUS streams with data rates of 2.048 Mbps, 4.096 Mbps, 8.192 Mbps or 16.384 Mbps in any combination, or a fixed allocation of 16 input and 16 output streams at 32.768 Mbps
- Local port accepts 32 input and 32 output ST-BUS streams with data rates of 2.048 Mbps, 4.096 Mbps, 8.192 Mbps or 16.384 Mbps in any combination, or a fixed allocation of 16 input and 16 output streams at 32.768 Mbps
- Exceptional input clock jitter tolerance (17 ns for 16 Mbps or lower data rates, 14 ns for 32 Mbps)
- Per-stream channel and bit delay for Local and Backplane input streams
- Per-stream advancement for Local and Backplane output streams
- Constant 2-frame throughput delay for frame integrity
- Per-channel high impedance output control for Local and Backplane streams

Ordering Information

ZL50060GAC	256 Ball PBGA	Trays
ZL50060GAG2	256 Ball PBGA**	Trays
ZL50061GAG	272 Ball PBGA	Trays
ZL50061GAG2	272 Ball PBGA**	Trays

**Pb Free Tin/Silver/Copper

-40°C to +85°C

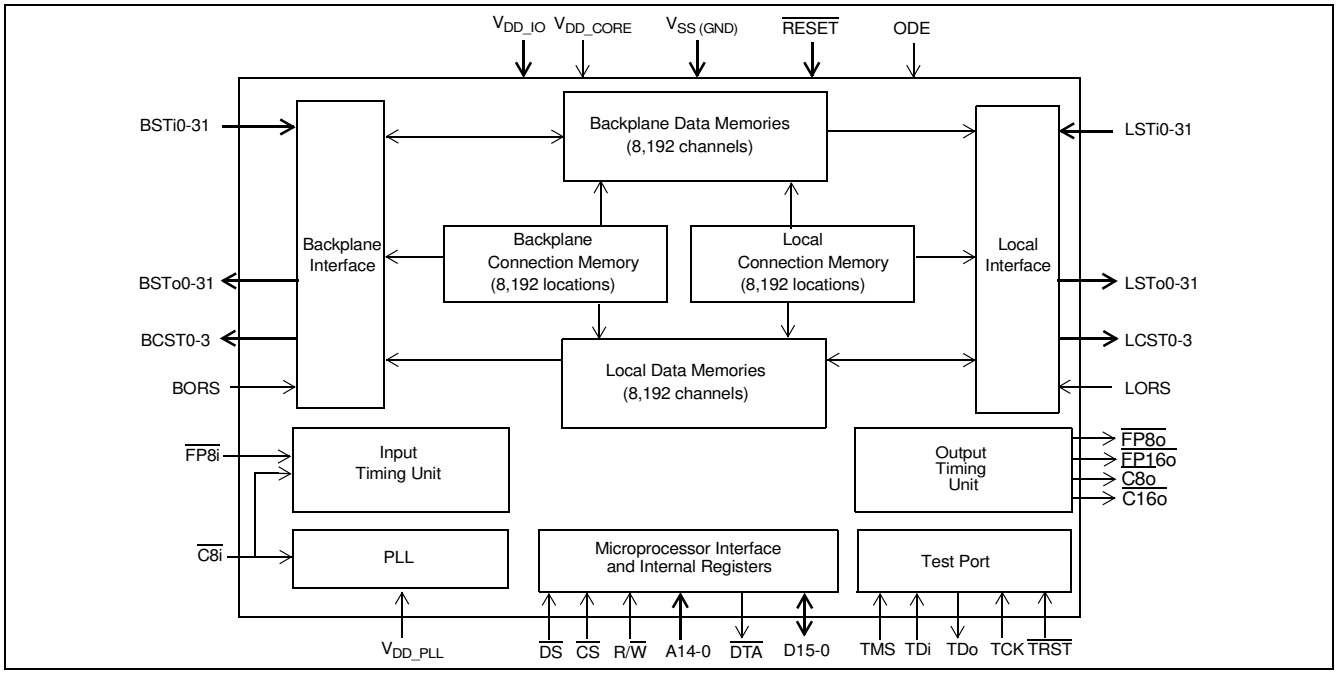

Figure 1 - ZL50060/1 Functional Block Diagram

- Per-channel driven-high output control for Local and Backplane streams
- High impedance control outputs for external drivers on Local and Backplane ports
- Per-channel message mode for Local and Backplane output streams
- Connection memory block programming for fast device initialization
- BER testing for Local and Backplane ports
- Automatic selection between ST-BUS and GCI-Bus operation
- Non-multiplexed Motorola microprocessor interface
- Conforms to the mandatory requirements of the IEEE-1149.1 (JTAG) standard
- Memory Built-In-Self-Test (BIST), controlled via microprocessor register
- 1.8 V core supply voltage
- 3.3 V I/O supply voltage
- 5 V tolerant inputs, outputs and I/Os
- ZL50061 is pin-to-pin compatible with Zarlink's MT90869 device [1]

Note 1: For software compatibility between ZL50061 and MT90869, please refer to Section 2.6.

Applications

- Central Office Switches (Class 5)
- Media Gateways
- Class-independent switches
- Access Concentrators
- Scalable TDM-Based Architectures
- Digital Loop Carriers

Device Overview

The ZL50060 and ZL50061 are two different packages of the same device. The ZL50060/1 has two data ports, the Backplane and the Local port. Both the Backplane and Local ports have two independent modes of operation, either 32 input and 32 output streams operated at 2.048 Mbps, 4.096 Mbps, 8.192 Mbps or 16.384 Mbps, in any combination, or 16 input and 16 output streams operated at 32.768 Mbps.

The ZL50060/1 contains two data memory blocks (Backplane and Local) to provide the following switching path configurations:

- Input-to-Output Unidirectional, supporting 16 K x 16 K switching
- Backplane-to-Local Bi-directional, supporting 8 K x 8 K data switching,
- Local-to-Backplane Bi-directional, supporting 8 K x 8 K data switching,
- Backplane-to-Backplane Bi-directional, supporting 8 K x 8 K data switching.
- Local-to-Local Bi-directional, supporting 8 K x 8 K data switching.

The device contains two connection memory blocks, one for the Backplane output and one for the Local output. Data to be output on the serial streams may come from either of the data memories (Connection Mode) or directly from the connection memory contents (Message Mode).

In Connection Mode, the contents of the connection memory define, for each output stream and channel, the source stream and channel (stored in data memory) to be switched.

In Message Mode, microprocessor data can be written to the connection memory for broadcast on the output streams on a per channel basis. This feature is useful for transferring control and status information to external circuits or other ST-BUS devices.

The device uses a master frame pulse ($\overline{\text{FP8i}}$) and master clock ($\overline{\text{C8i}}$) to define the input frame boundary and timing for both the Backplane port and the Local port. The device will automatically detect whether an ST-BUS or a GCI-Bus style frame pulse is being used. There is a two-frame delay from the time $\overline{\text{RESET}}$ is de-asserted to the establishment of full switch functionality. During this period, the input frame pulse format is determined before switching begins.

The device provides $\overline{\text{FP8o}}$, $\overline{\text{FP16o}}$, $\overline{\text{C8o}}$ and $\overline{\text{C16o}}$ outputs to support external devices connected to the outputs of the Backplane and Local ports.

A non-multiplexed Motorola microprocessor port allows programming of the various device operation modes and switching configurations. The microprocessor port provides access for Register read/write, Connection Memory read/write and Data Memory read-only operations. The port has a 15-bit address bus, 16-bit data bus and 4 control signals. The microprocessor may monitor channel data in the Backplane and Local data memories.

The mandatory requirements of the IEEE-1149.1 (JTAG) standard are fully supported via a dedicated test port.

The ZL50060 and ZL50061 are each available in one package:

- ZL50060: a 17 mm x 17 mm body, 1 mm ball-pitch, 256-PBGA.
- ZL50061: a 27 mm x 27 mm body, 1.27 mm ball-pitch, 272-PBGA.

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Pinout Diagram: (as viewed through top of package)

A1 corner identified by metallized marking

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	GND	IC_GND	BSTo5	BSTo4	BSTo2	A2	VDD_CORE	A8	A11	A14	$\overline{DS}$	ODE	$\overline{DTA}$	TCK	BCSTo1	LCSTo3	LSTo0	LSTo1	LSTo2	NC
B	BSTo6	BSTo7	BSTo8	VDD_CORE	BSTo1	NC	A5	A7	A10	NC	$\overline{CS}$	VDD_CORE	TDi	$\overline{TRST}$	BCSTo2	LCSTo2	IC_GND	LSTo3	LSTo4	LSTo5
C	BSTo9	BSTo10	IC_GND	BSTo3	BSTo0	A1	A4	A6	NC	A13	R/$\overline{W}$	$\overline{RESET}$	TDo	BCSTo0	BCSTo3	LCSTo1	LCSTo0	LSTo6	LSTo7	LSTo8
D	BSTo11	BSTo12	BSTo13	GND	A0	VDD_IO	A3	GND	A9	A12	VDD_IO	TMS	GND	VDD_CORE	VDD_IO	IC_GND	GND	LSTo9	LSTo10	LSTo11
E	BSTo14	BSTo15	BSTo16	BSTo17													LSTo12	LSTo13	LSTo14	LSTo15
F	BSTo18	BSTo19	BSTo20	VDD_IO													VDD_IO	LSTo16	LSTo17	LSTo18
G	BSTo21	BSTo22	BSTo23	BSTo24													LSTo19	LSTo20	LSTo21	LSTo22
H	BSTo25	BSTo26	BSTo27	GND													GND	LSTo23	LSTo24	LSTo25
J	BSTo28	BSTo29	BSTo30	BSTo31					GND	GND	GND	GND					LSTo26	LSTo27	LSTo28	LSTo29
K	VDD_CORE	BORS	BSTi0	VDD_IO					GND	GND	GND	GND					LSTo30	LSTo31	LORS	VDD_CORE
L	BSTi1	BSTi2	BSTi3	BSTi4					GND	GND	GND	GND					VDD_IO	LSTi0	LSTi1	LSTi2
M	BSTi5	BSTi6	BSTi7	BSTi8					GND	GND	GND	GND					LSTi3	LSTi4	LSTi5	LSTi6
N	BSTi9	BSTi10	VDD_CORE	GND													GND	LSTi7	LSTi8	LSTi9
P	BSTi11	BSTi12	BSTi13	BSTi14													LSTi10	VDD_CORE	LSTi11	LSTi12
R	BSTi15	BSTI16	BSTi17	VDD_IO													VDD_IO	LSTi13	LSTi14	LSTi15
T	BSTi18	BSTi19	BSTi20	BSTi21													VDD_CORE	LSTi16	LSTi17	LSTi18
U	BSTi22	NC	NC	GND	BSTi28	VDD_IO	D10	GND	D4	VDD_IO	GND	VDD_PLL	GND	$\overline{FP8i}$	VDD_IO	VDD_CORE	GND	LSTi19	LSTi20	LSTi21
V	VDD_CORE	NC	NC	BSTi29	VDD_CORE	D13	D9	D7	D3	D0	IC_GND	NC	$\overline{C8o}$	$\overline{FP8o}$	NC	NC	LSTi22	LSTi23	LSTi24	LSTi25
W	BSTi23	BSTi24	BSTi25	BSTi30	D15	D12	D8	D6	D2	IC_GND	IC_GND	$\overline{C8i}$	$\overline{C16o}$	$\overline{FP16o}$	NC	NC	NC	LSTi26	LSTi27	NC
Y	BSTi26	BSTi27	NC	BSTi31	D14	D11	VDD_CORE	D5	D1	IC_GND	VDD_CORE	IC_OPEN	IC_OPEN	VDD_CORE	NC	NC	LSTi29	LSTi30	LSTi31	LSTi28

Figure 2 - ZL50061 PBGA Connections (272 PBGA, 27 mm x 27 mm) Pin Diagram
(as viewed through top of package)

Pinout Diagram: (as viewed through top of package)

A1 corner identified by metallized marking

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	A0	A1	A2	A3	A4	$\overline{DS}$	R/$\overline{W}$	$\overline{CS}$	BCSTo0	BCSTo1	BCSTo2	BCSTo3	LCSTo3	LCSTo2	LCSTo1	LCSTo0
B	BSTo0	BSTo1	BSTo2	BSTo3	A5	A6	A7	A8	A9	ODE	$\overline{RESET}$	TMS	LSTo0	LSTo1	LSTo2	LSTo3
C	BSTo4	BSTo5	BSTo6	BSTo7	A10	A11	A12	A13	A14	$\overline{DTA}$	TDi	TDo	LSTo4	LSTo5	LSTo6	LSTo7
D	BSTo8	BSTo9	BSTo10	BSTo11	BORS	IC_GND	IC_GND	IC_GND	IC_GND	TCK	$\overline{TRST}$	LORS	LSTo8	LSTo9	LSTo10	LSTo11
E	BSTo12	BSTo13	BSTo14	BSTo15	VDD_IO	VDD_IO	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	VDD_IO	VDD_IO	LSTo12	LSTo13	LSTo14	LSTo15
F	BSTo16	BSTo17	BSTo18	BSTo19	VDD_IO	VDD_CORE	GND	GND	GND	GND	VDD_CORE	VDD_IO	LSTo16	LSTo17	LSTo18	LSTo19
G	BSTo20	BSTo21	BSTo22	BSTo23	VDD_IO	GND	GND	GND	GND	GND	GND	VDD_IO	LSTo20	LSTo21	LSTo22	LSTo23
H	BSTo24	BSTo25	BSTo26	BSTo27	VDD_IO	GND	GND	GND	GND	GND	GND	VDD_IO	LSTo24	LST25	LSTo26	LSTo27
J	BSTo28	BSTo29	BSTo30	BSTo31	VDD_CORE	GND	GND	GND	GND	GND	GND	VDD_CORE	LSTo28	LSTo29	LSTo30	LSTo31
K	BSTi0	BSTi1	BSTi2	BSTi3	VDD_CORE	GND	GND	GND	GND	GND	GND	VDD_CORE	LSTi0	LSTi1	LSTi2	LSTi3
L	BSTi4	BSTi5	BSTi6	BSTi7	VDD_IO	VDD_CORE	VDD_CORE	GND	GND	VDD_CORE	VDD_CORE	VDD_IO	LSTi4	LSTi5	LSTi6	LSTi7
M	BSTi8	BSTi9	BSTi10	BSTi11	VDD_IO	D3	D2	D1	D0	VDD_PLL	NC	VDD_IO	LSTi8	LSTi9	LSTi10	LSTi11
N	BSTi12	BSTi13	BSTi14	BSTi15	BSTi16	D7	D6	D5	D4	IC_OPEN	IC_OPEN	LSTi12	LSTi13	LSTi14	LSTi15	LSTi16
P	BSTi17	BSTi18	BSTi19	BSTi20	BSTi21	D11	D10	D9	D8	$\overline{C16o}$	$\overline{FP16o}$	LSTi17	LSTi18	LSTi19	LSTi20	LSTi21
R	BSTi22	BSTi23	BSTi24	BSTi25	BSTi26	D15	D14	D13	D12	$\overline{FP8o}$	$\overline{FP8i}$	LSTi22	LSTi23	LSTi24	LSTi25	LSTi26
T	BSTi27	BSTi28	BSTi29	BSTi30	BSTi31	IC_GND	IC_GND	IC_GND	IC_GND	$\overline{C8i}$	$\overline{C8o}$	LSTi27	LSTi28	LSTi29	LSTi30	LSTi31

Figure 3 - ZL50060 PBGA Connections (256 PBGA, 17 mm x 17 mm) Pin Diagram
(as viewed through top of package)

Pin Description

Pin Name	ZL50061 Package Coordinates (272-ball PBGA)	ZL50060 Package Coordinates (256-ball PBGA)	Description
Device Timing			
$\overline{C8i}$	W12	T10	**Master Clock (5 V Tolerant Schmitt-Triggered Input).** This pin accepts an 8.192 MHz clock. The internal frame boundary is aligned with the clock falling or rising edge, as controlled by the C8IPOL bit in the Control Register. Input data on both the Backplane and Local sides (BSTi0-31 and LSTi0-31) must be aligned to this clock and the accompanying input frame pulse, $\overline{FP8i}$.
$\overline{FP8i}$	U14	R11	**Frame Pulse Input (5 V Tolerant Schmitt-Triggered Input)**. When the Frame Pulse Width bit (FPW) of the Control Register is LOW (default), this pin accepts a 122 ns-wide frame pulse. When the FPW bit is HIGH, this pin accepts a 244 ns-wide frame pulse. The device will automatically detect whether an ST-BUS or GCI-Bus style frame pulse is applied. Input data on both the Backplane and Local sides (BSTi0-31 and LSTi0-31) must be aligned to this frame pulse and the accompanying input clock, $\overline{C8i}$.
$\overline{C8o}$	V13	T11	**$\overline{C8o}$ Output Clock (5 V Tolerant Three-state Output).** This pin outputs an 8.192 MHz clock generated within the device. The clock falling edge or rising edge is aligned with the output frame boundary presented on $\overline{FP8o}$; this edge polarity alignment is controlled by the COPOL bit of the Control Register. Output data on both the Backplane and Local sides (BSTo0-31 and LSTo0-31) will be aligned to this clock and the accompanying output frame pulse, $\overline{FP8o}$.
$\overline{FP8o}$	V14	R10	**Frame Pulse Output (5 V Tolerant Three-state Output).** When the Frame Pulse Width bit (FPW) of the Control Register is LOW (default), this pin outputs a 122 ns-wide frame pulse. When the FPW bit is HIGH, this pin outputs a 244 ns-wide frame pulse. The frame pulse, running at 8 kHz rate, will have the same format (ST-BUS or GCI-Bus) as the input frame pulse ($\overline{FP8i}$). Output data on both the Backplane and Local sides (BSTo0-31 and LSTo0-31) will be aligned to this frame pulse and the accompanying output clock, $\overline{C8o}$.
$\overline{C16o}$	W13	P10	**$\overline{C16o}$ Output Clock (5 V Tolerant Three-state Output).** This pin outputs a 16.384 MHz clock generated within the device. The clock falling edge or rising edge is aligned with the output frame boundary presented on $\overline{FP16o}$; this edge polarity alignment is controlled by the COPOL bit of the Control Register. Output data on both the Backplane and Local sides (BSTo0-31 and LSTo0-31) will be aligned to this clock and the accompanying output frame pulse, $\overline{FP16o}$.

Pin Description (continued)

Pin Name	ZL50061 Package Coordinates (272-ball PBGA)	ZL50060 Package Coordinates (256-ball PBGA)	Description
$\overline{\text{FP16o}}$	W14	P11	**Frame Pulse Output (5 V Tolerant Three-state Output).** When the Frame Pulse Width bit (FPW) of the Control Register is LOW (default), this pin outputs a 61 ns-wide frame pulse. When the FPW bit is HIGH, this pin outputs a 122 ns-wide frame pulse. The frame pulse, running at 8 kHz rate, will have the same format (ST-BUS or GCI-Bus) as the input frame pulse ($\overline{\text{FP8i}}$). Output data on both the Backplane and Local sides (BSTo0-31 and LSTo0-31) will be aligned to this frame pulse and the accompanying output clock, C16o.
Backplane and Local Inputs			
BSTi0-15	K3, L1, L2, L3, L4, M1, M2, M3, M4, N1, N2, P1, P2, P3, P4, R1	K1, K2, K3, K4, L1, L2, L3, L4, M1, M2, M3, M4, N1, N2, N3, N4	**Backplane Serial Input Streams 0 to 15 (5 V Tolerant Inputs with Internal Pull-downs).** In Backplane Non-32 Mbps Mode, these pins accept serial TDM data streams at a data rate of: 16.384 Mbps (with 256 channels per stream), 8.192 Mbps (with 128 channels per stream), 4.096 Mbps (with 64 channels per stream) or 2.048 Mbps (with 32 channels per stream). The data rate is independently programmable for each input stream. In Backplane 32 Mbps Mode, these pins accept serial TDM data streams at a fixed data rate of 32.768 Mbps (with 512 channels per stream).
BSTi16-31	R2, R3, T1, T2, T3, T4, U1, W1, W2, W3, Y1, Y2, U5, V4, W4, Y4	N5, P1, P2, P3, P4, P5, R1, R2, R3, R4, R5, T1, T2, T3, T4, T5	**Backplane Serial Input Streams 16 to 31 (5 V Tolerant Inputs with Internal Pull-downs).** In Backplane Non-32 Mbps Mode, these pins accept serial TDM data streams at a data rate of: 16.384 Mbps (with 256 channels per stream), 8.192 Mbps (with 128 channels per stream), 4.096 Mbps (with 64 channels per stream) or 2.048 Mbps (with 32 channels per stream). The data rate is independently programmable for each input stream. In Backplane 32 Mbps Mode, these pins are unused and should be externally connected to a defined logic level.

Pin Description (continued)

Pin Name	ZL50061 Package Coordinates (272-ball PBGA)	ZL50060 Package Coordinates (256-ball PBGA)	Description
LSTi0-15	L18, L19, L20, M17, M18, M19, M20, N18, N19, N20, P17, P19, P20, R18, R19, R20	K13, K14, K15, K16, L13, L14, L15, L16, M13, M14, M15, M16, N12, N13, N14, N15	**Local Serial Input Streams 0 to 15 (5 V Tolerant Inputs with Internal Pull-downs).** In Local Non-32 Mbps Mode, these pins accept serial TDM data streams at a data rate of: 16.384 Mbps (with 256 channels per stream), 8.192 Mbps (with 128 channels per stream), 4.096 Mbps (with 64 channels per stream) or 2.048 Mbps (with 32 channels per stream). The data rate is independently programmable for each input stream. In Local 32 Mbps Mode, these pins accept serial TDM data streams at a fixed data rate of 32.768 Mbps (with 512 channels per stream).
LSTi16-31	T18, T19, T20, U18, U19, U20, V17, V18, V19, V20, W18, W19, Y20, Y17, Y18, Y19	N16, P12, P13, P14, P15, P16, R12, R13, R14, R15, R16, T12, T13, T14, T15, T16	**Local Serial Input Streams 16 to 31 (5 V Tolerant Inputs with Internal Pull-downs).** In Local Non-32 Mbps Mode, these pins accept serial TDM data streams at a data rate of: 16.384 Mbps (with 256 channels per stream), 8.192 Mbps (with 128 channels per stream), 4.096 Mbps (with 64 channels per stream) or 2.048 Mbps (with 32 channels per stream). The data rate is independently programmable for each input stream. In Local 32 Mbps Mode, these pins are unused and should be externally connected to a defined logic level.
Backplane and Local Outputs and Control			
ODE	A12	B10	**Output Drive Enable (5 V Tolerant Input with Internal Pull-up)**. An asynchronous input providing Output Enable control to the BSTo0-31, LSTo0-31, BCSTo0-3, and LCSTo0-3 outputs. When LOW, the BSTo0-31 and LSTo0-31 outputs are driven HIGH or high impedance (dependent on the **BORS** and **LORS** pin settings respectively) and the outputs BCSTo0-3 and LCSTo0-3 are driven low. When HIGH, the outputs BSTo0-31, LSTo0-31, BCSTo0-3, and LCSTo0-3 are enabled.

Pin Description (continued)

Pin Name	ZL50061 Package Coordinates (272-ball PBGA)	ZL50060 Package Coordinates (256-ball PBGA)	Description
BORS	K2	D5	**Backplane Output Reset State (5 V Tolerant Input with Internal Pull-down)**. When this input is LOW, the device will initialize with the BSTo0-31 outputs driven high, and the BCSTo0-3 outputs driven low. Following initialization, the Backplane stream outputs are always active and a high impedance state, if required on a per-channel basis, may be implemented with external buffers controlled by outputs BCSTo0-3. When this input is HIGH, the device will initialize with the BSTo0-31 outputs at high impedance and the BCSTo0-3 outputs driven low. Following initialization, the Backplane stream outputs may be set active or high impedance using the **ODE** pin or on a per-channel basis with the **BE** bit in the Backplane Connection Memory.
BSTo0-15	C5, B5, A5, C4, A4, A3, B1, B2, B3, C1, C2, D1, D2, D3, E1, E2	B1, B2, B3, B4, C1, C2, C3, C4, D1, D2, D3, D4, E1, E2, E3, E4	**Backplane Serial Output Streams 0 to 15 (5 V Tolerant, Three-state Outputs with Slew-Rate Control)**. In Backplane Non-32 Mbps Mode, these pins output serial TDM data streams at a data rate of: 16.384 Mbps (with 256 channels per stream), 8.192 Mbps (with 128 channels per stream), 4.096 Mbps (with 64 channels per stream) or 2.048 Mbps (with 32 channels per stream). The data rate is independently programmable for each output stream. In Backplane 32 Mbps Mode, these pins output serial TDM data streams at a fixed data rate of 32.768 Mbps (with 512 channels per stream). Refer to the descriptions of the **BORS** and **ODE** pins for control of the output HIGH or high impedance state.

Pin Description (continued)

Pin Name	ZL50061 Package Coordinates (272-ball PBGA)	ZL50060 Package Coordinates (256-ball PBGA)	Description
BSTo16-31	E3, E4, F1, F2, F3, G1, G2, G3, G4, H1, H2, H3, J1, J2, J3, J4	F1, F2, F3, F4, G1, G2, G3, G4, H1, H2, H3, H4, J1, J2, J3, J4	**Backplane Serial Output Streams 16 to 31 (5 V Tolerant, Three-state Outputs with Slew-Rate Control).** In Backplane Non-32 Mbps Mode, these pins output serial TDM data streams at a data rate of: 16.384 Mbps (with 256 channels per stream), 8.192 Mbps (with 128 channels per stream), 4.096 Mbps (with 64 channels per stream) or 2.048 Mbps (with 32 channels per stream). The data rate is independently programmable for each output stream. These pins are unused when the Backplane 32 Mbps Mode is selected. Therefore, the value output on these pins during Backplane 32 Mbps Mode (either driven-HIGH or high impedance) is dependent on the configuration of the BORS pin. Refer to the descriptions of the **BORS** and **ODE** pins for control of the output HIGH or high impedance state.
BCSTo0-3	C14, A15, B15, C15	A9, A10, A11, A12	**Backplane Output Channel high impedance Control (5 V Tolerant, Three-state Outputs).** These pins control external buffering individually for a set of Backplane output streams on a per-channel basis. When LOW, the external output buffer will be tri-stated. When HIGH, the external output buffer will be enabled. In Backplane Non-32 Mbps Mode (stream rates 2 Mbps to 16Mbps): BCSTo0 is the output enable for BSTo0,4,8,12,16,20,24,28 BCSTo1 is the output enable for BSTo1,5,9,13,17,21,25,29 BCSTo2 is the output enable for BSTo2,6,10,14,18,22,26,30 BCSTo3 is the output enable for BSTo3,7,11,15,19,23,27,31. In Backplane 32Mbps Mode (stream rate 32Mbps): BCSTo0 is the output enable for BSTo0,4,8,12 BCSTo1 is the output enable for BSTo1,5,9,13 BCSTo2 is the output enable for BSTo2,6,10,14 BCSTo3 is the output enable for BSTo3,7,11,15. Refer to the descriptions of the **BORS** and **ODE** pins for control of the output LOW or active state.

Pin Description (continued)

Pin Name	ZL50061 Package Coordinates (272-ball PBGA)	ZL50060 Package Coordinates (256-ball PBGA)	Description
LORS	K19	D12	**Local Output Reset State (5 V Tolerant Input with Internal Pull-down)**. When this input is LOW, the device will initialize with the LSTo0-31 outputs driven high, and the LCSTo0-3 outputs driven low. Following initialization, the Local stream outputs are always active and a high impedance state, if required on a per-channel basis, may be implemented with external buffers controlled by outputs LCSTo0-3. When this input is HIGH, the device will initialize with the LSTo0-31 outputs at high impedance and the LCSTo0-3 outputs driven low. Following initialization, the Local stream outputs may be set active or high impedance using the **ODE** pin or on a per-channel basis with the **LE** bit in the Local Connection Memory.
LSTo0-15	A17, A18, A19, B18, B19, B20, C18, C19, C20, D18, D19, D20, E17, E18, E19, E20	B13, B14, B15, B16, C13, C14, C15, C16, D13, D14, D15, D16, E13, E14, E15, E16	**Local Serial Output Streams 0 to 15 (5 V Tolerant Three-state Outputs with Slew-Rate Control)**. In Local Non-32 Mbps Mode, these pins output serial TDM data streams at a data rate of: 16.384 Mbps (with 256 channels per stream), 8.192 Mbps (with 128 channels per stream), 4.096 Mbps (with 64 channels per stream) or 2.048 Mbps (with 32 channels per stream). The data rate is independently programmable for each output stream. In Local 32 Mbps Mode, these pins output serial TDM data streams at a fixed data rate of 32.768 Mbps (with 512 channels per stream). Refer to the descriptions of the **LORS** and **ODE** pins for control of the output HIGH or high impedance state.

Pin Description (continued)

Pin Name	ZL50061 Package Coordinates (272-ball PBGA)	ZL50060 Package Coordinates (256-ball PBGA)	Description
LSTo16-31	F18, F19, F20, G17, G18, G19, G20, H18, H19, H20, J17, J18, J19, J20, K17, K18	F13, F14, F15, F16, G13, G14, G15, G16, H13, H14, H15, H16, J13, J14, J15, J16	**Local Serial Output Streams 16 to 31 (5 V Tolerant Three-state Outputs with Slew-Rate Control)**. In Local Non-32 Mbps Mode, these pins output serial TDM data streams at a data rate of: 16.384 Mbps (with 256 channels per stream), 8.192 Mbps (with 128 channels per stream), 4.096 Mbps (with 64 channels per stream) or 2.048 Mbps (with 32 channels per stream). The data rate is independently programmable for each output stream. These pins are unused when the Local 32 Mbps Mode is selected. Therefore, the value output on these pins during Local 32 Mbps Mode (either driven-HIGH or high impedance) is dependent on the configuration of the LORS pin. Refer to the descriptions of the **LORS** and **ODE** pins for control of the output HIGH or high impedance state.
LCSTo0-3	C17, C16, B16, A16	A16, A15, A14, A13	**Local Output Channel high impedance Control (5 V Tolerant Three-state Outputs).** These pins control external buffering individually for a set of Local output streams on a per-channel basis. When LOW, the external output buffer will be tri-stated. When HIGH, the external output buffer will be enabled. In Local Non-32 Mbps Mode (stream rate 2 Mbps to 16 Mbps): LCSTo0 is the output enable for LSTo0,4,8,12,16,20,24,28 LCSTo1 is the output enable for LSTo1,5,9,13,17,21,25,29 LCSTo2 is the output enable for LSTo2,6,10,14,18,22,26,30 LCSTo3 is the output enable for LSTo3,7,11,15,19,23,27,31. In Local 32 Mbps Mode (stream rate 32 Mbps): LCSTo0 is the output enable for LSTo0,4,8,12 LCSTo1 is the output enable for LSTo1,5,9,13 LCSTo2 is the output enable for LSTo2,6,10,14 LCSTo3 is the output enable for LSTo3,7,11,15. Refer to descriptions of the **LORS** and **ODE** pins for control of the output LOW or active state.

Pin Description (continued)

Pin Name	ZL50061 Package Coordinates (272-ball PBGA)	ZL50060 Package Coordinates (256-ball PBGA)	Description
Microprocessor Port Signals			
A0 - A14	D5, C6, A6, D7, C7, B7, C8, B8, A8, D9, B9, A9, D10, C10, A10	A1, A2, A3, A4, A5, B5, B6, B7, B8, B9, C5, C6, C7, C8, C9	**Address 0 - 14 (5 V Tolerant Inputs).** These pins form the 15-bit address bus to the internal memories and registers. A0 = LSB
D0 - D15	V10, Y9, W9, V9, U9, Y8, W8, V8, W7, V7, U7, Y6, W6, V6, Y5, W5	M9, M8, M7, M6, N9, N8, N7, N6, P9, P8, P7, P6, R9, R8, R7, R6	**Data Bus 0 - 15 (5 V Tolerant Inputs/Outputs with Slew-Rate Control).** These pins form the 16-bit data bus of the microprocessor port. D0 = LSB
$\overline{CS}$	B11	A8	**Chip Select (5 V Tolerant Input).** Active LOW input used by the microprocessor to enable the microprocessor port access. **Note that a minimum of 30 ns must separate the de-assertion of DTA (to high) and the assertion of $\overline{CS}$ and/or $\overline{DS}$ to initiate the next access.**
$\overline{DS}$	A11	A6	**Data Strobe (5 V Tolerant Input).** This active LOW input works in conjunction with $\overline{CS}$ to enable the microprocessor port read and write operations. **Note that a minimum of 30 ns must separate the de-assertion of DTA (to high) and the assertion of CS and/or $\overline{DS}$ to initiate the next access.**
R/$\overline{W}$	C11	A7	**Read/$\overline{Write}$ (5 V Tolerant Input).** This input controls the direction of the data bus lines (D0-D15) during a microprocessor access.
$\overline{DTA}$	A13	C10	**Data Transfer Acknowledgment (5 V Tolerant Three-state Output).** This active LOW output indicates that a data bus transfer is complete. A pull-up resistor is required to hold a HIGH level. **Note that a minimum of 30 ns must separate the de-assertion of DTA (to high) and the assertion of CS and/or DS to initiate the next access.**

Pin Description (continued)

Pin Name	ZL50061 Package Coordinates (272-ball PBGA)	ZL50060 Package Coordinates (256-ball PBGA)	Description
$\overline{\text{RESET}}$	C12	B11	**Device Reset (5 V Tolerant Input with Internal Pull-up).** This input (active LOW) asynchronously applies reset and synchronously releases reset to the device. In the reset state, the outputs LSTo0-31 and BSTo0-31 are set to a HIGH or high impedance state, depending on the state of the LORS and $\overline{\text{BORS}}$ external control pins, respectively. The assertion of $\overline{\text{RESET}}$ causes the LCSTo0-3 and BCSTo0-3 pins to be driven LOW (refer to Table 2). The assertion of this pin also clears the device registers and internal counters. **Refer to Section 8.3 on page 47 for the timing requirements regarding this reset signal**.
JTAG Control Signals			
TCK	A14	D10	**Test Clock (5 V Tolerant Input).** Provides the clock to the JTAG test logic.
TMS	D12	B12	**Test Mode Select (5 V Tolerant Input with Internal Pull-up)**. JTAG signal that controls the state transitions of the TAP controller.
TDi	B13	C11	**Test Serial Data In (5 V Tolerant Input with Internal Pull-up).** JTAG serial test instructions and data are shifted in on this pin.
TDo	C13	C12	**Test Serial Data Out (5 V Tolerant Three-state Output).** JTAG serial data is output on this pin on the falling edge of TCK. This pin is held in a high impedance state when JTAG is not enabled.
$\overline{\text{TRST}}$	B14	D11	**Test Reset (5 V Tolerant Input with Internal Pull-up).** Asynchronously initializes the JTAG TAP controller to the Test-Logic-Reset state. This pin must be pulsed LOW during power-up for JTAG testing. This pin must be held LOW for normal functional operation of the device.
Power and Ground Pins			
V_{DD_IO}	D6, D11, D15, F4, F17, K4, L17, R4, R17, U6, U10, U15	E5, E6, E11, E12, F5, F12, G5, G12, H5, H12, L5, L12, M5, M12	**Power Supply for Periphery Circuits:** +3.3 V
V_{DD_CORE}	A7, B4, B12, D14, K1, K20, N3, P18, T17, U16, V1, V5, Y7, Y11, Y14	E7, E8, E9, E10, F6, F11, J5, J12, K5, K12, L6, L7, L10, L11	**Power Supply for Core Circuits:** +1.8 V

Pin Description (continued)

Pin Name	ZL50061 Package Coordinates (272-ball PBGA)	ZL50060 Package Coordinates (256-ball PBGA)	Description
V_{DD_PLL}	U12	M10	**Power Supply for Analog PLL:** +1.8 V
V_{SS} (GND)	A1, D4, D8, D13, D17, H4, H17, J9, J10, J11, J12, K9, K10, K11, K12, L9, L10, L11, L12, M9, M10, M11, M12, N4, N17, U4, U8, U11, U13, U17	F7, F8, F9, F10, G6, G7, G8, G9, G10, G11, H6, H7, H8, H9, H10, H11, J6, J7, J8, J9, J10, J11, K6, K7, K8, K9, K10, K11, L8, L9	Ground.
Unused Pins			
NC	A20, B6, B10, C9, U2, U3, V2, V3, V12, V15, V16, W15, W16, W17, W20, Y3, Y15, Y16	M11	**No Connects.** These pins are not used and can be tied HIGH, LOW, or left unconnected.
IC_OPEN	Y12, Y13	N10, N11	**Internal Connections - OPEN.** These pins must be left unconnected.
IC_GND	A2, B17, C3, D16, V11, W10, W11, Y10	D6, D7, D8, D9, T6, T7, T8, T9	**Internal Connections - GND.** These pins must be tied LOW.

1.0 Unidirectional and Bi-directional Switching Applications

The ZL50060/1 has a maximum capacity of 16,384 input channels and 16,384 output channels. This is calculated from the maximum number of streams and channels: 64 input streams (32 Backplane, 32 Local) at 16.384 Mbps and 64 output streams (32 Backplane, 32 Local) at 16.384 Mbps.

A typical mode of operation is to separate the input and output streams to form a unidirectional switch, as shown in Figure 4 below.

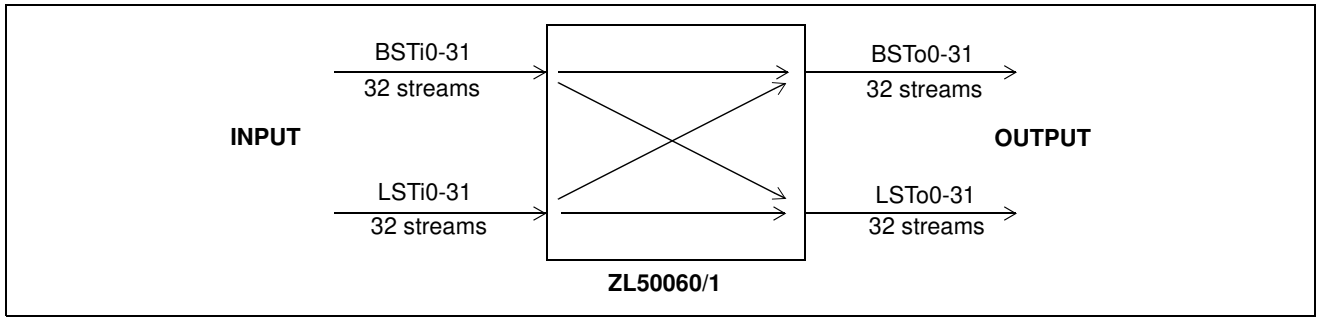

Figure 4 - 16,384 x 16,384 Channels (16 Mbps), Unidirectional Switching

In this system, the Backplane and Local input streams are combined, and the Backplane and Local output streams are combined, so that the switch appears as a 64 input stream by 64 output stream switch. This gives the maximum 16,384 x 16,384 channel capacity.

Often a system design needs to differentiate between a Backplane and a Local side, or it needs to put the switch in a bi-directional configuration. In this case, the ZL50060/1 can be used as shown in Figure 5 to give 8,192 x 8,192 channel bi-directional capacity.

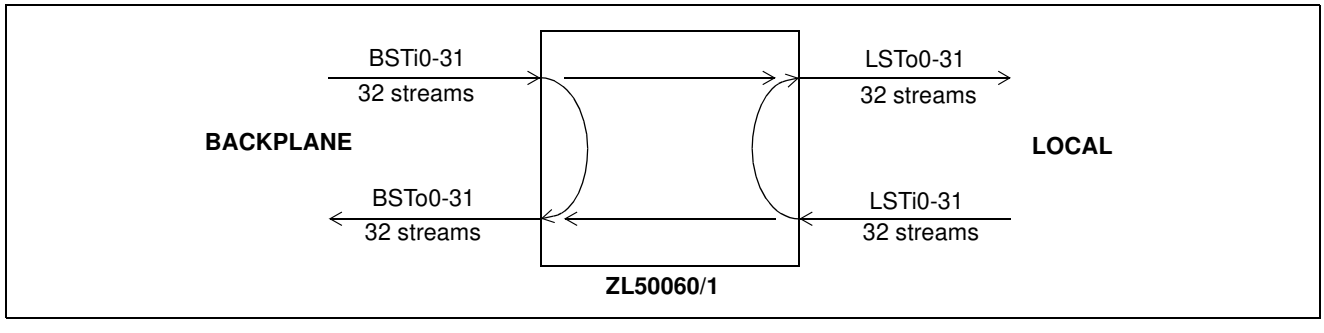

Figure 5 - 8,192 x 8,192 Channels (16 Mbps), Bi-directional Switching

In this system setup, the chip has a capacity of 8,192 input channels and 8,192 output channels on the Backplane side, as well as 8,192 input channels and 8,192 output channels on the Local side. Note that some or all of the output channels on one side can come from the other side, e.g., Backplane input to Local output switching.

Note that in either configuration, the Backplane port can be operated in the Backplane 32Mbps Mode, providing 512 channels on each of the 16 available input and output streams (BSTi0-15 and BSTo0-15) operating at a data rate of 32.768 Mbps, in conjunction with the Local streams (LSTi0-31 and LSTo0-31) operating at 16.384 Mbps (Local Non-32 Mbps Mode) or in conjunction with the Local streams (LSTi0-15 and LSTo0-15) operating at 32.768 Mbps (Local 32 Mbps Mode). Similarly, the Local port can be operated in the Local 32 Mbps Mode, providing 512 channels on each of the 16 available input and output streams (LSTi0-15 and LSTo0-15) operating at a data rate of 32.768 Mbps, in conjunction with the Backplane streams (BSTi0-31 and BSTo0-31) operating at 16.384 Mbps (Backplane Non-32 Mbps Mode) or in conjunction with the Backplane streams (BSTi0-15 and BSTo0-15) operating at 32.768 Mbps (Backplane 32 Mbps Mode).

The modes in which one port operates in 32Mbps Mode while the other port operates in Non-32 Mbps Mode allow data rate conversion between 32.768 Mbps and 16.384 Mbps without loss to the switching capacity.

1.1 Flexible Configuration

The ZL50060/1 can be configured as a 16 K by 16 K non-blocking unidirectional digital switch, an 8 K by 8 K non-blocking bi-directional digital switch, or as a blocking switch with various switching capacities.

1.1.1 Non-Blocking Unidirectional Configuration (Typical System Configuration)

Because the input and output drivers are synchronous, the user can combine input Backplane streams and input Local streams as well as output Backplane streams and output Local streams to increase the total number of input and output streams of the switch in a unidirectional configuration, as shown in Figure 4.

- 16,384-channel x 16,384-channel non-blocking switching from input to output streams

1.1.2 Non-Blocking Bi-directional Configuration

Another typical application is to configure the ZL50060/1 as a non-blocking 8 K by 8 K bi-directional switch, as shown in Figure 5:

- 8,192-channel x 8,192-channel non-blocking switching from Backplane input to Local output streams
- 8,192-channel x 8,192-channel non-blocking switching from Local input to Backplane output streams
- 8,192-channel x 8,192-channel non-blocking switching from Backplane input to Backplane output streams
- 8,192-channel x 8,192-channel non-blocking switching from Local input to Local output streams

1.1.3 Blocking Bi-directional Configuration

The ZL50060/1 can be configured as a blocking bi-directional switch if it is an application requirement. For example, it can be configured as a 12 K by 4 K bi-directional blocking switch, as shown in Figure 6:

- 12,288-channel x 4,096-channel blocking switching from Backplane input to Local output streams
- 4,096-channel x 12,288-channel blocking switching from Local input to Backplane output streams
- 12,288-channel x 12,288-channel non-blocking switching from Backplane input to Backplane output streams
- 4,096-channel x 4,096-channel non-blocking switching from Local input to Local output streams

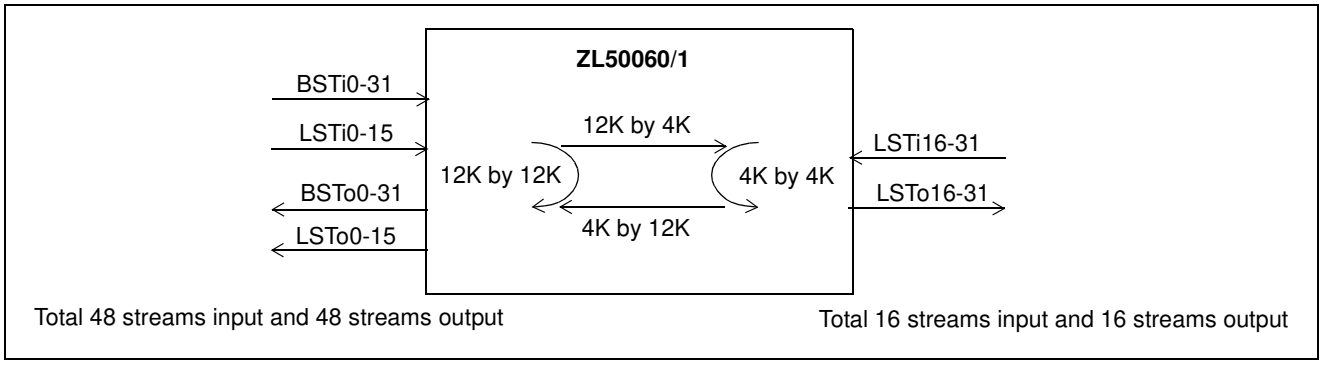

Figure 6 - 12,288 by 4,096 Channels Blocking Bi-directional Configuration

2.0 Functional Description

2.1 Switching Configuration

The device supports five switching configurations: (1) Unidirectional switch, (2) Backplane-to-Local, (3) Local-to-Backplane, (4) Backplane-to-Backplane, and (5) Local-to-Local. The following sections describe the switching paths in detail. Configurations (2) - (5) enable a non-blocking bi-directional switch with 8,192 Backplane input/output channels at Backplane stream data rates of 16.384 Mbps or 32.768 Mbps, and 8,192 Local input/output channels at Local stream data rates of 16.384 Mbps or 32.768 Mbps. The switching paths of configurations (2) to (5) may be operated simultaneously. When the lower data-rates of 8.192, 4.096 and 2.048 Mbps are included, there will be a corresponding reduction in switch capacity although conversion between differing rates will be maintained.

2.1.1 Unidirectional Switch

The device can be configured as a 16,384 x 16,384 unidirectional switch by grouping together all input streams and all output streams. All streams can be operated at a data rate of 16.384 Mbps or 32.768 Mbps, or a combination of 16.384 Mbps and 32.768 Mbps (i.e., one rate on the Local streams and the other rate on the Backplane streams). Lower data rates may be used with a corresponding reduction in switch capacity.

2.1.2 Backplane-to-Local Path

The device can provide data switching between the Backplane input port and the Local output port. The Local Connection Memory determines the switching configurations.

2.1.3 Local-to-Backplane Path

The device can provide data switching between the Local input port and the Backplane output port. The Backplane Connection Memory determines the switching configurations.

2.1.4 Backplane-to-Backplane Path

The device can provide data switching between the Backplane input and output ports. The Backplane Connection Memory determines the switching configurations.

2.1.5 Local-to-Local Path

The device can provide data switching between the Local input and output ports. The Local Connection Memory determines the switching configurations.

2.1.6 Port Data Rate Modes and Selection

The bit rate for each input stream is selected by writing to dedicated input bit rate registers, BIBRR0 to BIBRR31 for Backplane Input Bit Rate Registers (see Table 50) and LIBRR0 to LIBRR31 for Local Input Bit Rate Registers (see Table 46).

The bit rate for each output stream is selected by writing to dedicated output bit rate registers, BOBRR0 to BOBRR31 for Backplane Output Bit Rate Registers (see Table 52) and LOBRR0 to LOBRR31 for Local Output Bit Rate Registers (see Table 48).

If the Backplane 32 Mbps Mode is selected by setting the Control Register bit MODE32B HIGH, the settings in BIBRRn and BOBRRn are ignored. Similarly, if the Local 32 Mbps Mode is selected by setting the Control Register bit MODE32L HIGH, the settings in LIBRRn and LOBRRn are ignored.

Stream Numbers	Rate Selection Capability (for each individual stream)
Local Input streams - LSTi0-15	2.048, 4.096, 8.192 or 16.384 Mbps in Local Non-32 Mbps Mode. All streams at 32.768 Mbps in Local 32 Mbps Mode.
Local Input streams - LSTi16-31	2.048, 4.096, 8.192 or 16.384 Mbps in Local Non-32 Mbps Mode. Unused in Local 32 Mbps Mode.
Backplane Input streams - BSTi0-15	2.048, 4.096, 8.192 or 16.384 Mbps in Backplane Non-32 Mbps Mode. All streams at 32.768 Mbps in Backplane 32 Mbps Mode.
Backplane Input streams - BSTi16-31	2.048, 4.096, 8.192 or 16.384 Mbps in Backplane Non-32 Mbps Mode. Unused in Backplane 32 Mbps Mode.
Local Output streams - LSTo0-15	2.048, 4.096, 8.192 or 16.384 Mbps in Local Non-32 Mbps Mode. All streams at 32.768 Mbps in Local 32 Mbps Mode.
Local Output streams - LSTo16-31	2.048, 4.096, 8.192 or 16.384 Mbps in Local Non-32 Mbps Mode. Unused in Local 32 Mbps Mode.
Backplane Output streams - BSTo0-15	2.048, 4.096, 8.192 or 16.384 Mbps in Backplane Non-32 Mbps Mode. All streams at 32.768 Mbps in Backplane 32Mbps Mode.
Backplane Output streams - BSTo16-31	2.048, 4.096, 8.192 or 16.384 Mbps in Backplane Non-32 Mbps Mode. Unused in Backplane 32 Mbps Mode.

Table 1 - Per-stream Input and Output Data Rate Selection: Backplane and Local

2.1.7 Local Port Rate Selection

The Local port has 32 input (LSTi0-31) and 32 output (LSTo0-31) data streams.

The Local streams can be operated in one of two modes, Local Non-32 Mbps Mode and Local 32 Mbps Mode. The Local stream data rates are not affected by the operating mode of the Backplane port. The operating mode of the Local side is determined by the state of the Control Register bit MODE32L. Setting this bit HIGH will invoke the Local 32 Mbps Mode. Setting the bit LOW will invoke the Non-32 Mbps Mode. The default value of this bit on device reset is LOW. The timing of the input and output clocks and frame pulses is shown in Figure 8, “Input and Output Frame Pulse Alignment for Different Data Rates” on page 28.

Local Non-32 Mbps Mode: Each of the Local streams (LSTi0-31 and LSTo0-31) can be independently programmed for a data rate of 2.048 Mbps, 4.096 Mbps, 8.192 Mbps or 16.384 Mbps.

Local 32 Mbps Mode: 16 of the Local input streams (LSTi0-15) and 16 of the Local output streams (LSTo0-15) operate at a fixed rate of 32.768 Mbps. In this mode, the remaining input and output streams are unused.

2.1.7.1 Local Input Port

The input traffic on the Local streams are aligned based on the $\overline{\text{FP8i}}$ and $\overline{\text{C8i}}$ input timing signals. Each input stream, LSTi0-31, can be individually set to operate at 2.048 Mbps, 4.096 Mbps, 8.192 Mbps or 16.384 Mbps by programming the LIBR1-0 bits in the Local Input Bit Rate Register (LIBRR0-31). The Local streams can also be set to operate at 32.768 Mbps. When the MODE32L bit in the Control Register is set high, the first 16 input streams, LSTi0-15, operate at 32.768 Mbps and the remaining 16 streams, LSTi16-31, will not be used and must be connected to a defined logic level.

2.1.7.2 Local Output Port

The output traffic on the Local streams are aligned based on the $\overline{\text{FP8o}}$ and $\overline{\text{C8o}}$ output timing signals. Operation of stream data in Connection Mode or Message Mode is determined by the state of the LMM bit of the Local Connection Memory. The channel high impedance state is controlled by the LE bit of the Local Connection Memory. The data source (i.e. from the Local or Backplane Data Memory) is determined by the LSRC bit of the Local Connection Memory. Refer to Section 9.1, Local Connection Memory, and Section 12.3, Local Connection Memory Bit Definition for more details. Each output stream, LSTo0-31, can be individually set to operate at 2.048 Mbps, 4.096 Mbps, 8.192 Mbps or 16.384 Mbps by programming the LOBR1-0 bits in the Local Output Bit Rate Register (LOBRR0-31). The Local streams can also be set to operate at 32.768 Mbps. When the MODE32L bit in the Control Register is set high, the first 16 output streams, LSTo0-15, operate at 32.768 Mbps and the remaining 16 streams, LSTo16-31, will not be used and must be connected to a defined logic level.

2.1.8 Backplane Port Rate Selection

The Backplane port has 32 input (BSTi0-31) and 32 output (BSTo0-31) data streams.

The Backplane streams can be operated in one of two modes, Backplane Non-32 Mbps Mode and Backplane 32 Mbps Mode. The Backplane stream data rates are not affected by the operating mode of the Local port. The operating mode of the Backplane side is determined by the state of the Control Register bit MODE32B. Setting this bit HIGH will invoke the Backplane 32 Mbps Mode. Setting the bit LOW will invoke the Non-32 Mbps Mode. The default value of this bit on device reset is LOW. The timing of the input and output clocks and frame pulses is shown in Figure 8, “Input and Output Frame Pulse Alignment for Different Data Rates” on page 28.

Backplane Non-32 Mbps Mode: Each of the Backplane streams (BSTi0-31 and BSTo0-31) can be independently programmed for a data rate of 2.048 Mbps, 4.096 Mbps, 8.192 Mbps or 16.384 Mbps.

Backplane 32 Mbps Mode: 16 of the Backplane input streams (BSTi0-15) and 16 of the Backplane output streams (BSTo0-15) operate at a fixed rate of 32.768 Mbps. In this mode, the remaining input and output streams are unused.

2.1.8.1 Backplane Input Port

The input traffic on the Backplane streams are aligned based on the $\overline{\text{FP8i}}$ and $\overline{\text{C8i}}$ input timing signals. Each input stream, BSTi0-31, can be individually set to operate at 2.048 Mbps, 4.096 Mbps, 8.192 Mbps or 16.384 Mbps by programming the BIBR1-0 bits in the Backplane Input Bit Rate Register (BIBRR0-31). The Backplane streams can also be set to operate at 32.768 Mbps. When the MODE32B bit in the Control Register is set high, the first 16 input streams, BSTi0-15, operate at 32.768 Mbps and the remaining 16 streams, BSTi16-31, will not be used and must be connected to a defined logic level.

2.1.8.2 Backplane Output Port

The output traffic on the Backplane streams are aligned based on the $\overline{\text{FP8o}}$ and $\overline{\text{C8o}}$ output timing signals. Operation of stream data in Connection Mode or Message Mode is determined by the state of the BMM bit of the Backplane Connection Memory and the channel high impedance state is controlled by the BE bit of the Backplane Connection Memory. The data source (i.e. from the Local or Backplane Data Memory) is determined by the BSRC bit of the Backplane Connection Memory. Refer to Section 9.2, Backplane Connection Memory and Section 12.4, Backplane Connection Memory Bit Definition for more details. Each output stream, BSTo0-31, can be individually set to operate at 2.048 Mbps, 4.096 Mbps, 8.192 Mbps or 16.384 Mbps by programming the BOBR1-0 bits in the Backplane Output Bit Rate Register (BOBRR0-31). The Backplane streams can also be set to operate at 32.768 Mbps. When the MODE32B bit in the Control Register is set high, the first 16 output streams, BSTo0-15, operate at 32.768 Mbps and the remaining 16 streams, BSTo16-31, will not be used and must be connected to a defined logic level.