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16K-Channel Digital Switch with High Jitter Tolerance, Single Rate (32Mbps), and 32 Inputs and 32 Output

Data Sheet

November 2003

Features

- 16,384-channel x 16,384-channel non-blocking unidirectional switching.The Backplane and Local inputs and outputs can be combined to form a non-blocking switching matrix with 32 input streams and 32 output streams
- 8,192-channel x 8,192-channel non-blocking Backplane input to Local output stream switch
- 8,192-channel x 8,192-channel non-blocking Local input to Backplane output stream switch
- 8,192-channel x 8,192-channel non-blocking Backplane input to Backplane output switch
- 8,192-channel x 8,192-channel non-blocking Local input to Local output stream switch
- Backplane port accepts 16 input and 16 output ST-BUS streams with data rate of 32.768Mbps
- Local port accepts 16 input and 16 output ST-BUS streams with data rate of 32.768Mbps
- Exceptional input clock jitter tolerance (14ns)
- Per-stream bit delay for Local and Backplane input streams
- Per-stream advancement for Local and Backplane output streams

Ordering Information

ZL50063GAC 196-Ball PBGA

-40°C to +85°C

- Constant 2-frame throughput delay for frame integrity
- Per-channel high impedance output control for Local and Backplane streams
- Per-channel driven-high output control for Local and Backplane streams
- Per-channel message mode for Local and Backplane output streams
- Connection memory block programming for fast device initialization
- Automatic selection between ST-BUS and GCI-Bus operation
- Non-multiplexed Motorola microprocessor interface

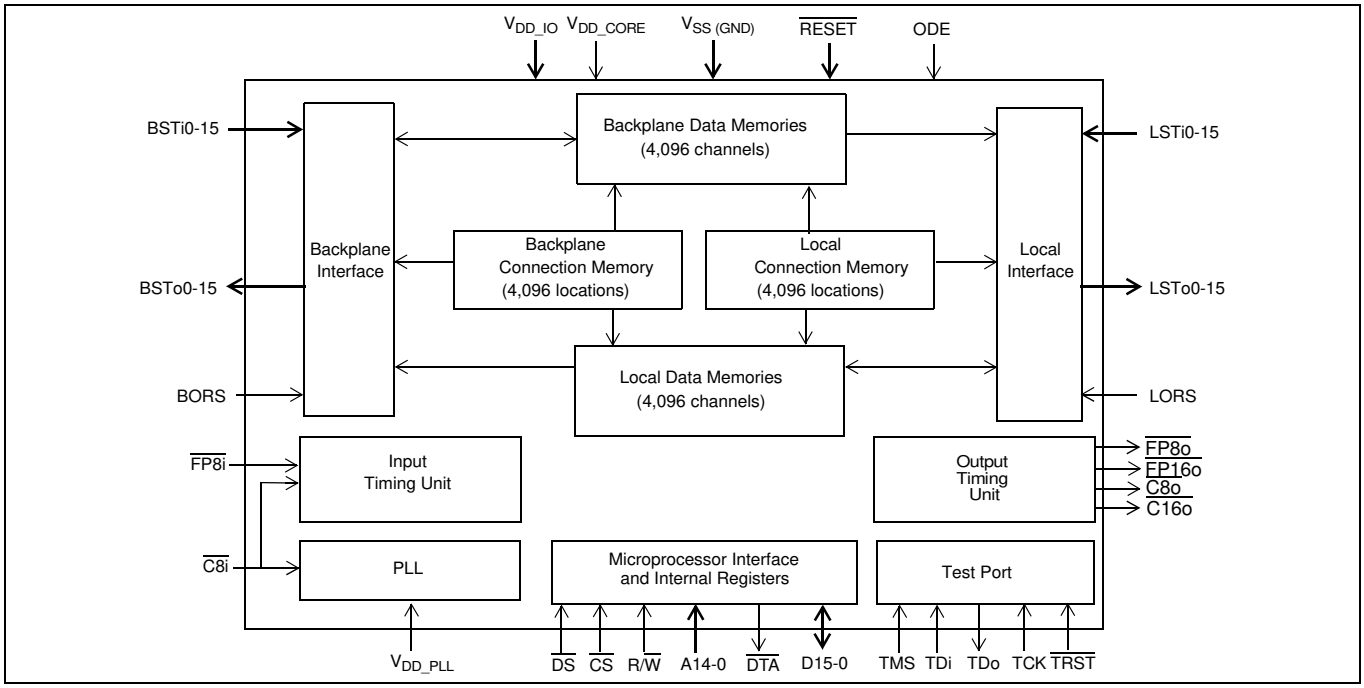

Figure 1 - ZL50063 Functional Block Diagram

- Conforms to the mandatory requirements of the IEEE-1149.1 (JTAG) standard
- Memory Built-In-Self-Test (BIST), controlled via microprocessor register
- 1.8V core supply voltage
- 3.3V I/O supply voltage
- 5V tolerant inputs, outputs and I/Os

Applications

- Central Office Switches (Class 5)
- Media Gateways
- Class-independent switches
- Access Concentrators
- Scalable TDM-Based Architectures
- Digital Loop Carriers

Device Overview

The ZL50063 has two data ports, the Backplane and the Local port. Both the Backplane and Local ports operate at 32.768Mbps.

The ZL50063 contains two data memory blocks (Backplane and Local) to provide the following switching path configurations:

- Input-to-Output Unidirectional, supporting 16K x 16K switching
- Backplane-to-Local Bi-directional, supporting 8K x 8K data switching,
- Local-to-Backplane Bi-directional, supporting 8K x 8K data switching,
- Backplane-to-Backplane Bi-directional, supporting 8K x 8K data switching.
- Local-to-Local Bi-directional, supporting 8K x 8K data switching.

The device contains two connection memory blocks, one for the Backplane output and one for the Local output. Data to be output on the serial streams may come from either of the data memories (Connection Mode) or directly from the connection memory contents (Message Mode).

In Connection Mode, the contents of the connection memory define, for each output stream and channel, the source stream and channel (stored in data memory) to be switched.

In Message Mode, microprocessor data can be written to the connection memory for broadcast on the output streams on a per channel basis. This feature is useful for transferring control and status information to external circuits or other ST-BUS devices.

The device uses a master frame pulse ($\overline{\text{FP8i}}$) and master clock ($\overline{\text{C8i}}$) to define the input frame boundary and timing for both the Backplane port and the Local port. The device will automatically detect whether an ST-BUS or a GCI-Bus style frame pulse is being used. There is a two-frame delay from the time $\overline{\text{RESET}}$ is de-asserted to the establishment of full switch functionality. During this period, the input frame pulse format is determined before switching begins.

The device provides $\overline{\text{FP8o}}$, $\overline{\text{FP16o}}$, $\overline{\text{C8o}}$ and $\overline{\text{C16o}}$ outputs to support external devices connected to the outputs of the Backplane and Local ports.

A non-multiplexed Motorola microprocessor port allows programming of the various device operation modes and switching configurations. The microprocessor port provides access for Register read/write, Connection Memory read/write and Data Memory read-only operations. The port has a 15-bit address bus, 16-bit data bus and 4 control signals. The microprocessor may monitor channel data in the Backplane and Local data memories.

The mandatory requirements of the IEEE-1149.1 (JTAG) standard are fully supported via a dedicated test port.

The ZL50063 is available in one package:

- a 15mm x 15mm body, 1mm ball-pitch, 196-PBGA.

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Pinout Diagram: (as viewed through top of package)

A1 corner identified by metallized marking, mold indent, ink dot, or right-angled corner.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	BSTo1	BSTo2	A4	A5	A8	A9	A12	A13	R/$\overline{W}$	$\overline{CS}$	TMS	TDo	IC_ OPEN	$\overline{TRST}$
B	A0	BSTo5	BSTo0	A1	A2	A7	A11	A14	ODE	TDi	TCK	IC_ OPEN	LSTo0	LSTo1
C	IC_GND	BSTo7	BSTo8	BSTo3	BSTo4	A6	A10	$\overline{DS}$	$\overline{RESET}$	IC_ OPEN	IC_GND	IC_ OPEN	IC_GND	LSTo3
D	IC_GND	BSTo6	BSTo10	GND	A3	VDD_IO	VDD_IO	VDD_IO	$\overline{DTA}$	VDD_IO	GND	LSTo4	LSTo6	LSTo2
E	BSTo12	BSTo11	BSTo13	VDD_IO	GND	VDD_ CORE	VDD_ CORE	VDD_ CORE	VDD_ CORE	GND	VDD_IO	LSTo8	LSTo7	LSTo5
F	BSTo9	BSTo14	BSTo15	VDD_IO	VDD_ CORE	GND	GND	GND	GND	VDD_ CORE	VDD_IO	LSTo12	LSTo13	LSTo9
G	BSTi0	BORS	VDD_ CORE	VDD_IO	VDD_ CORE	GND	GND	GND	GND	VDD_ CORE	VDD_IO	LSTo11	LSTo15	LSTo10
H	BSTi1	BSTi2	BSTi3	VDD_IO	VDD_ CORE	GND	GND	GND	GND	VDD_ CORE	VDD_IO	VDD_ CORE	LORS	LSTo14
J	BSTi4	BSTi5	BSTi7	VDD_IO	VDD_ CORE	GND	GND	GND	GND	VDD_ CORE	VDD_IO	LSTi5	LSTi1	LSTi2
K	BSTi6	BSTi9	BSTi13	VDD_IO	GND	VDD_ CORE	VDD_ CORE	VDD_ CORE	VDD_ CORE	GND	VDD_IO	LSTi15	LSTi3	LSTi0
L	BSTi8	BSTi11	BSTi14	GND	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	GND	LSTi14	LSTi8	LSTi6
M	BSTi10	BSTi15	D15	D14	D12	D5	IC_GND	IC_GND	$\overline{C16o}$	$\overline{FP8i}$	LSTi13	LSTi10	LSTi7	LSTi4
N	BSTi12	D13	D10	D11	D7	D3	D0	IC_GND	VDD_ PLL	$\overline{C8o}$	$\overline{FP8o}$	LSTi11	LSTi12	LSTi9
P	GND	D9	D8	D6	D4	D2	D1	IC_GND	IC_ OPEN	$\overline{C8i}$	IC_ OPEN	$\overline{FP16o}$	GND	GND

Figure 2 - ZL50063 PBGA Connections (196 PBGA, 15mm x 15mm) Pin Diagram
(as viewed through top of package)

Pin Description

Pin Name	ZL50063 Package Coordinates (196-ball PBGA)	Description
Device Timing		
C8i	P10	**Master Clock (5V Tolerant Schmitt-Triggered Input).** This pin accepts an 8.192MHz clock. The internal frame boundary is aligned with the clock falling or rising edge, as controlled by the C8IPOL bit in the Control Register. Input data on both the Backplane and Local sides (BSTi0-15 and LSTi0-15) must be aligned to this clock and the accompanying input frame pulse, FP8i.
FP8i	M10	**Frame Pulse Input (5V Tolerant Schmitt-Triggered Input)**. When the Frame Pulse Width bit (FPW) of the Control Register is LOW (default), this pin accepts a 122ns-wide frame pulse. When the FPW bit is HIGH, this pin accepts a 244ns-wide frame pulse. The device will automatically detect whether an ST-BUS or GCI-Bus style frame pulse is applied. Input data on both the Backplane and Local sides (BSTi0-15 and LSTi0-15) must be aligned to this frame pulse and the accompanying input clock, C8i.
C8o	N10	**C8o Output Clock (5V Tolerant Three-state Output).** This pin outputs an 8.192MHz clock generated within the device. The clock falling edge or rising edge is aligned with the output frame boundary presented on FP8o; this edge polarity alignment is controlled by the COPOL bit of the Control Register. Output data on both the Backplane and Local sides (BSTo0-15 and LSTo0-15) will be aligned to this clock and the accompanying output frame pulse, FP8o.
FP8o	N11	**Frame Pulse Output (5V Tolerant Three-state Output).** When the Frame Pulse Width bit (FPW) of the Control Register is LOW (default), this pin outputs a 122ns-wide frame pulse. When the FPW bit is HIGH, this pin outputs a 244ns-wide frame pulse. The frame pulse, running at 8kHz rate, will have the same format (ST-BUS or GCI-Bus) as the input frame pulse (FP8i). Output data on both the Backplane and Local sides (BSTo0-15 and LSTo0-15) will be aligned to this frame pulse and the accompanying output clock, C8o.
C16o	M9	**C16o Output Clock (5V Tolerant Three-state Output).** This pin outputs a 16.384MHz clock generated within the device. The clock falling edge or rising edge is aligned with the output frame boundary presented on FP16o; this edge polarity alignment is controlled by the COPOL bit of the Control Register. Output data on both the Backplane and Local sides (BSTo0-15 and LSTo0-15) will be aligned to this clock and the accompanying output frame pulse, FP16o.
FP16o	P12	**Frame Pulse Output (5V Tolerant Three-state Output).** When the Frame Pulse Width bit (FPW) of the Control Register is LOW (default), this pin outputs a 61ns-wide frame pulse. When the FPW bit is HIGH, this pin outputs a 122ns-wide frame pulse. The frame pulse, running at 8kHz rate, will have the same format (ST-BUS or GCI-Bus) as the input frame pulse (FP8i). Output data on both the Backplane and Local sides (BSTo0-15 and LSTo0-15) will be aligned to this frame pulse and the accompanying output clock, C16o.

Pin Description (continued)

Pin Name	ZL50063 Package Coordinates (196-ball PBGA)	Description
Backplane and Local Inputs		
BSTi0-7	G1, H1, H2, H3, J1, J2, K1, J3	**Backplane Serial Input Streams 0 to 7 (5V Tolerant Inputs with Internal Pull-downs).** These pins accept serial TDM data streams at a fixed data rate of 32.768Mbps (with 512 channels per stream).
BSTi8-15	L1, K2, M1, L2, N1, K3, L3, M2	**Backplane Serial Input Streams 8 to 15 (5V Tolerant Inputs with Internal Pull-downs).** These pins accept serial TDM data streams at a fixed data rate of 32.768Mbps (with 512 channels per stream).
LSTi0-7	K14, J13, J14, K13, M14, J12, L14, M13	**Local Serial Input Streams 0 to 7 (5V Tolerant Inputs with Internal Pull-downs).** These pins accept serial TDM data streams at a fixed data rate of 32.768Mbps (with 512 channels per stream).
LSTi8-15	L13, N14, M12, N12, N13, M11, L12, K12	**Local Serial Input Streams 8 to 15 (5V Tolerant Inputs with Internal Pull-downs).** These pins accept serial TDM data streams at a fixed data rate of 32.768Mbps (with 512 channels per stream).
Backplane and Local Outputs and Control		
ODE	B9	**Output Drive Enable (5V Tolerant Input with Internal Pull-up)**. An asynchronous input providing Output Enable control to the BSTo0-15 and LSTo0-15 outputs. When LOW, the BSTo0-15 and LSTo0-15 outputs are driven HIGH or high impedance (dependent on the **BORS** and **LORS** pin settings respectively). When HIGH, the outputs BSTo0-15 and LSTo0-15 are enabled.
BORS	G2	**Backplane Output Reset State (5V Tolerant Input with Internal Pull-down)**. When this input is LOW, the device will initialize with the BSTo0-15 outputs driven high. Following initialization, the Backplane stream outputs are always active. When this input is HIGH, the device will initialize with the BSTo0-15 outputs at high impedance. Following initialization, the Backplane stream outputs may be set active or high impedance using the **ODE** pin or on a per-channel basis with the **BE** bit in the Backplane Connection Memory.
BSTo0-7	B3, A1, A2, C4, C5, B2, D2, C2	**Backplane Serial Output Streams 0 to 7 (5V Tolerant, Three-state Outputs with Slew-Rate Control).** These pins output serial TDM data streams at a fixed data rate of 32.768Mbps (with 512 channels per stream). Refer to the descriptions of the **BORS** and **ODE** pins for control of the output HIGH or high impedance state.

Pin Description (continued)

Pin Name	ZL50063 Package Coordinates (196-ball PBGA)	Description
BSTo8-15	C3, F1, D3, E2, E1, E3, F2, F3	**Backplane Serial Output Streams 8 to 15 (5V Tolerant, Three-state Outputs with Slew-Rate Control).** These pins output serial TDM data streams at a fixed data rate of 32.768Mbps (with 512 channels per stream). Refer to the descriptions of the **BORS** and **ODE** pins for control of the output HIGH or high impedance state.
LORS	H13	**Local Output Reset State (5V Tolerant Input with Internal Pull-down)**. When this input is LOW, the device will initialize with the LSTo0-15 outputs driven high. Following initialization, the Local stream outputs are always active. When this input is HIGH, the device will initialize with the LSTo0-15 outputs at high impedance. Following initialization, the Local stream outputs may be set active or high impedance using the **ODE** pin or on a per-channel basis with the **LE** bit in the Local Connection Memory.
LSTo0-7	B13, B14, D14, C14, D12, E14, D13, E13	**Local Serial Output Streams 0 to 7 (5V Tolerant Three-state Outputs with Slew-Rate Control).** These pins output serial TDM data streams at a fixed data rate of 32.768Mbps (with 512 channels per stream). Refer to the descriptions of the **LORS** and **ODE** pins for control of the output HIGH or high impedance state.
LSTo8-15	E12, F14, G14, G12, F12, F13, H14, G13	**Local Serial Output Streams 8 to 15 (5V Tolerant Three-state Outputs with Slew-Rate Control).** These pins output serial TDM data streams at a fixed data rate of 32.768Mbps (with 512 channels per stream). Refer to the descriptions of the **LORS** and **ODE** pins for control of the output HIGH or high impedance state.
Microprocessor Port Signals		
A0 - A14	B1, B4, B5, D5, A3, A4, C6, B6, A5, A6, C7, B7, A7, A8, B8	**Address 0 - 14 (5V Tolerant Inputs).** These pins form the 15-bit address bus to the internal memories and registers. A0 = LSB
D0 - D15	N7, P7, P6, N6, P5, M6, P4, N5, P3, P2, N3, N4, M5, N2, M4, M3	**Data Bus 0 - 15 (5V Tolerant Inputs/Outputs with Slew-Rate Control).** These pins form the 16-bit data bus of the microprocessor port. D0 = LSB
$\overline{CS}$	A10	**Chip Select (5V Tolerant Input).** Active LOW input used by the microprocessor to enable the microprocessor port access. **Note that a minimum of 30ns must separate the de-assertion of DTA (to high) and the assertion of CS and/or DS to initiate the next access.**

Pin Description (continued)

Pin Name	ZL50063 Package Coordinates (196-ball PBGA)	Description
$\overline{DS}$	C8	**Data Strobe (5V Tolerant Input).** This active LOW input works in conjunction with $\overline{CS}$ to enable the microprocessor port read and write operations. **Note that a minimum of 30ns must separate the de-assertion of DTA (to high) and the assertion of CS and/or DS to initiate the next access.**
R/$\overline{W}$	A9	**Read/Write (5V Tolerant Input).** This input controls the direction of the data bus lines (D0-D15) during a microprocessor access.
$\overline{DTA}$	D9	**Data Transfer Acknowledgment (5V Tolerant Three-state Output).** This active LOW output indicates that a data bus transfer is complete. A pull-up resistor is required to hold a HIGH level. **Note that a minimum of 30ns must separate the de-assertion of DTA (to high) and the assertion of CS and/or DS to initiate the next access.**
$\overline{RESET}$	C9	**Device Reset (5V Tolerant Input with Internal Pull-up).** This input (active LOW) asynchronously applies reset and synchronously releases reset to the device. In the reset state, the outputs LSTo0-15 and BSTo0-15 are set to a HIGH or high impedance state, depending on the state of the LORS and BORS external control pins, respectively. The assertion of this pin also clears the device registers and internal counters. **Refer to Section 7.3 on page 25 for the timing requirements regarding this reset signal**.
JTAG Control Signals		
TCK	B11	**Test Clock (5V Tolerant Input).** Provides the clock to the JTAG test logic.
TMS	A11	**Test Mode Select (5V Tolerant Input with Internal Pull-up).** JTAG signal that controls the state transitions of the TAP controller.
TDi	B10	**Test Serial Data In (5V Tolerant Input with Internal Pull-up).** JTAG serial test instructions and data are shifted in on this pin.
TDo	A12	**Test Serial Data Out (5V Tolerant Three-state Output).** JTAG serial data is output on this pin on the falling edge of TCK. This pin is held in a high impedance state when JTAG is not enabled.
$\overline{TRST}$	A14	**Test Reset (5V Tolerant Input with Internal Pull-up).** Asynchronously initializes the JTAG TAP controller to the Test-Logic-Reset state. This pin must be pulsed LOW during power-up for JTAG testing. This pin must be held LOW for normal functional operation of the device.

Pin Description (continued)

Pin Name	ZL50063 Package Coordinates (196-ball PBGA)	Description
Power and Ground Pins		
V_{DD_IO}	D6, D7, D8, D10, E4, E11, F4, F11, G4, G11, H4, H11, J4, J11, K4, K11, L5, L6, L7, L8, L9, L10	**Power Supply for Periphery Circuits:** +3.3V
V_{DD_CORE}	E6, E7, E8, E9, F5, F10, G3, G5, G10, H5, H10, H12, J5, J10, K6, K7, K8, K9	**Power Supply for Core Circuits:** +1.8V
V_{DD_PLL}	N9	**Power Supply for Analog PLL:** +1.8V
V_{SS} (GND)	D4, D11, E5, E10, F6, F7, F8, F9, G6, G7, G8, G9, H6, H7, H8, H9, J6, J7, J8, J9, K5, K10, L4, L11, P1, P13, P14	**Ground.**
Unused Pins		
IC_OPEN	A13, B12, C10, C12, P9, P11	**Internal Connections - OPEN.** These pins must be left unconnected.
IC_GND	C1, C11, C13, D1, M7, M8, N8, P8	**Internal Connections - GND.** These pins must be tied LOW.

1.0 Unidirectional and Bi-directional Switching Applications

The ZL50063 has a maximum capacity of 16,384 input channels and 16,384 output channels. This is calculated from the number of streams and channels: 32 input streams (16 Backplane, 16 Local) at 32.768Mbps and 32 output streams (16 Backplane, 16 Local) at 32.768Mbps, with each stream providing 512 channels.

A typical mode of operation is to separate the input and output streams to form a unidirectional switch, as shown in Figure 3 below.

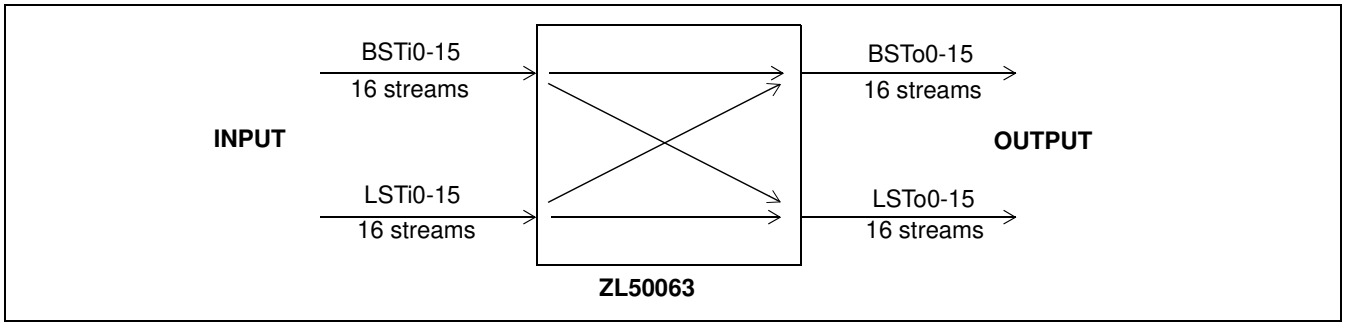

Figure 3 - 16,384 x 16,384 Channels (32Mbps), Unidirectional Switching

In this system, the Backplane and Local input streams are combined, and the Backplane and Local output streams are combined, so that the switch appears as a 32 input stream by 32 output stream switch. This gives the maximum 16,384 x 16,384 channel capacity.

Often a system design needs to differentiate between a Backplane and a Local side, or it needs to put the switch in a bi-directional configuration. In this case, the ZL50063 can be used as shown in Figure 4 to give 8,192 x 8,192 channel bi-directional capacity.

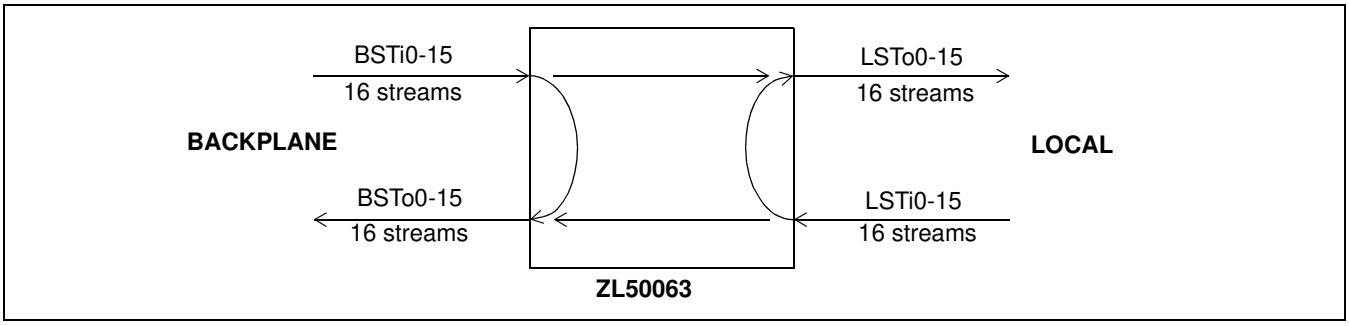

Figure 4 - 8,192 x 8,192 Channels (32Mbps), Bi-directional Switching

In this system setup, the chip has a capacity of 8,192 input channels and 8,192 output channels on the Backplane side, as well as 8,192 input channels and 8,192 output channels on the Local side. Note that some or all of the output channels on one side can come from the other side, e.g., Backplane input to Local output switching.

1.1 Flexible Configuration

The ZL50063 can be configured as an 16K by 16K non-blocking unidirectional digital switch, a 8K by 8K non-blocking bi-directional digital switch, or as a blocking switch with various switching capacities.

1.1.1 Non-Blocking Unidirectional Configuration (Typical System Configuration)

Because the input and output drivers are synchronous, the user can combine input Backplane streams and input Local streams as well as output Backplane streams and output Local streams to increase the total number of input and output streams of the switch in a unidirectional configuration, as shown in Figure 3.

- 16,384-channel x 16,384-channel non-blocking switching from input to output streams

1.1.2 Non-Blocking Bi-directional Configuration

Another typical application is to configure the ZL50063 as a non-blocking 8K by 8K bi-directional switch, as shown in Figure 4:

- 8,192-channel x 8,192-channel non-blocking switching from Backplane input to Local output streams
- 8,192-channel x 8,192-channel non-blocking switching from Local input to Backplane output streams
- 8,192-channel x 8,192-channel non-blocking switching from Backplane input to Backplane output streams
- 8,192-channel x 8,192-channel non-blocking switching from Local input to Local output streams

1.1.3 Blocking Bi-directional Configuration

The ZL50063 can be configured as a blocking bi-directional switch if it is an application requirement. For example, it can be configured as a 12K by 4K bi-directional blocking switch, as shown in Figure 5:

- 12,288-channel x 4,096-channel blocking switching from Backplane input to Local output streams
- 4,096-channel x 12,288-channel blocking switching from Local input to Backplane output streams
- 12,288-channel x 12,288-channel non-blocking switching from Backplane input to Backplane output streams
- 4,096-channel x 4,096-channel non-blocking switching from Local input to Local output streams

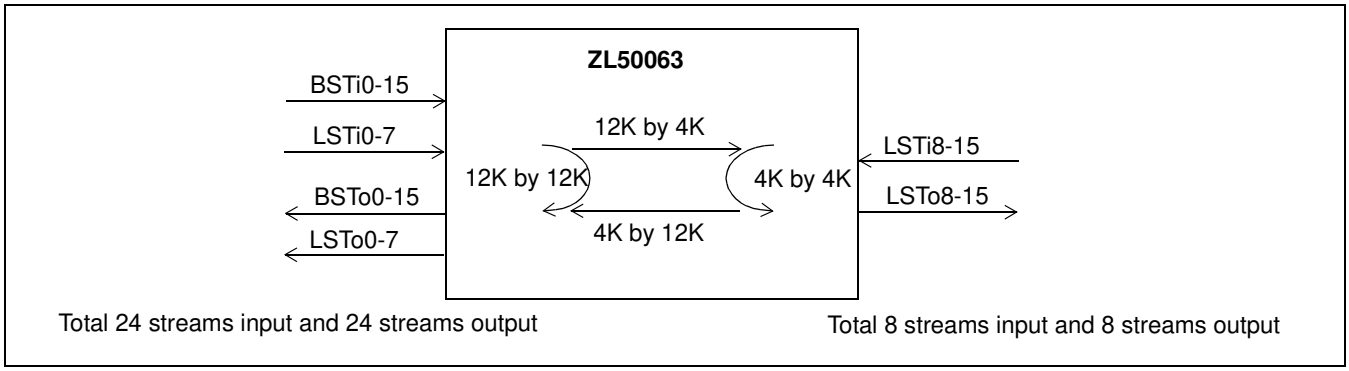

Figure 5 - 12,288 by 4,096 Channels Blocking Bi-directional Configuration

2.0 Functional Description

2.1 Switching Configuration

The device supports five switching configurations: (1) Unidirectional switch, (2) Backplane-to-Local, (3) Local-to-Backplane, (4) Backplane-to-Backplane, and (5) Local-to-Local. The following sections describe the switching paths in detail. Configurations (2) - (5) enable a non-blocking bi-directional switch with 8,192 Backplane input/output channels at Backplane stream data rates of 32.768Mbps, and 8,192 Local input/output channels at Local stream data rates of 32.768Mbps. The switching paths of configurations (2) to (5) may be operated simultaneously.

2.1.1 Unidirectional Switch

The device can be configured as a 16,384 x 16,384 unidirectional switch by grouping together all input streams and all output streams. All streams operate at a data rate of 32.768Mbps.

2.1.2 Backplane-to-Local Path

The device can provide data switching between the Backplane input port and the Local output port. The Local Connection Memory determines the switching configurations.

2.1.3 Local-to-Backplane Path

The device can provide data switching between the Local input port and the Backplane output port. The Backplane Connection Memory determines the switching configurations.

2.1.4 Backplane-to-Backplane Path

The device can provide data switching between the Backplane input and output ports. The Backplane Connection Memory determines the switching configurations.

2.1.5 Local-to-Local Path

The device can provide data switching between the Local input and output ports. The Local Connection Memory determines the switching configurations.

2.1.6 Port Operation

The Local port has 16 input (LSTi0-15) and 16 output (LSTo0-15) data streams. Similarly, the Backplane port has 16 input (BSTi0-15) and 16 output (BSTo0-15) data streams. All the streams operate at 32.768Mbps. The timing of the input and output clocks and frame pulses is shown in Figure 7, “Input and Output (Generated) Frame Pulse Alignment for Different Data Rates” on page 18. The input traffic are aligned based on the FP8i and C8i input timing signals, while the output traffic are aligned based on the FP8o and C8o output timing signals.

2.1.6.1 Local Output Port

Operation of stream data in Connection Mode or Message Mode is determined by the state of the LMM bit of the Local Connection Memory. The channel high impedance state is controlled by the LE bit of the Local Connection Memory. The data source (i.e. from the Local or Backplane Data Memory) is determined by the LSRC bit of the Local Connection Memory. Refer to Section 8.1, Local Connection Memory, and Section 11.3, Local Connection Memory Bit Definition for more details.

2.1.6.2 Backplane Output Port

Operation of stream data in Connection Mode or Message Mode is determined by the state of the BMM bit of the Backplane Connection Memory and the channel high impedance state is controlled by the BE bit of the Backplane Connection Memory. The data source (i.e. from the Local or Backplane Data Memory) is determined by the BSRC bit of the Backplane Connection Memory. Refer to Section 8.2, Backplane Connection Memory and Section 11.4, Backplane Connection Memory Bit Definition for more details.

2.2 Frame Pulse Input and Master Input Clock Timing

The input frame pulse ($\overline{FP8i}$) is an 8kHz input signal active for 122ns or 244ns at the frame boundary. The FPW bit in the Control Register must be set according to the applied pulse width. See Pin Description and Table 11, “Control Register Bits” on page 32, for details.

The active state and timing of $\overline{FP8i}$ can conform either to the ST-BUS or to the GCI-Bus as shown in Figure 6, ST-BUS and GCI-Bus Input Timing Diagram. The ZL50063 device will automatically detect whether an ST-BUS or a GCI-Bus style frame pulse is being used for the master frame pulse ($\overline{FP8i}$). The output frame pulses ($\overline{FP8o}$ and $\overline{FP16o}$) are always of the same style (ST-BUS or GCI-Bus) as the input frame pulse. The active edge of the input clock ($\overline{C8i}$) shall be selected by the state of the Control Register bit C8IPOL.

Note that the active edge of ST-BUS is falling edge, which is the default mode of the device, while GCI-Bus uses rising edge as the active edge. Although GCI frame pulse will be automatically detected, to fully conform to GCI-Bus operation, the device should be set to use $\overline{C8i}$ rising edge as the active edge (by setting bit C8IPOL HIGH) when GCI-Bus is used.

For the purposes of describing the device operation, the remaining part of this document assumes the ST-BUS frame pulse format with a single width frame pulse of 122ns and a falling active clock-edge, unless explicitly stated otherwise.

In addition, the device provides $\overline{FP8o}$, $\overline{FP16o}$, $\overline{C8o}$ and $\overline{C16o}$ outputs to support external devices which connect to the output ports. The generated frame pulses ($\overline{FP8o}$, $\overline{FP16o}$) will be provided in the same format as the master frame pulse ($\overline{FP8i}$). The polarity of $\overline{C8o}$ and $\overline{C16o}$, at the frame boundary, can be controlled by the Control Register bit, COPOL. An analog phase lock loop (APLL) is used to multiply the input clock frequency on $\overline{C8i}$ to generate an internal clock signal operating at 131.072MHz.

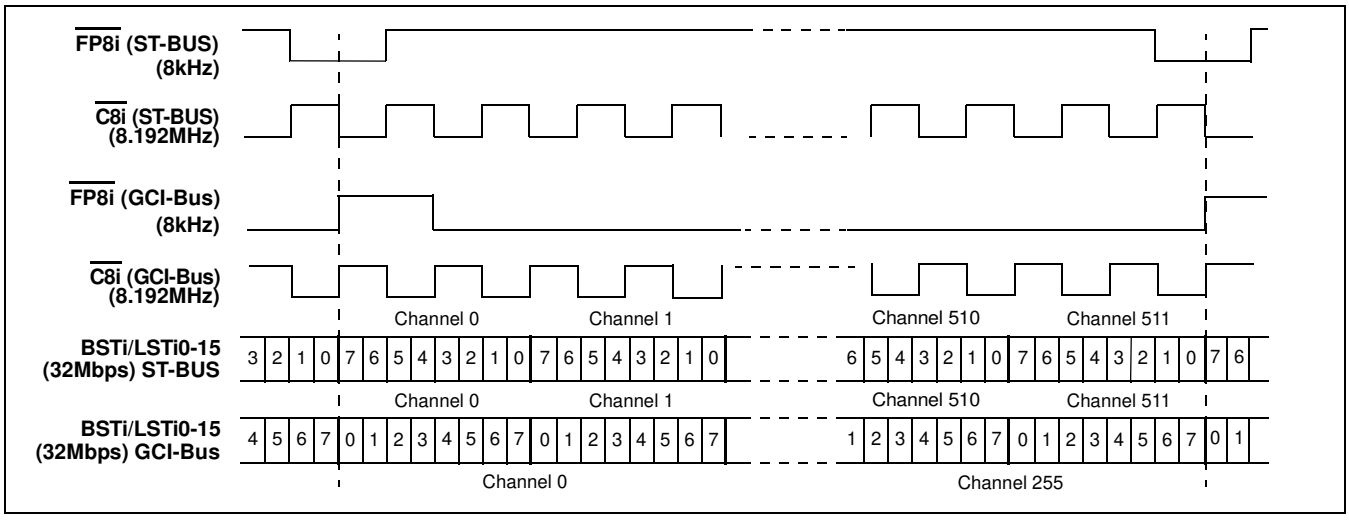

Figure 6 - ST-BUS and GCI-Bus Input Timing Diagram

2.3 Input Frame Pulse and Generated Frame Pulse Alignment

The ZL50063 accepts a frame pulse ($\overline{FP8i}$) and generates two frame pulse outputs, $\overline{FP8o}$ and $\overline{FP16o}$, which are aligned to the master frame pulse. There is a constant throughput delay for data being switched from the input to the output of the device such that data which is input during Frame N is output during Frame N+2.

For further details of frame pulse conditions and options, see Section 13.1, Control Register (CR), Figure 15, Frame Boundary Conditions, ST-BUS Operation, and Figure 16, Frame Boundary Conditions, GCI-Bus Operation.

Figure 7 - Input and Output (Generated) Frame Pulse Alignment for Different Data Rates

The t_{FBOS} is the offset between the input frame pulse, $\overline{FP8i}$, and the generated output frame pulse, $\overline{FP8o}$. Refer to the “AC Electrical Characteristics,” on page 47. Note that although the figure above shows the traditional setups of the frame pulses and clocks for both ST-BUS and GCI-Bus configurations, the devices can be configured to accept/generate double-width frame pulses (if the FPW bit in the Control Register is set) as well as to use the opposite clock edge for frame-boundary determination (using the C8IPOL and COPOL bits in the Control Register). See the timing diagrams in “AC Electrical Characteristics,” on page 47 for all of the available configurations.

2.4 Jitter Tolerance Improvement Circuit - Frame Boundary Discriminator

To improve the jitter tolerance of the ZL50063, a Frame Boundary Discriminator (FBD) circuit was added to the device. This circuit is enabled by setting the Control Register bit FBDEN to HIGH. By default the FBD is disabled.

The FBD can operate in two modes, as controlled by the FBD_MODE[2:0] bits of the Control Register. When bits FBD_MODE[2:0] are set to 000_B, the FBD is set to handle lower frequency jitter only (<8kHz). When bits FBD_MODE[2:0] are set to 111_B, the FBD can handle both low frequency and high frequency jitter. All other values are reserved. These bits are ignored when bit FBDEN is LOW. It is strongly recommended that if bit FBDEN is set HIGH, bits FBD_MODE[2:0] should be set to 111_B to improve the high frequency jitter handling capability.

To achieve the best jitter tolerance performance, it is also recommended that the input data sampling point be optimized. In most applications, the optimum sampling point is 1/2 instead of the default 3/4 (it can be changed by programming all the LIDR and BIDR registers). This will give more allowance for sampling point variations caused by jitter. There are, however, some cases where data experience more delay than the timing signals. A common example is when multiple data lines are tied together to form bidirectional buses. The large bus loading may cause data to be delayed. If this is the case, the optimum sampling point may be 3/4 or 4/4 instead of 1/2. The optimum sampling point is dependent on the application. The user should optimize the sampling point to achieve the best jitter tolerance performance.

2.5 Input Clock Jitter Tolerance

Jitter tolerance can not be accurately represented by just one number. Jitter of the same amplitude but different frequency spectrum can have different effect on the operation of a device. For example, a device that can tolerate 20ns of jitter of 10kHz frequency may only be able to tolerate 10ns of jitter of 1MHz frequency. Therefore, jitter tolerance should be represented as a spectrum over frequency. The highest possible jitter frequency is half of the carrier frequency. In the case of the ZL50063, the input clock is 8.192MHz, and the jitter associated with this clock can have the highest frequency component at 4.096MHz.

For the above reasons, jitter tolerance of the ZL50063 has been characterized at 32.768Mbps. Tolerance of jitter of different frequencies are shown in the “AC Electrical Characteristics“ section, table “Input Clock Jitter Tolerance“ on page 55. The Jitter Tolerance Improvement Circuit was enabled (Control Register, bit FBDEN set HIGH, and bits FBD_MODE[2:0] set to 111_B), and the sampling point was optimized.

3.0 Input and Output Offset Programming

Various registers are used to control the input sampling point (delay) and the output advancement for the Local and Backplane streams. The following sections explain the details of these offset programming features.

3.1 Input Offsets

Control of the Input Bit Delay allows each input stream to have a different frame boundary with respect to the master frame pulse, $\overline{FP8i}$. Each input stream can be individually delayed by up to 7 3/4 bits with a resolution of 1/4 bit of the bit period.

3.1.1 Input Bit Delay Programming (Backplane and Local Input Streams)

Input Bit Delay Registers LIDR0 - 15 and BIDR0 - 15 work in conjunction with the SMPL_MODE bit in the Control Register to allow users to control input bit fractional delay as well as input bit sample point selection for greater flexibility when designing switch matrices for high speed operation.

When SMPL_MODE = LOW (input bit fractional delay mode), bits LID[4:0] and BID[4:0] in the LIDR0 - 15 and BIDR0 - 15 registers respectively define the input bit fractional delay of the corresponding local and backplane stream. The total delay can be up to 7 3/4 bits with a resolution of 1/4 bit at the selected data rate. When SMPL_MODE = HIGH (sampling point select mode), bits LID[1:0] and BID[1:0] define the input bit sampling point of the stream. The sampling point can be programmed at the 3/4, 4/4, 1/4 or 2/4 bit location to allow better tolerance for input jitter. Bits LID[4:2] and BID[4:2] define the integer input bit delay, with a maximum value of 7 bits at a resolution of 1 bit.

Refer to Figure 8 for Input Bit Delay Timing at 32Mbps data rates.

Refer to Figure 9 for Input Sampling Point Selection Timing at 32Mbps data rates.

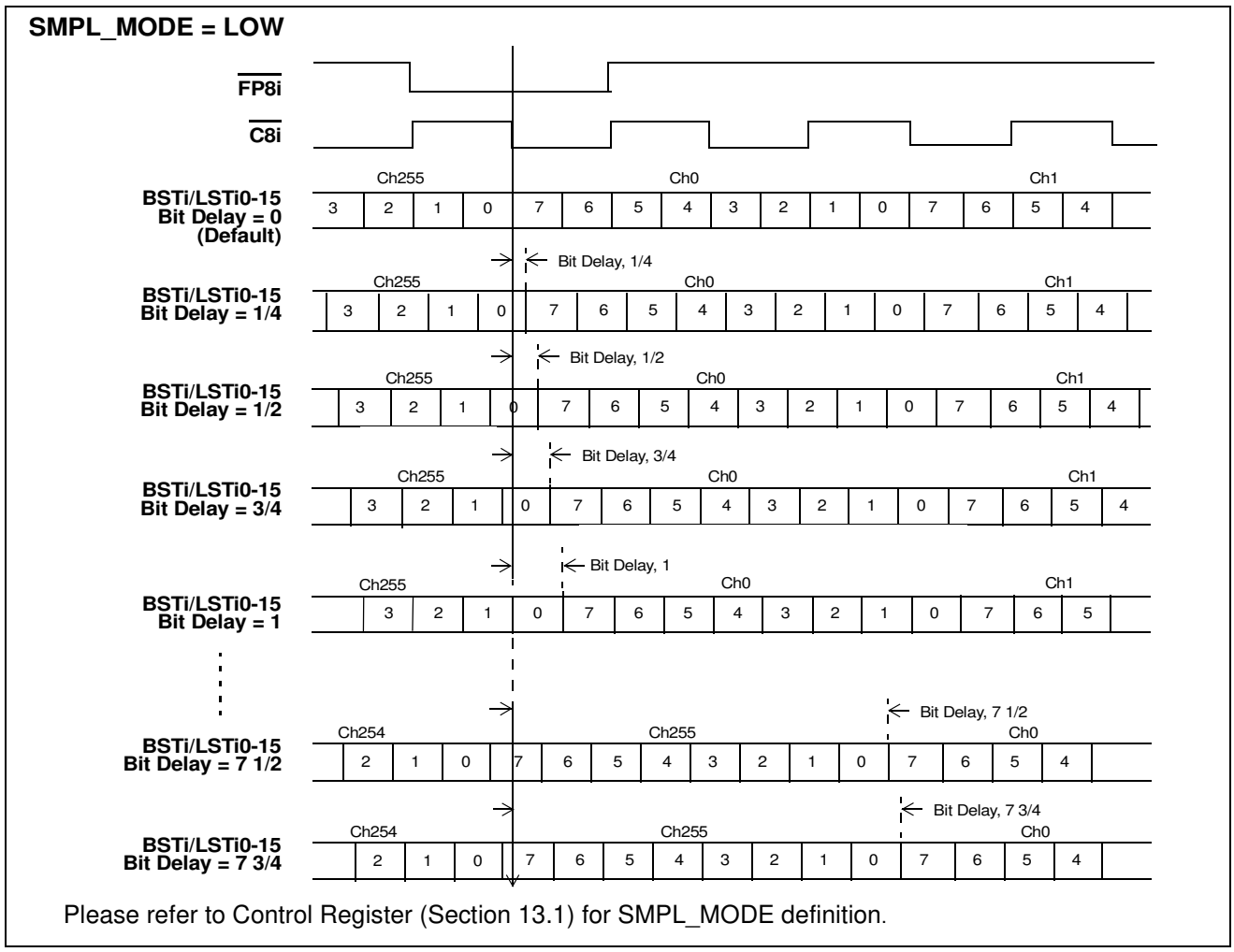

Figure 8 - Backplane and Local Input Bit Delay Timing Diagram for Data Rate of 32Mbps

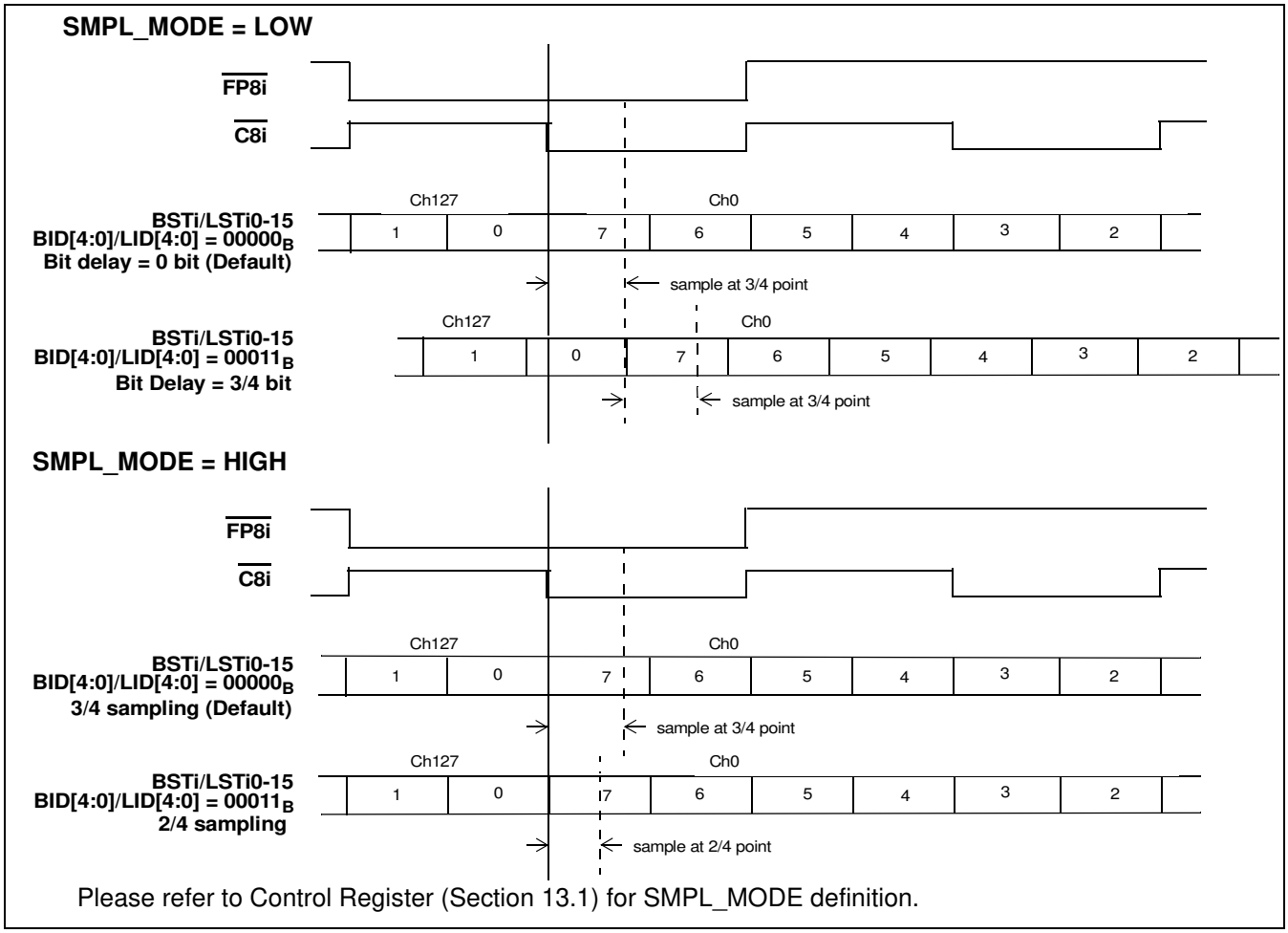

Figure 9 - Backplane and Local Input Bit Delay or Sampling Point Selection Timing Diagram for Data Rate of 32Mbps

3.2 Output Advancement Programming (Backplane and Local Output Streams)

This feature is used to advance the output channel alignment of individual Local or Backplane output streams with respect to the frame boundary FP8o. Each output stream has its own advancement value that can be programmed by the Output Advancement Registers. The output advancement selection is useful in compensating for various parasitic loading on the serial data output pins.

The Local and Backplane Output Advancement Registers, LOAR0 - LOAR15 and BOAR0 - BOAR15, are used to control the Local and Backplane output advancement respectively. The advancement is determined with reference to the internal system clock rate (131.072MHz). The advancement can be 0, -1 cycle, -2 cycles or -3 cycles, which converts to approximately 0ns, -7.6ns, -15ns or -23ns as shown in Figure 10.

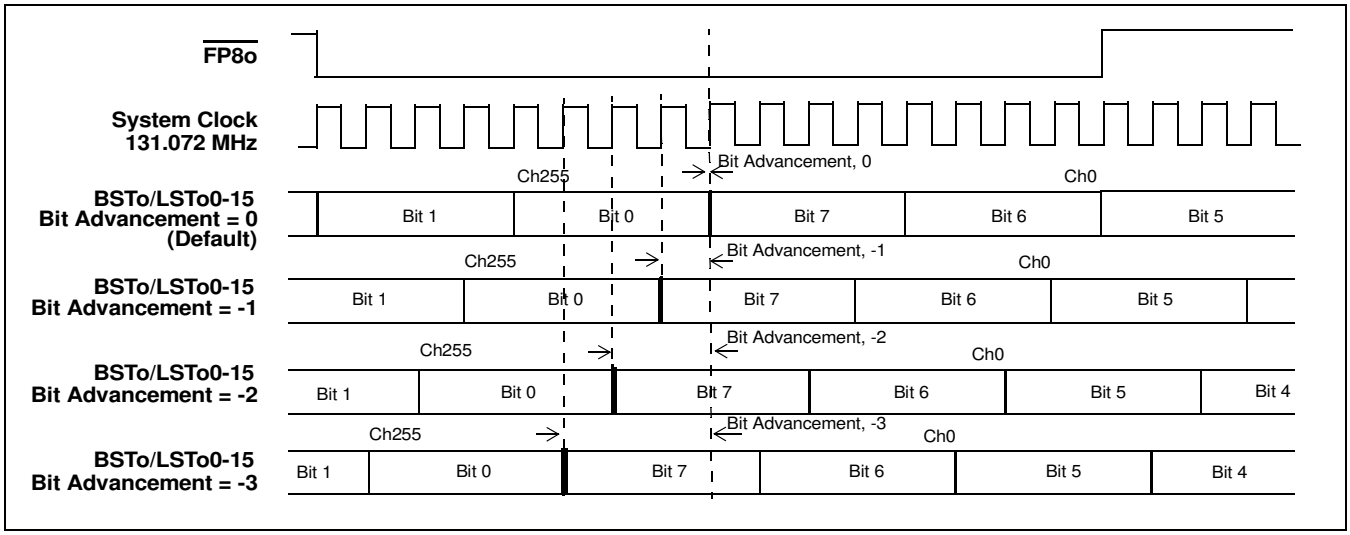

Figure 10 - Local and Backplane Output Advancement Timing Diagram for Data Rate of 32Mbps

4.0 Port High-Impedance Control

The input pins, **LORS** and **BORS**, select whether the Local (**LSTo0-15**) and Backplane (**BSTo0-15**) output streams, respectively, are set to high impedance at the output of the device itself, or are always driven (active HIGH or active LOW).

Setting **LORS**/**BORS** to a LOW state will configure the output streams, **LSTo0-15**/**BSTo0-15,** to transmit bi-state channel data.

Setting **LORS**/**BORS** to a HIGH state will configure the output streams, **LSTo0-15**/**BSTo0-15,** of the device to invoke a high impedance output on a per-channel basis. The Local/Backplane Output Enable Bit (**LE**/**BE**) of the Local/Backplane Connection Memory has direct per-channel control on the high impedance state of the Local/Backplane output streams, **L**/**BSTo0-15**. Programming a LOW state in the connection memory LE/BE bit will set the stream output of the device to high impedance for the duration of the channel period. See “Local Connection Memory Bit Definition,” on page 30 and “Backplane Connection Memory Bit Definition,” on page 31 for programming details.

The state of the **LORS**/**BORS** pin is detected and the device configured accordingly during a **$\overline{\text{RESET}}$** operation, e.g. following power-up. The **LORS**/**BORS** pin is an asynchronous input and is expected to be hard-wired for a particular system application, although it may be driven under logic control if preferred.

The Local/Backplane output enable control in order of highest priority is: $\overline{\text{RESET}}$, ODE, OSB, LE/BE.

$\overline{\text{RESET}}$ (input pin)	**ODE (input pin)**	**OSB (Control Register bit)**	**LE/BE (Local / Backplane Connection Memory bit)**	**LORS/BORS (input pin)**	**LSTo0-15/ BSTo0-15**
0	X	X	X	0	HIGH
0	X	X	X	1	HI-Z
1	0	X	X	0	HIGH
1	0	X	X	1	HI-Z
1	1	0	X	0	HIGH

Table 1 - Local and Backplane Output Enable Control Priority

$\overline{\text{RESET}}$ (input pin)	ODE (input pin)	OSB (Control Register bit)	LE/BE (Local / Backplane Connection Memory bit)	LORS/BORS (input pin)	LSTo0-15/ BSTo0-15
1	1	0	X	1	HI-Z
1	1	1	0	0	HIGH
1	1	1	0	1	HI-Z
1	1	1	1	X	ACTIVE (HIGH or LOW)

Table 1 - Local and Backplane Output Enable Control Priority (continued)

5.0 Data Delay Through the Switching Paths

Serial data which goes into the device is converted into parallel format and written to consecutive locations in the data memory. Each data memory location corresponds to the input stream and channel number. Channels written to any of the buffers during Frame N will be read out during Frame N+2. The input bit delay and output bit advancement have no impact on the overall data throughput delay.

In the following paragraphs, the data throughput delay (**T**) is represented as a function of ST-BUS frames, input channel number, (**m**), and output channel number (**n**). For 32.768Mbps data rate, there are 512 channels on each stream. The input channel number (**m**) and output channel number (**n**) can therefore have a range of 0 to 511. The data throughput delay under various input channel and output channel conditions can be summarized as:

T = 2 frames + (n - m)

The data throughput delay (**T**) is: **T = 2 frames + (n - m)**. Assuming that **m** (input channel) and **n** (output channel) are equal, we have the figure below, in which the delay between the input data being written and the output data being read is exactly 2 frames.

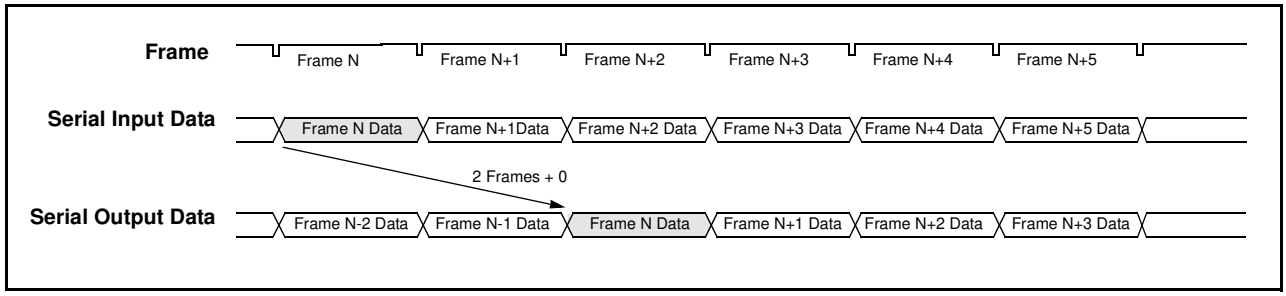

Figure 11 - Data Throughput Delay with Input Ch0 Switched to Output Ch0

Assuming that **n** (output channel) is greater than **m** (input channel), we have the figure below, in which the delay time between the input channel being written and the output channel being read exceeds 2 frames.

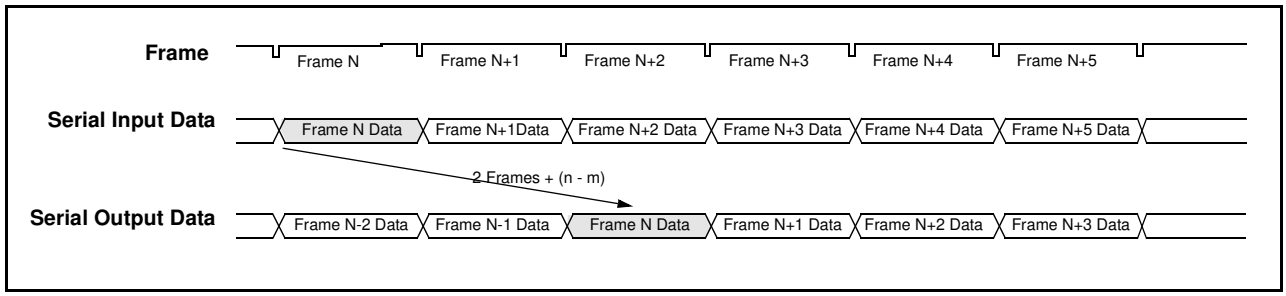

Figure 12 - Data Throughput Delay with Input Ch0 Switched to Output Ch13

Assuming that **n** (output channel) is less than **m** (input channel), we have the figure below, in which the delay time between the input channel being written and the output channel being read is less than 2 frames.

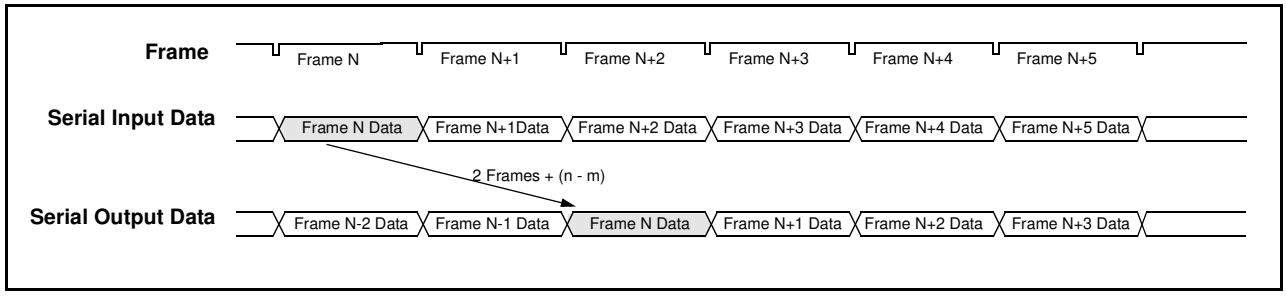

Figure 13 - Data Throughput Delay with Input Ch13 Switched to Output Ch0

6.0 Microprocessor Port

The 16K switch family supports non-multiplexed Motorola type microprocessor buses. The microprocessor port consists of a 16-bit parallel data bus (**D0-15**), a 15-bit address bus (**A0-14**) and four control signals (**CS, DS, R/W** and **DTA**). The data bus provides access to the internal registers, the Backplane Connection and Data Memories, and the Local Connection and Data Memories. Each memory has 8,192 locations. See Table 5, Address Map for Data and Connection Memory Locations (A14 = 1), for the address mapping.

Each Connection Memory can be read or written via the 16-bit microprocessor port. The Data Memories can only be read (but not written) from the microprocessor port.

To prevent the bus 'hanging', in the event of the switch not receiving a master clock, the microprocessor port shall complete the DTA handshake when accessed, but any data read from the bus will be invalid.

7.0 Device Power-up, Initialization and Reset

7.1 Power-Up Sequence

The recommended power-up sequence is for the V_{DD_IO} supply (nominally +3.3V) to be established before the power-up of the V_{DD_PLL} and V_{DD_CORE} supplies (nominally +1.8V). The V_{DD_PLL} and V_{DD_CORE} supplies may be powered up simultaneously, but neither should 'lead' the V_{DD_IO} supply by more than 0.3V.

All supplies may be powered-down simultaneously.

7.2 Initialization

Upon power up, the device should be initialized by applying the following sequence:

1 Ensure the **TRST** pin is permanently LOW to disable the JTAG TAP controller.

2 Set **ODE** pin to LOW. This sets the **LSTo0-15** outputs to HIGH or high impedance, dependent on the **LORS** input value, and sets the **BSTo0-15** outputs to HIGH or high impedance, dependent on **BORS** input value. Refer to Pin Description for details of the **LORS** and **BORS** pins.

3 Reset the device by asserting the **RESET** pin to zero for at least two cycles of the input clock, **C8i**. A delay of an additional 250µs must also be applied before the first microprocessor access is performed following the de-assertion of the **RESET** pin; this delay is required for determination of the input frame pulse format.

4 Use the Block Programming Mode to initialize the Local and the Backplane Connection Memories. Refer to Section 8.3, Connection Memory Block Programming.

5 Set **ODE** pin to HIGH after the connection memories are programmed to ensure that bus contention will not occur at the serial stream outputs.

7.3 Reset

The **RESET** pin is used to reset the device. When set LOW, an asynchronous reset is applied to the device. It is then synchronized to the internal clock. During the reset period, depending on the state of input pins **LORS** and **BORS**, the output streams **LSTo0-15** and **BSTo0-15** are set to HIGH or high impedance, and all internal registers and counters are reset to the default state.

The **RESET** pin must remain LOW for two input clock cycles (**C8i**) to guarantee a synchronized reset release. A delay of an additional 250µs must also be waited before the first microprocessor access is performed following the de-assertion of the **RESET** pin; this delay is required for determination of the frame pulse format.

In addition, the reset signal must be de-asserted less than 12µs after the frame boundary or more than 13µs after the frame boundary, as illustrated in Figure 14. This can be achieved, for example, by synchronizing the de-assertion of the reset signal with the input frame pulse **FP8i**.

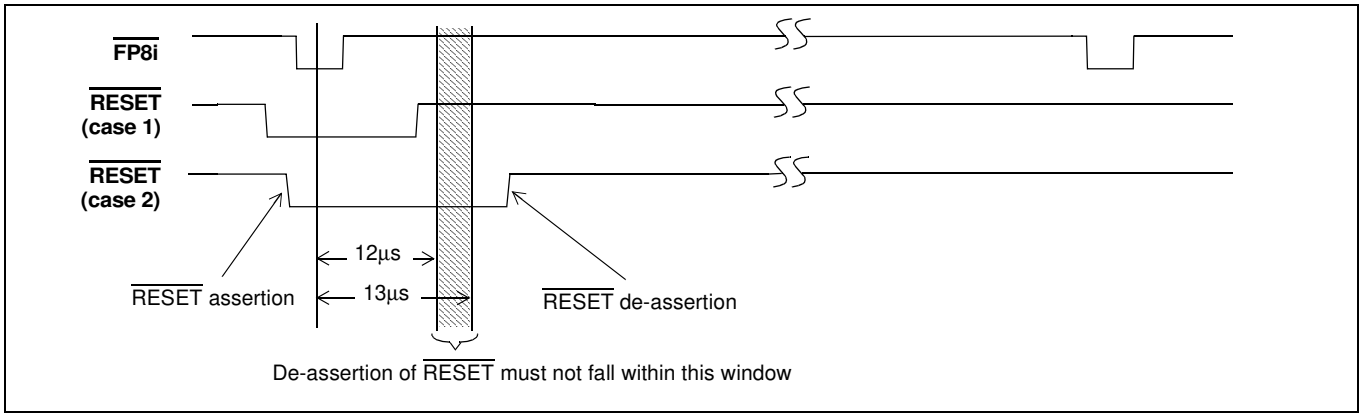

Figure 14 - Hardware RESET De-assertion