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16K-Channel Digital Switch with High Jitter Tolerance, Single Rate (2, 4, 8, or 16Mbps), and 64 Inputs and 64 Outputs

Data Sheet

November 2003

Features

- 16,384-channel x 16,384-channel non-blocking unidirectional switching.The Backplane and Local inputs and outputs can be combined to form a non-blocking switching matrix with 64 input streams and 64 output streams
- 8,192-channel x 8,192-channel non-blocking Backplane input to Local output stream switch
- 8,192-channel x 8,192-channel non-blocking Local input to Backplane output stream switch
- 8,192-channel x 8,192-channel non-blocking Backplane input to Backplane output switch
- 8,192-channel x 8,192-channel non-blocking Local input to Local output stream switch
- Backplane port accepts 32 input and 32 output ST-BUS streams with fixed data rates of 2.048Mbps, 4.096Mbps, 8.192Mbps or 16.384Mbps
- Local port accepts 32 input and 32 output ST-BUS streams with fixed data rates of 2.048Mbps, 4.096Mbps, 8.192Mbps or 16.384Mbps
- Exceptional input clock jitter tolerance (17ns)

Ordering Information

ZL50062GAC	256-Ball PBGA
ZL50064QCC	256-Pin LQFP

-40°C to +85°C

- Per-stream bit delay for Local and Backplane input streams
- Per-stream advancement for Local and Backplane output streams
- Constant 2-frame throughput delay for frame integrity
- Per-channel high impedance output control for Local and Backplane streams
- Per-channel driven-high output control for Local and Backplane streams
- Per-channel message mode for Local and Backplane output streams
- Connection memory block programming for fast device initialization

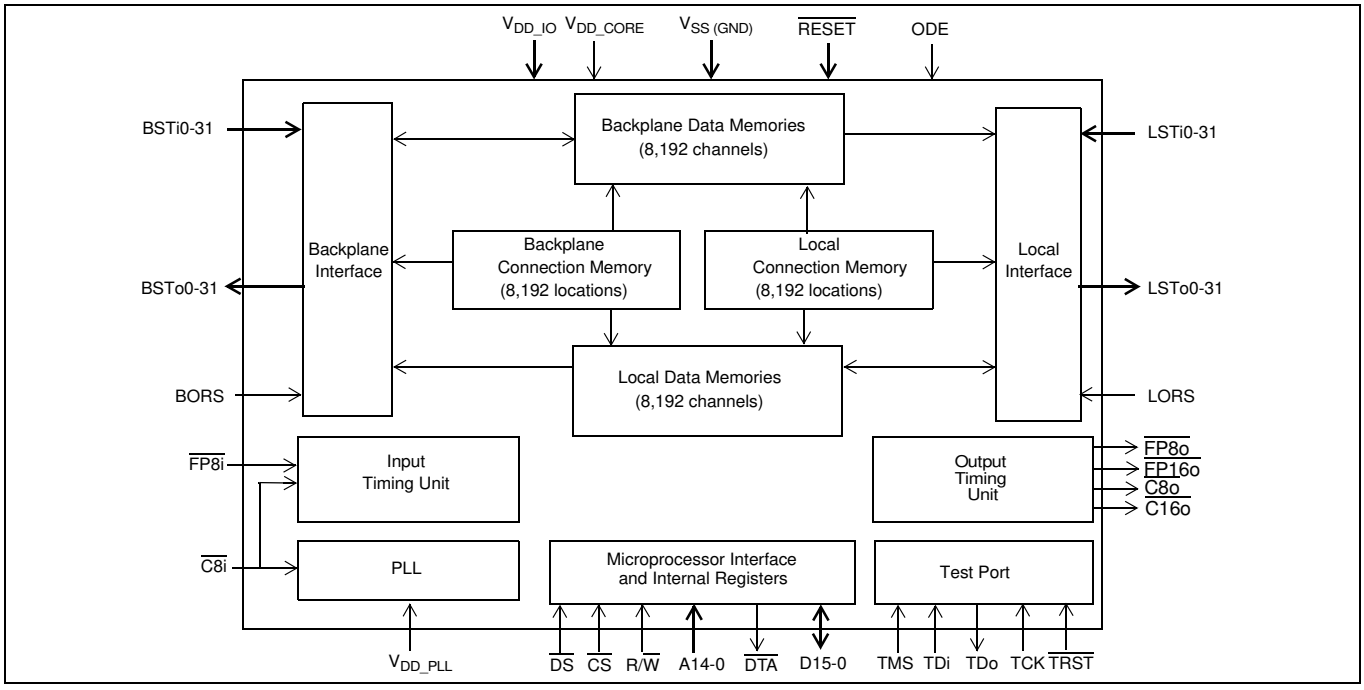

Figure 1 - ZL50062/4 Functional Block Diagram

- Automatic selection between ST-BUS and GCI-Bus operation
- Non-multiplexed Motorola microprocessor interface
- Conforms to the mandatory requirements of the IEEE-1149.1 (JTAG) standard
- Memory Built-In-Self-Test (BIST), controlled via microprocessor register
- 1.8V core supply voltage
- 3.3V I/O supply voltage
- 5V tolerant inputs, outputs and I/Os

Applications

- Central Office Switches (Class 5)
- Media Gateways
- Class-independent switches
- Access Concentrators
- Scalable TDM-Based Architectures
- Digital Loop Carriers

Device Overview

The ZL50062 and ZL50064 are two different packages of the same device. They have the same functionality except that ZL50064 does not have 16.384MHz output clock and frame pulse (C16o and FP16o) due to package differences. The ZL50062/4 has two data ports, the Backplane and the Local port. The device can operate at four different data rates, 2.048Mbps, 4.096Mbps, 8.192Mbps or 16.384Mbps. All 64 input and 64 output streams must operate at the same data rate.

The ZL50062/4 contains two data memory blocks (Backplane and Local) to provide the following switching path configurations:

- Input-to-Output Unidirectional, supporting 16K x 16K switching
- Backplane-to-Local Bi-directional, supporting 8K x 8K data switching,
- Local-to-Backplane Bi-directional, supporting 8K x 8K data switching,
- Backplane-to-Backplane Bi-directional, supporting 8K x 8K data switching.
- Local-to-Local Bi-directional, supporting 8K x 8K data switching.

The device contains two connection memory blocks, one for the Backplane output and one for the Local output. Data to be output on the serial streams may come from either of the data memories (Connection Mode) or directly from the connection memory contents (Message Mode).

In Connection Mode, the contents of the connection memory define, for each output stream and channel, the source stream and channel (stored in data memory) to be switched.

In Message Mode, microprocessor data can be written to the connection memory for broadcast on the output streams on a per channel basis. This feature is useful for transferring control and status information to external circuits or other ST-BUS devices.

The device uses a master frame pulse ($\overline{\text{FP8i}}$) and master clock ($\overline{\text{C8i}}$) to define the input frame boundary and timing for both the Backplane port and the Local port. The device will automatically detect whether an ST-BUS or a GCI-Bus style frame pulse is being used. There is a two-frame delay from the time $\overline{\text{RESET}}$ is de-asserted to the establishment of full switch functionality. During this period, the input frame pulse format is determined before switching begins.

The device provides $\overline{\text{FP8o}}$, $\overline{\text{FP16o}}$, $\overline{\text{C8o}}$ and $\overline{\text{C16o}}$ outputs to support external devices connected to the outputs of the Backplane and Local ports.

A non-multiplexed Motorola microprocessor port allows programming of the various device operation modes and switching configurations. The microprocessor port provides access for Register read/write, Connection Memory read/write and Data Memory read-only operations. The port has a 15-bit address bus, 16-bit data bus and 4 control signals. The microprocessor may monitor channel data in the Backplane and Local data memories.

The mandatory requirements of the IEEE-1149.1 (JTAG) standard are fully supported via a dedicated test port.

The ZL50062 and ZL50064 are each available in one package:

- ZL50062: a 17mm x 17mm body, 1mm ball-pitch, 256-PBGA.
- ZL50064: a 28mm x 28mm body, 0.40mm pin-pitch, 256-LQFP.

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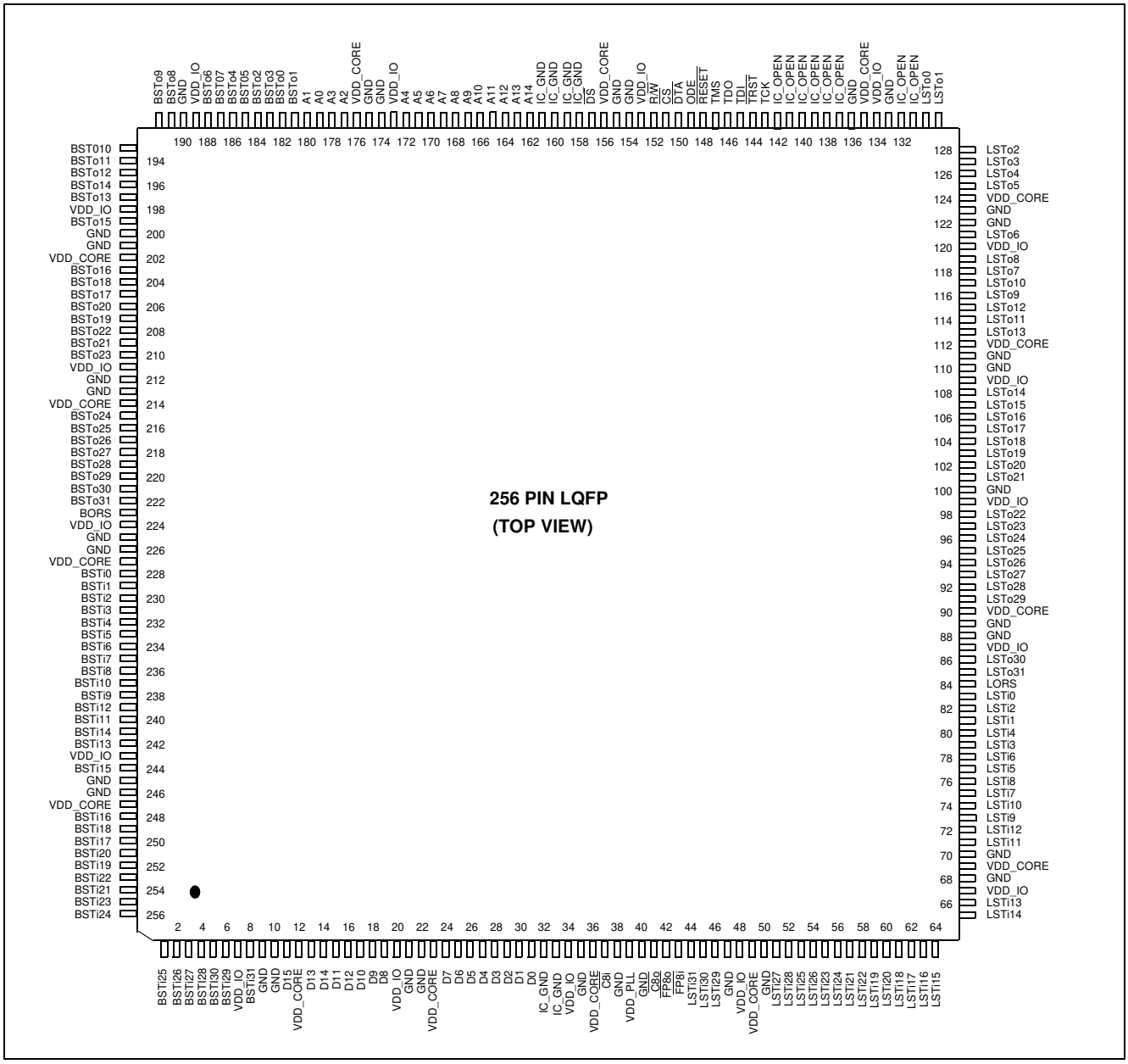

Figure 2 - ZL50064 LQFP Connections (256 LQFP, 28mm x 28mm) Pin Diagram
(as viewed through top of package)

Pinout Diagram: (as viewed through top of package)

A1 corner identified by metallized marking

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	A0	A1	A2	A3	A4	$\overline{DS}$	R/$\overline{W}$	$\overline{CS}$	IC_ OPEN	IC_ OPEN	IC_ OPEN	IC_ OPEN	IC_ OPEN	IC_ OPEN	IC_ OPEN	IC_ OPEN
B	BSTo0	BSTo1	BSTo2	BSTo3	A5	A6	A7	A8	A9	ODE	$\overline{RESET}$	TMS	LSTo0	LSTo1	LSTo2	LSTo3
C	BSTo4	BSTo5	BSTo6	BSTo7	A10	A11	A12	A13	A14	$\overline{DTA}$	TDi	TDo	LSTo4	LSTo5	LSTo6	LSTo7
D	BSTo8	BSTo9	BSTo10	BSTo11	BORS	IC_GND	IC_GND	IC_GND	IC_GND	TCK	$\overline{TRST}$	LORS	LSTo8	LSTo9	LSTo10	LSTo11
E	BSTo12	BSTo13	BSTo14	BSTo15	VDD_IO	VDD_IO	VDD_ CORE	VDD_ CORE	VDD_ CORE	VDD_ CORE	VDD_IO	VDD_IO	LSTo12	LSTo13	LSTo14	LSTo15
F	BSTo16	BSTo17	BSTo18	BSTo19	VDD_IO	VDD_ CORE	GND	GND	GND	GND	VDD_ CORE	VDD_IO	LSTo16	LSTo17	LSTo18	LSTo19
G	BSTo20	BSTo21	BSTo22	BSTo23	VDD_IO	GND	GND	GND	GND	GND	GND	VDD_IO	LSTo20	LSTo21	LSTo22	LSTo23
H	BSTo24	BSTo25	BSTo26	BSTo27	VDD_IO	GND	GND	GND	GND	GND	GND	VDD_IO	LSTo24	LST25	LSTo26	LSTo27
J	BSTo28	BSTo29	BSTo30	BSTo31	VDD_ CORE	GND	GND	GND	GND	GND	GND	VDD_ CORE	LSTo28	LSTo29	LSTo30	LSTo31
K	BSTi0	BSTi1	BSTi2	BSTi3	VDD_ CORE	GND	GND	GND	GND	GND	GND	VDD_ CORE	LSTi0	LSTi1	LSTi2	LSTi3
L	BSTi4	BSTi5	BSTi6	BSTi7	VDD_IO	VDD_ CORE	VDD_ CORE	GND	GND	VDD_ CORE	VDD_ CORE	VDD_IO	LSTi4	LSTi5	LSTi6	LSTi7
M	BSTi8	BSTi9	BSTi10	BSTi11	VDD_IO	D3	D2	D1	D0	VDD_ PLL	NC	VDD_IO	LSTi8	LSTi9	LSTi10	LSTi11
N	BSTi12	BSTi13	BSTi14	BSTi15	BSTi16	D7	D6	D5	D4	IC_ OPEN	IC_ OPEN	LSTi12	LSTi13	LSTi14	LSTi15	LSTi16
P	BSTi17	BSTi18	BSTi19	BSTi20	BSTi21	D11	D10	D9	D8	$\overline{C16o}$	$\overline{FP16o}$	LSTi17	LSTi18	LSTi19	LSTi20	LSTi21
R	BSTi22	BSTi23	BSTi24	BSTi25	BSTi26	D15	D14	D13	D12	$\overline{FP8o}$	$\overline{FP8i}$	LSTi22	LSTi23	LSTi24	LSTi25	LSTi26
T	BSTi27	BSTi28	BSTi29	BSTi30	BSTi31	IC_GND	IC_GND	IC_GND	IC_GND	$\overline{C8i}$	$\overline{C8o}$	LSTi27	LSTi28	LSTi29	LSTi30	LSTi31

Figure 3 - ZL50062 PBGA Connections (256 PBGA, 17mm x 17mm) Pin Diagram
(as viewed through top of package)

Pin Description

Pin Name	ZL50064 Package Coordinates (256-pin LQFP)	ZL50062 Package Coordinates (256-ball PBGA)	Description
Device Timing			
C8i	37	T10	**Master Clock (5V Tolerant Schmitt-Triggered Input).** This pin accepts an 8.192MHz clock. The internal frame boundary is aligned with the clock falling or rising edge, as controlled by the C8IPOL bit in the Control Register. Input data on both the Backplane and Local sides (BSTi0-31 and LSTi0-31) must be aligned to this clock and the accompanying input frame pulse, FP8i.
FP8i	43	R11	**Frame Pulse Input (5V Tolerant Schmitt-Triggered Input)**. When the Frame Pulse Width bit (FPW) of the Control Register is LOW (default), this pin accepts a 122ns-wide frame pulse. When the FPW bit is HIGH, this pin accepts a 244ns-wide frame pulse. The device will automatically detect whether an ST-BUS or GCI-Bus style frame pulse is applied. Input data on both the Backplane and Local sides (BSTi0-31 and LSTi0-31) must be aligned to this frame pulse and the accompanying input clock, C8i.
C8o	41	T11	**C8o Output Clock (5V Tolerant Three-state Output).** This pin outputs an 8.192MHz clock generated within the device. The clock falling edge or rising edge is aligned with the output frame boundary presented on FP8o; this edge polarity alignment is controlled by the COPOL bit of the Control Register. Output data on both the Backplane and Local sides (BSTo0-31 and LSTo0-31) will be aligned to this clock and the accompanying output frame pulse, FP8o.
FP8o	42	R10	**Frame Pulse Output (5V Tolerant Three-state Output).** When the Frame Pulse Width bit (FPW) of the Control Register is LOW (default), this pin outputs a 122ns-wide frame pulse. When the FPW bit is HIGH, this pin outputs a 244ns-wide frame pulse. The frame pulse, running at 8kHz rate, will have the same format (ST-BUS or GCI-Bus) as the input frame pulse (FP8i). Output data on both the Backplane and Local sides (BSTo0-31 and LSTo0-31) will be aligned to this frame pulse and the accompanying output clock, C8o.
C16o	NA	P10	**C16o Output Clock (5V Tolerant Three-state Output).** This pin outputs a 16.384MHz clock generated within the device. The clock falling edge or rising edge is aligned with the output frame boundary presented on FP16o; this edge polarity alignment is controlled by the COPOL bit of the Control Register. Output data on both the Backplane and Local sides (BSTo0-31 and LSTo0-31) will be aligned to this clock and the accompanying output frame pulse, FP16o.

Pin Description (continued)

Pin Name	ZL50064 Package Coordinates (256-pin LQFP)	ZL50062 Package Coordinates (256-ball PBGA)	Description
$\overline{\text{FP16o}}$	NA	P11	**Frame Pulse Output (5V Tolerant Three-state Output).** When the Frame Pulse Width bit (FPW) of the Control Register is LOW (default), this pin outputs a 61ns-wide frame pulse. When the FPW bit is HIGH, this pin outputs a 122ns-wide frame pulse. The frame pulse, running at 8kHz rate, will have the same format (ST-BUS or GCI-Bus) as the input frame pulse ($\overline{\text{FP8i}}$). Output data on both the Backplane and Local sides (BSTo0-31 and LSTo0-31) will be aligned to this frame pulse and the accompanying output clock, C16o.
Backplane and Local Inputs			
BSTi0-15	228, 229, 230, 231, 232, 233, 234, 235, 236, 238, 237, 240, 239, 242, 241, 244	K1, K2, K3, K4, L1, L2, L3, L4, M1, M2, M3, M4, N1, N2, N3, N4	**Backplane Serial Input Streams 0 to 15 (5V Tolerant Inputs with Internal Pull-downs).** These pins accept serial TDM data streams at a data rate of: 16.384Mbps (with 256 channels per stream), 8.192Mbps (with 128 channels per stream), 4.096Mbps (with 64 channels per stream) or 2.048Mbps (with 32 channels per stream).
BSTi16-31	248, 250, 249, 252, 251, 254, 253, 255, 256, 1, 2, 3, 4, 6, 5, 8	N5, P1, P2, P3, P4, P5, R1, R2, R3, R4, R5, T1, T2, T3, T4, T5	**Backplane Serial Input Streams 16 to 31 (5V Tolerant Inputs with Internal Pull-downs).** These pins accept serial TDM data streams at a data rate of: 16.384Mbps (with 256 channels per stream), 8.192Mbps (with 128 channels per stream), 4.096Mbps (with 64 channels per stream) or 2.048Mbps (with 32 channels per stream).
LSTi0-15	83, 81, 82, 79, 80, 77, 78, 75, 76, 73, 74, 71, 72, 66, 65, 64	K13, K14, K15, K16, L13, L14, L15, L16, M13, M14, M15, M16, N12, N13, N14, N15	**Local Serial Input Streams 0 to 15 (5V Tolerant Inputs with Internal Pull-downs).** These pins accept serial TDM data streams at a data rate of: 16.384Mbps (with 256 channels per stream), 8.192Mbps (with 128 channels per stream), 4.096Mbps (with 64 channels per stream) or 2.048Mbps (with 32 channels per stream).
LSTi16-31	63, 62, 61, 59, 60, 57, 58, 55, 56, 53, 54, 51, 52, 46, 45, 44	N16, P12, P13, P14, P15, P16, R12, R13, R14, R15, R16, T12, T13, T14, T15, T16	**Local Serial Input Streams 16 to 31 (5V Tolerant Inputs with Internal Pull-downs).** These pins accept serial TDM data streams at a data rate of: 16.384Mbps (with 256 channels per stream), 8.192Mbps (with 128 channels per stream), 4.096Mbps (with 64 channels per stream) or 2.048Mbps (with 32 channels per stream).

Pin Description (continued)

Pin Name	ZL50064 Package Coordinates (256-pin LQFP)	ZL50062 Package Coordinates (256-ball PBGA)	Description
Backplane and Local Outputs and Control			
ODE	149	B10	**Output Drive Enable (5V Tolerant Input with Internal Pull-up)**. An asynchronous input providing Output Enable control to the BSTo0-31 and LSTo0-31 outputs. When LOW, the BSTo0-31 and LSTo0-31 outputs are driven HIGH or high impedance (dependent on the **BORS** and **LORS** pin settings respectively). When HIGH, the outputs BSTo0-31 and LSTo0-31 are enabled.
BORS	223	D5	**Backplane Output Reset State (5V Tolerant Input with Internal Pull-down)**. When this input is LOW, the device will initialize with the BSTo0-31 outputs driven high. Following initialization, the Backplane stream outputs are always active. When this input is HIGH, the device will initialize with the BSTo0-31 outputs at high impedance. Following initialization, the Backplane stream outputs may be set active or high impedance using the **ODE** pin or on a per-channel basis with the **BE** bit in the Backplane Connection Memory.
BSTo0-15	182, 181, 184, 183, 186, 185, 188, 187, 191, 192, 193, 194, 195, 197, 196, 199	B1, B2, B3, B4, C1, C2, C3, C4, D1, D2, D3, D4, E1, E2, E3, E4	**Backplane Serial Output Streams 0 to 15 (5V Tolerant, Three-state Outputs with Slew-Rate Control).** These pins output serial TDM data streams at a data rate of: 16.384Mbps (with 256 channels per stream), 8.192Mbps (with 128 channels per stream), 4.096Mbps (with 64 channels per stream) or 2.048Mbps (with 32 channels per stream). Refer to the descriptions of the **BORS** and **ODE** pins for control of the output HIGH or high impedance state.
BSTo16-31	203, 205, 204, 207, 206, 209, 208, 210, 215, 216, 217, 218, 219, 220, 221, 222	F1, F2, F3, F4, G1, G2, G3, G4, H1, H2, H3, H4, J1, J2, J3, J4	**Backplane Serial Output Streams 16 to 31 (5V Tolerant, Three-state Outputs with Slew-Rate Control).** These pins output serial TDM data streams at a data rate of: 16.384Mbps (with 256 channels per stream), 8.192Mbps (with 128 channels per stream), 4.096Mbps (with 64 channels per stream) or 2.048Mbps (with 32 channels per stream). Refer to the descriptions of the **BORS** and **ODE** pins for control of the output HIGH or high impedance state.

Pin Description (continued)

Pin Name	ZL50064 Package Coordinates (256-pin LQFP)	ZL50062 Package Coordinates (256-ball PBGA)	Description
LORS	84	D12	**Local Output Reset State (5V Tolerant Input with Internal Pull-down)**. When this input is LOW, the device will initialize with the LSTo0-31 outputs driven high. Following initialization, the Local stream outputs are always active. When this input is HIGH, the device will initialize with the LSTo0-31 outputs at high impedance. Following initialization, the Local stream outputs may be set active or high impedance using the **ODE** pin or on a per-channel basis with the **LE** bit in the Local Connection Memory.
LSTo0-15	130, 129, 128, 127, 126, 125, 121, 118, 119, 116, 117, 114, 115, 113, 108, 107	B13, B14, B15, B16, C13, C14, C15, C16, D13, D14, D15, D16, E13, E14, E15, E16	**Local Serial Output Streams 0 to 15 (5V Tolerant Three-state Outputs with Slew-Rate Control).** These pins output serial TDM data streams at a data rate of: 16.384Mbps (with 256 channels per stream), 8.192Mbps (with 128 channels per stream), 4.096Mbps (with 64 channels per stream) or 2.048Mbps (with 32 channels per stream). Refer to the descriptions of the **LORS** and **ODE** pins for control of the output HIGH or high impedance state.
LSTo16-31	106, 105, 104, 103, 102, 101, 98, 97, 96, 95, 94, 93, 92, 91, 86, 85	F13, F14, F15, F16, G13, G14, G15, G16, H13, H14, H15, H16, J13, J14, J15, J16	**Local Serial Output Streams 16 to 31 (5V Tolerant Three-state Outputs with Slew-Rate Control).** These pins output serial TDM data streams at a data rate of: 16.384Mbps (with 256 channels per stream), 8.192Mbps (with 128 channels per stream), 4.096Mbps (with 64 channels per stream) or 2.048Mbps (with 32 channels per stream). Refer to the descriptions of the **LORS** and **ODE** pins for control of the output HIGH or high impedance state.
Microprocessor Port Signals			
A0 - A14	179, 180, 177, 178, 172, 171, 170, 169, 168, 167, 166, 165, 164, 163, 162	A1, A2, A3, A4, A5, B5, B6, B7, B8, B9, C5, C6, C7, C8, C9	**Address 0 - 14 (5V Tolerant Inputs).** These pins form the 15-bit address bus to the internal memories and registers. A0 = LSB
D0 - D15	31, 30, 29, 28, 27, 26, 25, 24, 19, 18, 17, 15, 16, 13, 14, 11	M9, M8, M7, M6, N9, N8, N7, N6, P9, P8, P7, P6, R9, R8, R7, R6	**Data Bus 0 - 15 (5V Tolerant Inputs/Outputs with Slew-Rate Control).** These pins form the 16-bit data bus of the microprocessor port. D0 = LSB

Pin Description (continued)

Pin Name	ZL50064 Package Coordinates (256-pin LQFP)	ZL50062 Package Coordinates (256-ball PBGA)	Description
$\overline{CS}$	151	A8	**Chip Select (5V Tolerant Input).** Active LOW input used by the microprocessor to enable the microprocessor port access. **Note that a minimum of 30ns must separate the de-assertion of $\overline{DTA}$ (to high) and the assertion of $\overline{CS}$ and/or $\overline{DS}$ to initiate the next access.**
$\overline{DS}$	157	A6	**Data Strobe (5V Tolerant Input).** This active LOW input works in conjunction with $\overline{CS}$ to enable the microprocessor port read and write operations. **Note that a minimum of 30ns must separate the de-assertion of DTA (to high) and the assertion of CS and/or DS to initiate the next access.**
R/$\overline{W}$	152	A7	**Read/$\overline{Write}$ (5V Tolerant Input).** This input controls the direction of the data bus lines (D0-D15) during a microprocessor access.
$\overline{DTA}$	150	C10	**Data Transfer Acknowledgment (5V Tolerant Three-state Output).** This active LOW output indicates that a data bus transfer is complete. A pull-up resistor is required to hold a HIGH level. **Note that a minimum of 30ns must separate the de-assertion of DTA (to high) and the assertion of $\overline{CS}$ and/or $\overline{DS}$ to initiate the next access.**
$\overline{RESET}$	148	B11	**Device Reset (5V Tolerant Input with Internal Pull-up).** This input (active LOW) asynchronously applies reset and synchronously releases reset to the device. In the reset state, the outputs LSTo0-31 and BSTo0-31 are set to a HIGH or high impedance state, depending on the state of the LORS and BORS external control pins, respectively. The assertion of this pin also clears the device registers and internal counters. **Refer to Section 7.3 on page 29 for the timing requirements regarding this reset signal**.
JTAG Control Signals			
TCK	143	D10	**Test Clock (5V Tolerant Input).** Provides the clock to the JTAG test logic.
TMS	147	B12	**Test Mode Select (5V Tolerant Input with Internal Pull-up).** JTAG signal that controls the state transitions of the TAP controller.
TDi	145	C11	**Test Serial Data In (5V Tolerant Input with Internal Pull-up).** JTAG serial test instructions and data are shifted in on this pin.
TDo	146	C12	**Test Serial Data Out (5V Tolerant Three-state Output).** JTAG serial data is output on this pin on the falling edge of TCK. This pin is held in a high impedance state when JTAG is not enabled.

Pin Description (continued)

Pin Name	ZL50064 Package Coordinates (256-pin LQFP)	ZL50062 Package Coordinates (256-ball PBGA)	Description
$\overline{\text{TRST}}$	144	D11	**Test Reset (5V Tolerant Input with Internal Pull-up).** Asynchronously initializes the JTAG TAP controller to the Test-Logic-Reset state. This pin must be pulsed LOW during power-up for JTAG testing. This pin must be held LOW for normal functional operation of the device.
Power and Ground Pins			
V_{DD_IO}	7, 20, 34, 48, 67, 87, 99, 109, 120, 134, 153, 173, 189, 198, 211, 224, 243	E5, E6, E11, E12, F5, F12, G5, G12, H5, H12, L5, L12, M5, M12	**Power Supply for Periphery Circuits:** +3.3V
V_{DD_CORE}	12, 23, 36, 49, 69, 90, 112, 124, 135, 156, 176, 202, 214, 227, 247	E7, E8, E9, E10, F6, F11, J5, J12, K5, K12, L6, L7, L10, L11	**Power Supply for Core Circuits:** +1.8V
V_{DD_PLL}	39	M10	**Power Supply for Analog PLL:** +1.8V
V_{SS} (GND)	9, 10, 21, 22, 35, 38, 40, 47, 50, 68, 70, 88, 89, 100, 110, 111, 122, 123, 133, 136, 154, 155, 174, 175, 190, 200, 201, 212, 213, 225, 226, 245, 246	F7, F8, F9, F10, G6, G7, G8, G9, G10, G11, H6, H7, H8, H9, H10, H11, J6, J7, J8, J9, J10, J11, K6, K7, K8, K9, K10, K11, L8, L9	**Ground.**

Pin Description (continued)

Pin Name	ZL50064 Package Coordinates (256-pin LQFP)	ZL50062 Package Coordinates (256-ball PBGA)	Description
Unused Pins			
NC		M11	**No Connects.** These pins are not used and can be tied HIGH, LOW, or left unconnected.
IC_OPEN	131, 132, 137, 138, 139, 140, 141, 142	A9, A10, A11, A12, A13, A14, A15, A16, N10, N11	**Internal Connections - OPEN.** These pins must be left unconnected.
IC_GND	32, 33, 158, 159, 160, 161	D6, D7, D8, D9, T6, T7, T8, T9	**Internal Connections - GND.** These pins must be tied LOW.

1.0 Unidirectional and Bi-directional Switching Applications

The ZL50062/64 has a maximum capacity of 16,384 input channels and 16,384 output channels. This is calculated from the maximum number of streams and channels: 64 input streams (32 Backplane, 32 Local) at 16.384Mbps and 64 output streams (32 Backplane, 32 Local) at 16.384Mbps.

A typical mode of operation is to separate the input and output streams to form a unidirectional switch, as shown in Figure 4 below.

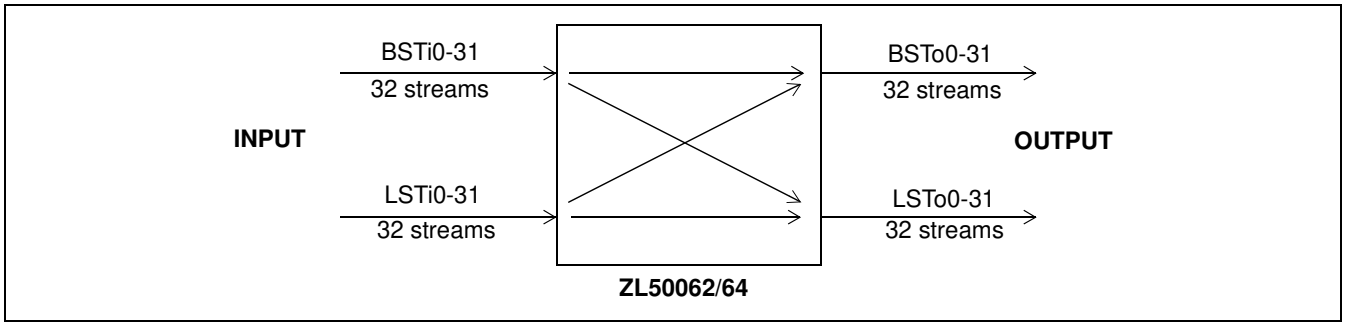

Figure 4 - 16,384 x 16,384 Channels (16Mbps), Unidirectional Switching

In this system, the Backplane and Local input streams are combined, and the Backplane and Local output streams are combined, so that the switch appears as a 64 input stream by 64 output stream switch. This gives the maximum 16,384 x 16,384 channel capacity.

Often a system design needs to differentiate between a Backplane and a Local side, or it needs to put the switch in a bi-directional configuration. In this case, the ZL50062/64 can be used as shown in Figure 5 to give 8,192 x 8,192 channel bi-directional capacity.

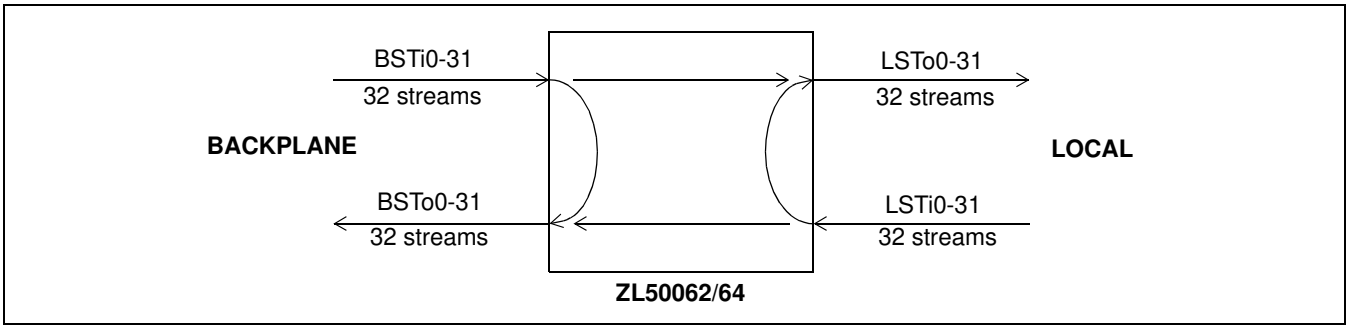

Figure 5 - 8,192 x 8,192 Channels (16Mbps), Bi-directional Switching

In this system setup, the chip has a capacity of 8,192 input channels and 8,192 output channels on the Backplane side, as well as 8,192 input channels and 8,192 output channels on the Local side. Note that some or all of the output channels on one side can come from the other side, e.g., Backplane input to Local output switching.

1.1 Flexible Configuration

The ZL50062/64 can be configured as a 16K by 16K non-blocking unidirectional digital switch, an 8K by 8K non-blocking bi-directional digital switch, or as a blocking switch with various switching capacities.

1.1.1 Non-Blocking Unidirectional Configuration (Typical System Configuration)

Because the input and output drivers are synchronous, the user can combine input Backplane streams and input Local streams as well as output Backplane streams and output Local streams to increase the total number of input and output streams of the switch in a unidirectional configuration, as shown in Figure 4.

- 16,384-channel x 16,384-channel non-blocking switching from input to output streams

1.1.2 Non-Blocking Bi-directional Configuration

Another typical application is to configure the ZL50062/64 as a non-blocking 8K by 8K bi-directional switch, as shown in Figure 5:

- 8,192-channel x 8,192-channel non-blocking switching from Backplane input to Local output streams
- 8,192-channel x 8,192-channel non-blocking switching from Local input to Backplane output streams
- 8,192-channel x 8,192-channel non-blocking switching from Backplane input to Backplane output streams
- 8,192-channel x 8,192-channel non-blocking switching from Local input to Local output streams

1.1.3 Blocking Bi-directional Configuration

The ZL50062/64 can be configured as a blocking bi-directional switch if it is an application requirement. For example, it can be configured as a 12K by 4K bi-directional blocking switch, as shown in Figure 6:

- 12,288-channel x 4,096-channel blocking switching from Backplane input to Local output streams
- 4,096-channel x 12,288-channel blocking switching from Local input to Backplane output streams
- 12,288-channel x 12,288-channel non-blocking switching from Backplane input to Backplane output streams
- 4,096-channel x 4,096-channel non-blocking switching from Local input to Local output streams

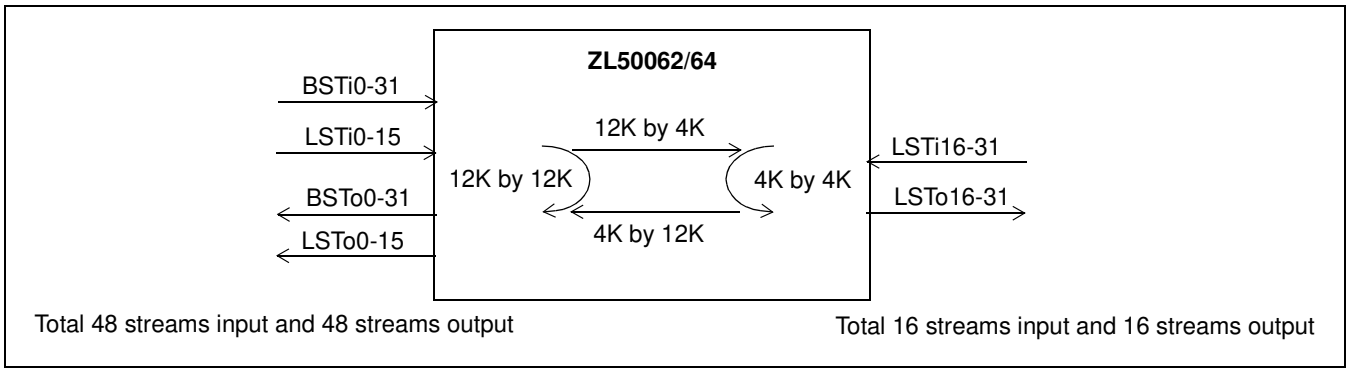

Figure 6 - 12,288 by 4,096 Channels Blocking Bi-directional Configuration

2.0 Functional Description

2.1 Switching Configuration

The device supports five switching configurations: (1) Unidirectional switch, (2) Backplane-to-Local, (3) Local-to-Backplane, (4) Backplane-to-Backplane, and (5) Local-to-Local. The following sections describe the switching paths in detail. Configurations (2) - (5) enable a non-blocking bi-directional switch with 8,192 Backplane input/output channels at Backplane stream data rates of 16.384Mbps, and 8,192 Local input/output channels at Local stream data rates of 16.384Mbps. The switching paths of configurations (2) to (5) may be operated simultaneously. When the lower data-rates of 8.192, 4.096 and 2.048Mbps are used, there will be a corresponding reduction in switch capacity.

2.1.1 Unidirectional Switch

The device can be configured as a 16,384 x 16,384 unidirectional switch by grouping together all input streams and all output streams. All streams can be operated at a data rate of 16.384Mbps. Lower data rates may be used with a corresponding reduction in switch capacity.

2.1.2 Backplane-to-Local Path

The device can provide data switching between the Backplane input port and the Local output port. The Local Connection Memory determines the switching configurations.

2.1.3 Local-to-Backplane Path

The device can provide data switching between the Local input port and the Backplane output port. The Backplane Connection Memory determines the switching configurations.

2.1.4 Backplane-to-Backplane Path

The device can provide data switching between the Backplane input and output ports. The Backplane Connection Memory determines the switching configurations.

2.1.5 Local-to-Local Path

The device can provide data switching between the Local input and output ports. The Local Connection Memory determines the switching configurations.

2.1.6 Port Data Rate Modes and Selection

The Local port has 32 input (LSTi0-31) and 32 output (LSTo0-31) data streams. Similarly, the Backplane port has 32 input (BSTi0-31) and 32 output (BSTo0-31) data streams. The bit rate of all these streams is selected by writing to the Bit Rate Registers, BRR (see Table 24). All the streams operate at the same bit rate at a time. The device can operate at 2.048, 4.096, 8.192 or 16.384 Mbps. The default operation mode is 2.048Mbps. The timing of the input and output clocks and frame pulses is shown in Figure 8, “Input and Output Frame Pulse Alignment for Different Data Rates” on page 22. The input traffic are aligned based on the $\overline{\text{FP8i}}$ and $\overline{\text{C8i}}$ input timing signals, while the output traffic are aligned based on the $\overline{\text{FP8o}}$ and $\overline{\text{C8o}}$ output timing signals.

2.1.6.1 Local Output Port

Operation of stream data in Connection Mode or Message Mode is determined by the state of the LMM bit of the Local Connection Memory. The channel high impedance state is controlled by the LE bit of the Local Connection Memory. The data source (i.e. from the Local or Backplane Data Memory) is determined by the LSRC bit of the Local Connection Memory. Refer to Section 8.1, Local Connection Memory, and Section 11.3, Local Connection Memory Bit Definition for more details.

2.1.6.2 Backplane Output Port

Operation of stream data in Connection Mode or Message Mode is determined by the state of the BMM bit of the Backplane Connection Memory and the channel high impedance state is controlled by the BE bit of the Backplane Connection Memory. The data source (i.e. from the Local or Backplane Data Memory) is determined by the BSRC bit of the Backplane Connection Memory. Refer to Section 8.2, Backplane Connection Memory and Section 11.4, Backplane Connection Memory Bit Definition for more details.

2.2 Frame Pulse Input and Master Input Clock Timing

The input frame pulse ($\overline{\text{FP8i}}$) is an 8kHz input signal active for 122ns or 244ns at the frame boundary. The FPW bit in the Control Register must be set according to the applied pulse width. See Pin Description and Table 13, “Control Register Bits” on page 37, for details.

The active state and timing of $\overline{\text{FP8i}}$ can conform either to the ST-BUS or to the GCI-Bus as shown in Figure 7, ST-BUS and GCI-Bus Input Timing Diagram for Different Data Rates. The ZL50062/64 device will automatically detect whether an ST-BUS or a GCI-Bus style frame pulse is being used for the master frame pulse ($\overline{\text{FP8i}}$). The output frame pulses ($\overline{\text{FP8o}}$ and $\overline{\text{FP16o}}$) are always of the same style (ST-BUS or GCI-Bus) as the input frame pulse. The active edge of the input clock ($\overline{\text{C8i}}$) shall be selected by the state of the Control Register bit C8IPOL.

Note that the active edge of ST-BUS is falling edge, which is the default mode of the device, while GCI-Bus uses rising edge as the active edge. Although GCI frame pulse will be automatically detected, to fully conform to GCI-Bus operation, the device should be set to use $\overline{\text{C8i}}$ rising edge as the active edge (by setting bit C8IPOL HIGH) when GCI-Bus is used.

For the purposes of describing the device operation, the remaining part of this document assumes the ST-BUS frame pulse format with a single width frame pulse of 122ns and a falling active clock-edge, unless explicitly stated otherwise.

In addition, the ZL50062 device provides $\overline{\text{FP8o}}$, $\overline{\text{FP16o}}$, $\overline{\text{C8o}}$ and $\overline{\text{C16o}}$ outputs to support external devices which connect to the output ports. The ZL50064 only provides $\overline{\text{FP8o}}$ and $\overline{\text{C8o}}$ outputs. The generated frame pulses ($\overline{\text{FP8o}}$, $\overline{\text{FP16o}}$) will be provided in the same format as the master frame pulse ($\overline{\text{FP8i}}$). The polarity of $\overline{\text{C8o}}$ and $\overline{\text{C16o}}$, at the frame boundary, can be controlled by the Control Register bit, COPOL. An analog phase lock loop (APLL) is used to multiply the input clock frequency on $\overline{\text{C8i}}$ to generate an internal clock signal operating at 131.072MHz.

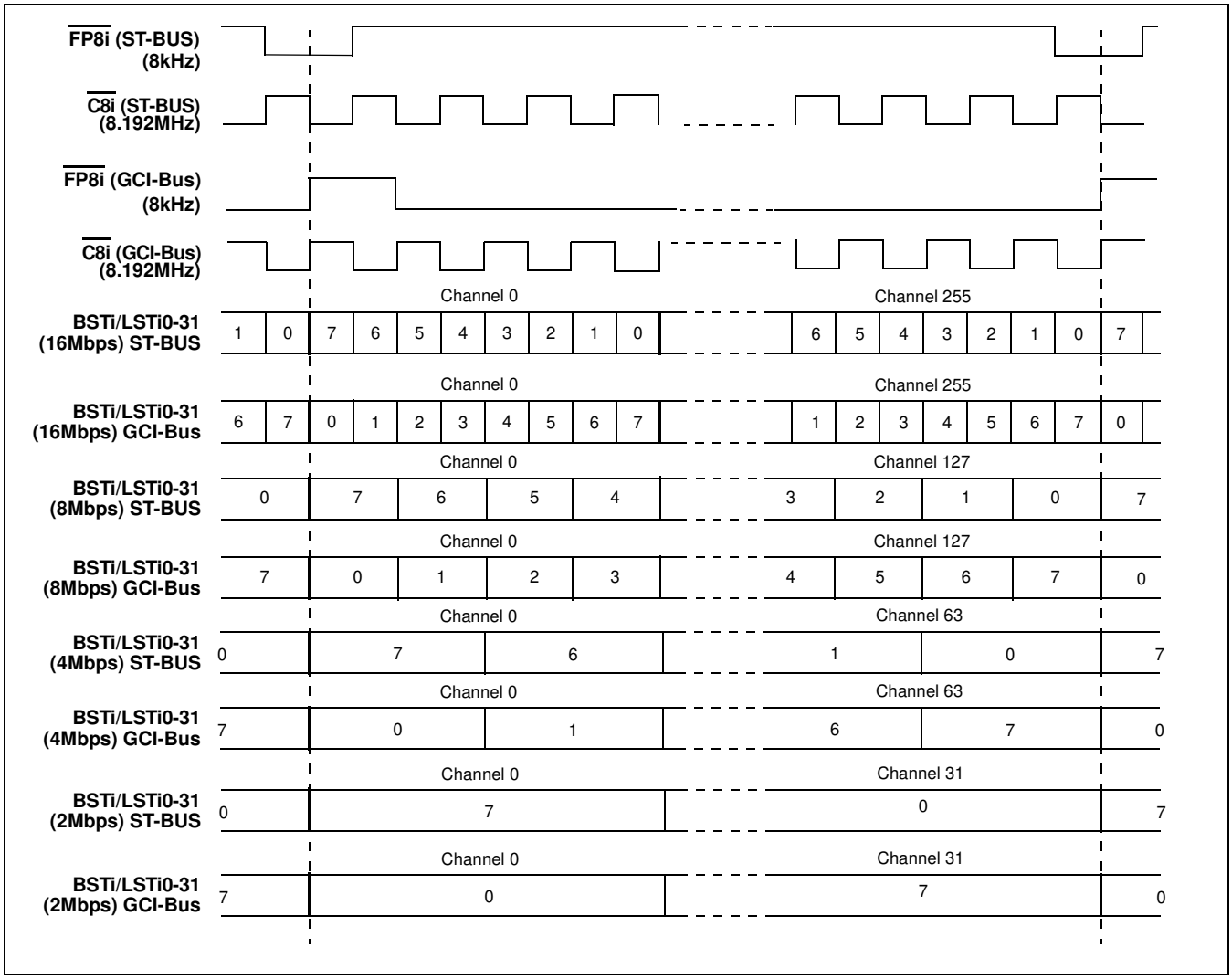

Figure 7 - ST-BUS and GCI-Bus Input Timing Diagram for Different Data Rates

2.3 Input Frame Pulse and Generated Frame Pulse Alignment

The ZL50062 accepts a frame pulse ($\overline{FP8i}$) and generates two frame pulse outputs, $\overline{FP8o}$ and $\overline{FP16o}$, which are aligned to the master frame pulse. The ZL50064 only generates one frame pulse output, $\overline{FP8o}$. There is a constant throughput delay for data being switched from the input to the output of the device such that data which is input during Frame N is output during Frame N+2.

For further details of frame pulse conditions and options, see Section 13.1, Control Register (CR), Figure 16, Frame Boundary Conditions, ST-BUS Operation, and Figure 17, Frame Boundary Conditions, GCI-Bus Operation.

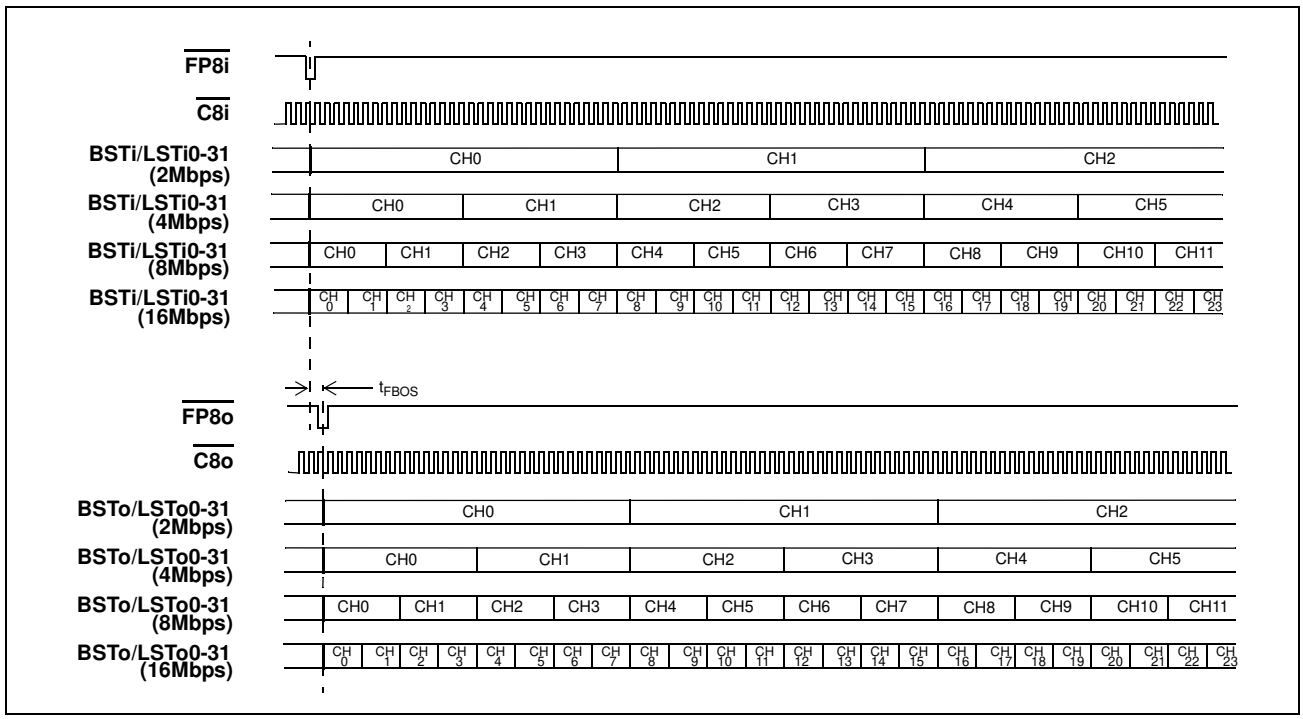

Figure 8 - Input and Output Frame Pulse Alignment for Different Data Rates

The t_{FBOS} is the offset between the input frame pulse, $\overline{FP8i}$, and the generated output frame pulse, $\overline{FP8o}$. Refer to the “AC Electrical Characteristics,” on page 52. Note that although the figure above shows the traditional setups of the frame pulses and clocks for both ST-BUS and GCI-Bus configurations, the devices can be configured to accept/generate double-width frame pulses (if the FPW bit in the Control Register is set) as well as to use the opposite clock edge for frame-boundary determination (using the C8IPOL and COPOL bits in the Control Register). See the timing diagrams in “AC Electrical Characteristics,” on page 52 for all of the available configurations.

2.4 Jitter Tolerance Improvement Circuit - Frame Boundary Discriminator

To improve the jitter tolerance of the ZL50062/64, a Frame Boundary Discriminator (FBD) circuit was added to the device. This circuit is enabled by setting the Control Register bit FBDEN to HIGH. By default the FBD is disabled.

The FBD can operate in two modes, as controlled by the FBD_MODE[2:0] bits of the Control Register. When bits FBD_MODE[2:0] are set to 000_B, the FBD is set to handle lower frequency jitter only (<8kHz). When bits FBD_MODE[2:0] are set to 111_B, the FBD can handle both low frequency and high frequency jitter. All other values are reserved. These bits are ignored when bit FBDEN is LOW. It is strongly recommended that if bit FBDEN is set HIGH, bits FBD_MODE[2:0] should be set to 111_B to improve the high frequency jitter handling capability.

To achieve the best jitter tolerance performance, it is also recommended that the input data sampling point be optimized. In most applications, the optimum sampling point is 1/2 instead of the default 3/4 (it can be changed by programming all the LIDR and BIDR registers). This will give more allowance for sampling point variations caused

by jitter. There are, however, some cases where data experience more delay than the timing signals. A common example is when multiple data lines are tied together to form bidirectional buses. The large bus loading may cause data to be delayed. If this is the case, the optimum sampling point may be 3/4 or 4/4 instead of 1/2. The optimum sampling point is dependent on the application. The user should optimize the sampling point to achieve the best jitter tolerance performance.

2.5 Input Clock Jitter Tolerance

Input clock jitter tolerance depends on the data rate. In general, the higher the data rate, the smaller the jitter tolerance is, because the period of a bit cell is shorter, and the sampling point variation allowance is smaller.

Jitter tolerance can not be accurately represented by just one number. Jitter of the same amplitude but different frequency spectrum can have different effect on the operation of a device. For example, a device that can tolerate 20ns of jitter of 10kHz frequency may only be able to tolerate 10ns of jitter of 1MHz frequency. Therefore, jitter tolerance should be represented as a spectrum over frequency. The highest possible jitter frequency is half of the carrier frequency. In the case of the ZL50062/64, the input clock is 8.192MHz, and the jitter associated with this clock can have the highest frequency component at 4.096MHz.

For the above reasons, jitter tolerance of the ZL50062/64 has been characterized at 16.384Mbps. The lower data rates (2.048Mbps, 4.096Mbps, 8.192Mbps) will have the same or better tolerance than that of the 16.384Mbps operation. Tolerance of jitter of different frequencies are shown in the “AC Electrical Characteristics“ section, table “Input Clock Jitter Tolerance“ on page 62. The Jitter Tolerance Improvement Circuit was enabled (Control Register, bit FBDEN set HIGH, and bits FBD_MODE[2:0] set to 111_B), and the sampling point was optimized.

3.0 Input and Output Offset Programming

Various registers are used to control the input sampling point (delay) and the output advancement for the Local and Backplane streams. The following sections explain the details of these offset programming features.

3.1 Input Offsets

Control of the Input Bit Delay allows each input stream to have a different frame boundary with respect to the master frame pulse, $\overline{FP8i}$. Each input stream can be individually delayed by up to 7 3/4 bits with a resolution of 1/4 bit of the bit period.

3.1.1 Input Bit Delay Programming (Backplane and Local Input Streams)

Input Bit Delay Registers LIDR0-31 and BIDR0-31 work in conjunction with the SMPL_MODE bit in the Control Register to allow users to control input bit fractional delay as well as input bit sample point selection for greater flexibility when designing switch matrices for high speed operation.

When SMPL_MODE = LOW (input bit fractional delay mode), bits LID[4:0] and BID[4:0] in the LIDR0-31 and BIDR0-31 registers respectively define the input bit fractional delay of the corresponding local and backplane stream. The total delay can be up to 7 3/4 bits with a resolution of 1/4 bit at the selected data rate. When SMPL_MODE = HIGH (sampling point select mode), bits LID[1:0] and BID[1:0] define the input bit sampling point of the stream. The sampling point can be programmed at the 3/4, 4/4, 1/4 or 2/4 bit location to allow better tolerance for input jitter. Bits LID[4:2] and BID[4:2] define the integer input bit delay, with a maximum value of 7 bits at a resolution of 1 bit.

Refer to Figure 9 and Figure 10 for Input Bit Delay Timing at 16Mbps and 8Mbps data rates, respectively.

Refer to Figure 10 for Input Sampling Point Selection Timing at 8Mbps data rates.

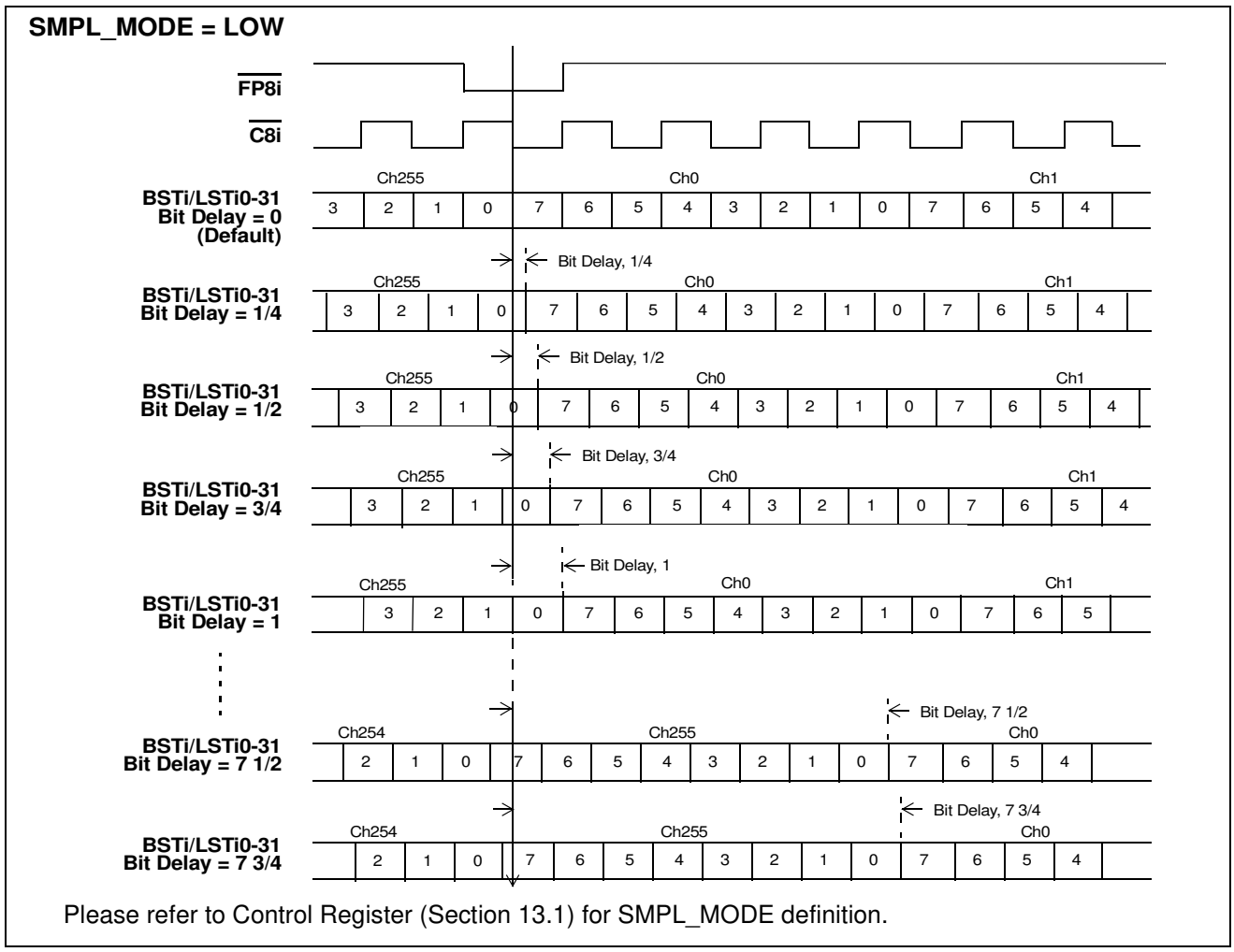

Figure 9 - Backplane and Local Input Bit Delay Timing Diagram for Data Rate of 16Mbps

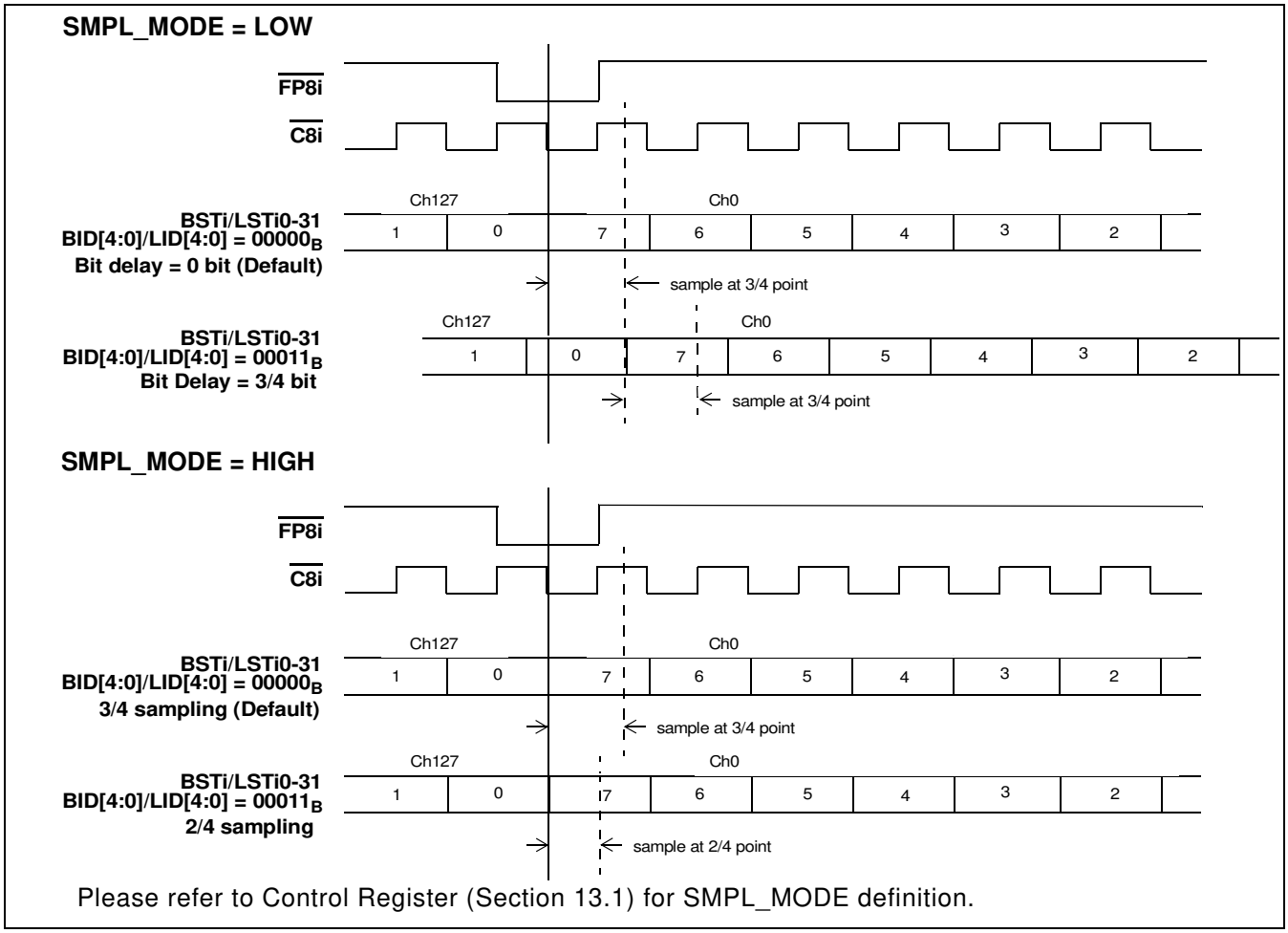

Figure 10 - Backplane and Local Input Bit Delay or Sampling Point Selection Timing Diagram for Data Rate of 8Mbps

3.2 Output Advancement Programming (Backplane and Local Output Streams)

This feature is used to advance the output channel alignment of individual Local or Backplane output streams with respect to the frame boundary $\overline{FP8o}$. Each output stream has its own advancement value that can be programmed by the Output Advancement Registers. The output advancement selection is useful in compensating for various parasitic loading on the serial data output pins.

The Local and Backplane Output Advancement Registers, LOAR0 - LOAR31 and BOAR0 - BOAR31, are used to control the Local and Backplane output advancement respectively. The advancement is determined with reference to the internal system clock rate (131.072MHz). The advancement can be 0, -2 cycles, -4 cycles or -6 cycles, which converts to approximately 0ns, -15ns, -31ns or -46ns as shown in Figure 11.