Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

32 K Channel Digital Switch with High Jitter Tolerance, Rate Conversion per Group of 4 Streams (8, 16, 32 or 64 Mbps), and 128 Inputs and 128 Outputs

Data Sheet

January 2006

Features

- 32,768 channel x 32,768 channel non-blocking digital Time Division Multiplex (TDM) switch at 65.536 Mbps, 32.768 Mbps and 16.384 Mbps or using a combination of rates
- 16,384 channel x 16,384 channel non-blocking digital TDM switch at 8.192 Mbps
- High jitter tolerance with multiple input clock sources and frequencies
- Up to 128 serial TDM input streams, divided into 32 groups with 4 input streams per group
- Up to 128 serial TDM output streams, divided into 32 groups with 4 output streams per group
- Per-group input and output data rate conversion selection at 65.536 Mbps, 32.768 Mbps, 16.384 Mbps and 8.192 Mbps. Input and output data group rates can differ
- Per-group input bit delay for flexible sampling point selection
- Per-group output fractional bit advancement
- Four sets of output timing signals for interfacing additional devices
- Per-channel A-Law/μ-Law Translation

Ordering Information

ZL50073GAC	484 Ball PBGA	Trays
ZL50073GAG2	484 Ball PBGA**	Trays

**Pb Free Tin/Silver/Copper

-40°C to +85°C

- Per-channel constant or variable throughput delay for frame integrity and low latency applications
- Per-stream Bit Error Rate (BER) test circuits
- Per-channel high impedance output control
- Per-channel force high output control
- Per-channel message mode
- Control interface compatible with Intel and Motorola Selectable 32 bit and 16 bit non-multiplexed buses
- Connection Memory block programming
- Supports ST-BUS and GCI-Bus standards for input and output timing
- IEEE 1149.1 (JTAG) test port
- 3.3 V I/O with 5 V tolerant inputs; 1.8 V core voltage

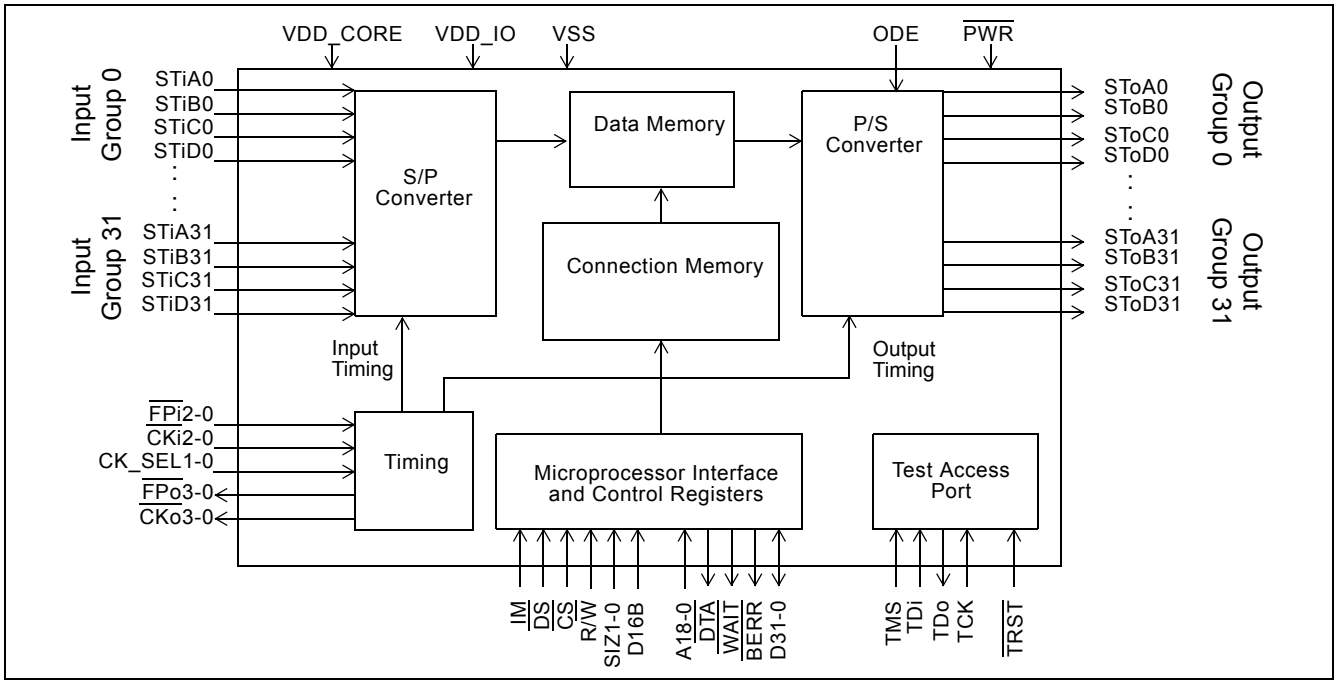

Figure 1 - ZL50073 Functional Block Diagram

Applications

- Large Switching Platforms
- Central Office Switches
- Wireless Base Stations
- Multi-service Access Platforms
- Media Gateways

Description

The ZL50073 is a non-blocking Time Division Multiplex (TDM) switch with maximum 32,768 x 32,768 channels. The device can switch 64 kbps and Nx64 kbps TDM channels from any input stream to any output stream. With a number of enhanced features, the ZL50073 is designed for high capacity voice and data switching applications.

The ZL50073 has 128 input and 128 output data streams which can operate at 8.192 Mbps, 16.384 Mbps, 32.768 Mbps or 65.536 Mbps. The large number of inputs and outputs maintains full 32 K x 32 K channel switching capacity at bit rates of 65 Mbps, 32 Mbps and 16 Mbps. Up to 32 input and output data streams may operate at 65 Mbps. Up to 64 input and output data streams may operate at 32 Mbps. Up to 128 input and output data streams may operate at 16 Mbps or 8 Mbps. The data rate can be independently set in groups of 4 input or output streams. In this way it is possible to provide rate conversion from input data channel to output data channel.

The ZL50073 uses a master clock ($\overline{\text{CKi}}$0) and frame pulse ($\overline{\text{FPi}}$0) to define the TDM data stream frame boundary and timing. A high speed system clock is derived internally from $\overline{\text{CKi}}$0 and $\overline{\text{FPi}}$0. The input and output data streams can independently reference their timings to one of the input clocks or to the internal system clock.

The ZL50073 has a variety of user configurable options designed to provide flexibility when data streams are connected to multiple TDM components or circuits. These include:

- Two additional programmable reference inputs, $\overline{\text{CKi}}$2 - 1 and $\overline{\text{FPi}}$2 - 1, which can be used to provide alternative sources for input and output stream timing
- Variable input bit delay and output advancement, to accommodate delays and frame offsets of streams connected through different data paths
- Four timing outputs, $\overline{\text{CKo}}$3 - 0 and $\overline{\text{FPo}}$3 - 0, which can be configured independently to provide a variety of clock and frame pulse options
- Support of both ST-BUS and GCI-Bus formats

The ZL50073 also has a number of value added features for voice and data applications:

- Per-channel variable delay mode for low latency applications and constant delay mode for frame integrity applications
- Per-channel A-Law/μ-Law Conversions for both voice and data
- 128 separate Pseudo-random Bit Sequence (PRBS) test circuits; one per stream. This provides an integrated Bit Error Rate (BER) test capability to facilitate data path integrity checking

The ZL50073 has two major modes of operation: Connection Mode (normal) and Message Mode. In Connection Mode, data bytes received at the TDM inputs are switched to timeslots in the output data streams, with mapping controlled by the Connection Memories. Using Zarlink's Message Mode capability, microprocessor data can be broadcast to the output data streams on a per-channel basis. This feature is useful for transferring control and status information to external circuits or other TDM devices.

A non-multiplexed microprocessor port provides access to the internal Data Memory, Connection Memory and Control Registers used to program ZL50073 options. The port is configurable to interface with either Motorola or Intel-type microprocessors and is selectable to be either 32 bit or 16 bit.

The mandatory requirements of IEEE 1149.1 standard are supported via the dedicated Test Access Port.

Table of Contents

Table of Contents

List of Figures

List of Tables

Change Summary

The following table captures the changes from the April 2005 issue.

Page	Item	Change
28	10.4.1, “Read Cycle“	Clarified $\overline{\text{WAIT}}$ signal description in Read Cycle.
29	Figure 10 "Read Cycle Operation"	Corrected $\overline{\text{WAIT}}$ signal tristate timing in Read Cycle.
29	10.4.2, “Write Cycle“	Clarified $\overline{\text{WAIT}}$ signal description in Write Cycle.
30	Figure 11 "Write Cycle Operation"	Corrected $\overline{\text{WAIT}}$ signal tristate timing in write Cycle.
43	Table 23 “BER Counter Group and Stream Address Mapping“	Corrected BER Counter Group and Stream Mapping Addresses.

The following table captures the changes from the July 2004 issue.

Page	Item	Change
12	"Pin Description" - CKo0-3	Added special requirement for using output clock at 65.536 MHz.
13	"Pin Description" - $\overline{\text{DTA}}$, $\overline{\text{WAIT}}$	Added more detailed description to the $\overline{\text{DTA}}$ and $\overline{\text{WAIT}}$ pins.
54	“AC Electrical Characteristics1 - FPi0-2 and CKi0-2 Timing“	Added t_{FPIS}, t_{FPIH} (input frame pulse setup and hold) maximum values.
56	Figure 13 "Frame Skew Timing Diagram"	Added $\overline{\text{FPi}}$1,2 frame pulse to Figure “Frame Skew Timing Diagram” to clarify frame boundary skew.
57	(1) “AC Electrical Characteristics1 - FPO0-3 and CKO0-3 (65.536 MHz) Timing“ (2) “AC Electrical Characteristics1 - FPO0-3 and CKO0-3 (32.768 MHz) Timing“ (3) “AC Electrical Characteristics1 - FPO0-3 and CKO0-3 (16.384 MHz) Timing“ (4) “AC Electrical Characteristics1 - FPO0-3 and CKO0-3 (8.192 MHz) Timing“	Added $\overline{\text{CKO}}$0-3 and $\overline{\text{FPO}}$0-3 setup and hold parameters for all different clock rates.
58	“AC Electrical Characteristics - Output Clock Jitter Generation“	Added this table to specify $\overline{\text{CKO}}$0-3 jitter generation.
59	“AC Electrical Characteristics1 - Serial Data Timing2 to CKi“	(1) Values of parameters t_{SIPS}, t_{SIPH}, t_{SINS}, t_{SINH}, t_{SINV}, t_{SIPV}, t_{SIPZ} and t_{SINZ} are revised. (2) Separated parameter t_{CKD} into t_{CKDP} and t_{CKDN}.
60	Figure 16 "Serial Data Timing to CKi"	Added more detail to figure.
61	“AC Electrical Characteristics - Serial Data Timing1 to CKo2“	Values of parameters t_{SOPS}, t_{SOPH}, t_{SONS}, t_{SONH}, t_{SOPV}, t_{SONV}, t_{SOPZ} and t_{SONZ} are revised.
62	Figure 17 "Serial Data Timing to CKo"	Added more detail to figure.
63	“AC Electrical Characteristics - CKo to Other CKo Skew1“	Added $\overline{\text{CKO}}$ skew parameters, t_{CKOS}.
63	Figure 18 "CKo to other CKo Skew"	Added figure to show t_{CKOS}.

Pin Diagram - ZL50073 23 mm x 23 mm 484 Ball PBGA (as viewed through top of package)

A1 corner identified by metallized marking.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
A	$\overline{\text{CKo}}$ [0]	STiA [0]	D[30]	D[25]	D[20]	D[16]	D[15]	D[11]	D[7]	D[4]	D[0]	A[18]	A[14]	A[10]	A[7]	A[2]	A[1]	IC	$\overline{\text{DTA}}$	$\overline{\text{PWR}}$	STOA [31]	TCK
B	STOB [1]	STiD [1]	STOA [0]	D[31]	D[26]	D[21]	D16B	D[13]	D[9]	D[5]	D[3]	A[17]	A[11]	A[8]	A[6]	A[0]	$\overline{\text{BERR}}$	SIZ[0]	STOB [31]	STiA [31]	TDo	STiA [30]
C	STiA [2]	STiA [3]	STiB [1]	STiD [0]	IM	D[27]	D[22]	D[19]	D[12]	D[6]	D[1]	A[15]	A[9]	A[3]	R/$\overline{\text{W}}$	$\overline{\text{CS}}$	$\overline{\text{FPo}}$ [3]	STiD [31]	$\overline{\text{TRST}}$	STOD [30]	STiB [30]	STiD [29]
D	STiC [3]	STiD [2]	STOC [1]	STOD [0]	STOB [0]	STiC [0]	D[28]	D[23]	D[17]	D[8]	A[16]	A[13]	A[5]	$\overline{\text{DS}}$	$\overline{\text{WAIT}}$	STOD [31]	STiB [31]	TDi	STOB [30]	STiC [30]	STOA [29]	STOD [28]
E	STiD [4]	STOB [3]	STiC [2]	STOA [1]	STiA [1]	STOC [0]	STiB [0]	D[24]	D[18]	D[14]	D[2]	A[12]	A[4]	$\overline{\text{CKo}}$ [3]	SIZ[1]	STiC [31]	TMS	STOC [30]	STiD [30]	STOD [29]	STiA [29]	STiB [28]
F	STOB [4]	STOC [3]	STOB [2]	STOD [1]	STiC [1]	V_{SS}	V_{DD_CORE}	D[29]	V_{DD_IO}	V_{DD_CORE}	D[10]	V_{DD_IO}	V_{DD_CORE}	STOC [31]	V_{DD_IO}	V_{SS}	V_{DD_CORE}	STOA [30]	STOC [29]	STiC [29]	STOB [28]	STiA [28]
G	STOD [4]	STOD [3]	STOD [2]	STiB [2]	$\overline{\text{FPo}}$ [0]	V_{DD_IO}	V_{SS}	V_{SS}	V_{DD_CORE}	V_{DD_IO}	V_{SS}	V_{DD_CORE}	V_{DD_IO}	V_{SS}	V_{DD_CORE}	V_{DD_IO}	V_{SS}	STOB [29]	STiB [29]	STiC [28]	$\overline{\text{CKi}}$ [2]	STiD [27]
H	STiA [5]	STiA [4]	STiD [3]	STOC [2]	STOA [2]	V_{DD_CORE}	V_{DD_IO}	V_{SS}	V_{SS}	V_{DD_CORE}	V_{DD_IO}	V_{SS}	V_{DD_CORE}	V_{DD_IO}	V_{SS}	V_{DD_CORE}	STOA [28]	STOC [28]	STiD [28]	STOD [27]	STiC [27]	STiA [27]
J	STiB [5]	$\overline{\text{CKi}}$ [1]	STiC [4]	STOA [3]	STiB [3]	V_{DD_IO}	V_{DD_CORE}	V_{DD_IO}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DD_IO}	V_{SS}	V_{DD_IO}	STOB [27]	STOC [27]	STiB [27]	IC	STOC [26]
K	STOB [5]	STiD [5]	$\overline{\text{FPi}}$ [1]	STOC [4]	STOA [4]	STiB [4]	V_{SS}	V_{DD_CORE}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DD_CORE}	V_{DD_IO}	V_{DD_CORE}	STOA [27]	$\overline{\text{FPi}}$ [2]	STOA [26]	STOB [26]	STiD [26]
L	ODE	STOD [5]	STOC [5]	STiD [6]	STiC [5]	V_{DD_CORE}	V_{DD_IO}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DD_CORE}	STOD [26]	STiC [26]	STiB [26]	STiA [26]	STOD [25]	STOC [25]
M	STiA [6]	STiB [6]	STiC [6]	STiC [7]	STOA [5]	V_{DD_IO}	V_{DD_CORE}	V_{DD_IO}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DD_IO}	V_{SS}	V_{DD_IO}	STiA [25]	STiD [25]	STOB [25]	STOA [25]	IC
N	STOB [6]	STOC [6]	STOD [6]	STOA [7]	STOA [6]	V_{SS}	V_{SS}	V_{DD_CORE}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DD_CORE}	V_{DD_IO}	STOD [23]	STOC [24]	STiD [24]	STOB [24]	STiB [25]	STiC [25]
P	STiA [7]	STiB [7]	STOB [7]	STiA [8]	STOA [8]	V_{DD_CORE}	V_{DD_IO}	V_{DD_IO}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DD_IO}	V_{DD_CORE}	V_{DD_CORE}	STOA [23]	STiC [23]	STiB [24]	STOA [24]	STOD [24]
R	STiD [7]	STOC [7]	IC	STOB [8]	STiB [8]	V_{DD_IO}	V_{DD_CORE}	V_{SS}	V_{SS}	V_{DD_CORE}	V_{DD_IO}	V_{SS}	V_{DD_CORE}	V_{DD_IO}	V_{SS}	V_{SS}	V_{DD_IO}	$\overline{\text{CKo}}$ [2]	STiD [22]	STiB [23]	STiA [24]	STiC [24]
T	STOD [7]	V_{SS}	STOC [8]	STiD [9]	STiB [10]	STOD [9]	V_{SS}	V_{SS}	V_{DD_CORE}	V_{DD_IO}	V_{SS}	V_{DD_CORE}	V_{SS}	V_{SS}	V_{DD_CORE}	V_{DD_IO}	V_{SS}	STOA [21]	$\overline{\text{FPo}}$ [2]	STOC [22]	STiD [23]	STOC [23]
U	STiC [8]	STOD [8]	STiC [9]	STiA [10]	STOC [10]	V_{SS}	V_{DD_IO}	STOC [12]	V_{DD_IO}	V_{DD_CORE}	STiA [16]	V_{DD_IO}	V_{DD_CORE}	STOA [18]	V_{DD_IO}	STiC [19]	V_{DD_CORE}	STOC [20]	STiD [21]	STiC [22]	STOD [22]	STOB [23]
V	STiD [8]	STiB [9]	STOC [9]	STOB [10]	STOD [10]	STOB [11]	STiC [12]	STiB [13]	STOA [13]	STiC [15]	STOB [16]	STOC [16]	IC	CK_SEL[1]	STiB [18]	STOA [19]	STiA [20]	STOB [20]	STOD [20]	STOC [21]	STOA [22]	STiA [23]
W	STiA [9]	STOB [9]	STiD [10]	STiA [11]	STOA [11]	STiB [12]	STOD [12]	STiC [13]	STiA [14]	STOD [14]	STOC [15]	$\overline{\text{CKi}}$ [0]	IC	STOB [17]	CK_SEL[0]	STOC [18]	STiD [19]	STOD [19]	STiD [20]	STiC [21]	STiA [22]	STOB [22]
Y	STOA [9]	STOA [10]	STiB [11]	STOC [11]	STOA [12]	$\overline{\text{FPo}}$ [1]	STiD [13]	STiB [14]	STOB [14]	STiD [15]	STOD [15]	STOD [16]	IC	STiC [17]	STOC [17]	STiA [18]	STOB [18]	STiB [19]	STiB [20]	STOA [20]	STOB [21]	STiB [22]
AA	STiC [10]	STiC [11]	STOD [11]	STiD [12]	STiA [13]	STOB [13]	STOD [13]	STOA [14]	STiA [15]	STOA [15]	STiB [16]	STOA [16]	$\overline{\text{FPi}}$ [0]	STiA [17]	STOA [17]	IC	IC	STOD [18]	STOB [19]	STOC [19]	STiA [21]	STOD [21]
AB	STiD [11]	STiA [12]	STOB [12]	$\overline{\text{CKo}}$ [1]	STOC [13]	STiC [14]	STiD [14]	STOC [14]	STiB [15]	STOB [15]	STiC [16]	STiD [16]	NC	NC	STiB [17]	STiD [17]	STOD [17]	STiC [18]	STiD [18]	STiA [19]	STiC [20]	STiB [21]

Pin Description

Pin	Name	Description
TDM Interface		
F7, F10, F13, F17, G9, G12, G15, H6, H10, H13, H16, J7, K8, K15, K17, L6, L16, M7, N8, N15, P6, P16, P17, R7, R10, R13, T9, T12, T15, U10, U13, U17	V_{DD_CORE}	**Power Supply for the Core Logic:** +1.8 V
F9, F12, F15, G6, G10, G13, G16, H7, H11, H14, J6, J8, J15, J17, K16, L7, M6, M8, M15, M17, N16, P7, P8, P15, R6, R11, R14, R17, T10, T16, U7, U9, U12, U15	V_{DD_IO}	**Power Supply for the I/O:** +3.3 V
F6, F16, G7, G8, G11, G14, G17, H8, H9, H12, H15, J9, J10, J11, J12, J13, J14, J16, K7, K9, K10, K11, K12, K13, K14, L8, L9, L10, L11, L12, L13, L14, L15, M9, M10, M11, M12, M13, M14, M16, N6, N7, N9, N10, N11, N12, N13, N14, P9, P10, P11, P12, P13, P14, R8, R9, R12, R15, R16, T2, T7, T8, T11, T13, T14, T17, U6	V_{SS}	**Ground**
A2, E5, C1, C2, H2, H1, M1, P1, P4, W1, U4, W4, AB2, AA5, W9, AA9, U11, AA14, Y16, AB20, V17, AA21, W21, V22, R21, M18, L20, H22, F22, E21, B22, B20	STiA0-31	**Serial TDM Input Data 'A' Streams (5 V Tolerant Input with Internal Pull-down)** The data rate of these input streams can be selected in a group of 4 to be either 8.192 Mbps, 16.384 Mbps, 32.678 Mbps or 65.536 Mbps. Refer to Section 1.4 for rate programming options. The data streams can be selected to be either inverted or non-inverted, programmed by the Group Control Registers (Section 14.4). Unused inputs are pulled low by internal pull-down resistors and may be left unconnected.
E7, C3, G4, J5, K6, J1, M2, P2, R5, V2, T5, Y3, W6, V8, Y8, AB9, AA11, AB15, V15, Y18, Y19, AB22, Y22, R20, P20, N21, L19, J20, E22, G19, C21, D17	STiB0-31	**Serial TDM Input Data 'B' Streams (5 V Tolerant Input with Internal Pull-down)** The data rate of these input streams can be selected in a group of 4 to be either 8.192 Mbps, 16.384 Mbps or 32.678 Mbps. The stream is unused when its input group rate is 65.536 Mbps. Refer to Section 1.4 for rate programming options. The data streams can be selected to be either inverted or non-inverted, programmed by the Group Control Registers (Section 14.4). Unused inputs are pulled low by internal pull-down resistors and may be left unconnected.

Pin Description (continued)

Pin	Name	Description
D6, F5, E3, D1, J3, L5, M3, M4, U1, U3, AA1, AA2, V7, W8, AB6, V10, AB11, Y14, AB18, U16, AB21, W20, U20, P19, R22, N22, L18, H21, G20, F20, D20, E16	STiC0-31	**Serial TDM Input Data 'C' Streams (5 V Tolerant Input with Internal Pull-down)** The data rate of these input streams can be selected in a group of 4 to be either 8.192 Mbps or 16.384 Mbps. The stream is unused when its input group rate is 65.536 Mbps or 32.678 Mbps. Refer to Section 1.4 for rate programming options. The data streams can be selected to be either inverted or non-inverted, programmed by the Group Control Registers (Section 14.4). Unused inputs are pulled low by internal pull-down resistors and may be left unconnected.
C4, B2, D2, H3, E1, K2, L4, R1, V1, T4, W3, AB1, AA4, Y7, AB7, Y10, AB12, AB16, AB19, W17, W19, U19, R19, T21, N19, M19, K22, G22, H19, C22, E19, C18	STiD0-31	**Serial TDM Input Data 'D' Streams (5 V Tolerant Input with Internal Pull-down)** The data rate of these input streams can be selected in a group of 4 to be either 8.192 Mbps or 16.384 Mbps. The stream is unused when its input group rate is 65.536 Mbps or 32.678 Mbps. Refer to Section 1.4 for rate programming options. The data streams can be selected to be either inverted or non-inverted, programmed by the Group Control Registers (Section 14.4). Unused inputs are pulled low by internal pull-down resistors and may be left unconnected.
B3, E4, H5, J4, K5, M5, N5, N4, P5, Y1, Y2, W5, Y5, V9, AA8, AA10, AA12, AA15, U14, V16, Y20, T18, V21, P18, P21, M21, K20, K18, H17, D21, F18, A21	SToA0-31	**Serial TDM Output Data 'A' Streams (5 V Tolerant, 3.3 V Tri-state Slew-Rate Controlled Outputs)** The data rate of these output streams can be selected in a group of 4 to be either 8.192 Mbps, 16.384 Mbps, 32.678 Mbps or 65.536 Mbps. Refer to Section 1.4 for rate programming options. The data streams can be selected to be either inverted or non-inverted, programmed by the Group Control Registers (Section 14.4).
D5, B1, F3, E2, F1, K1, N1, P3, R4, W2, V4, V6, AB3, AA6, Y9, AB10, V11, W14, Y17, AA19, V18, Y21, W22, U22, N20, M20, K21, J18, F21, G18, D19, B19	SToB0-31	**Serial TDM Output Data 'B' Streams (5 V Tolerant, 3.3 V Tri-state Slew-Rate Controlled Outputs)** The data rate of these output streams can be selected in a group of 4 to be either 8.192 Mbps, 16.384 Mbps or 32.678 Mbps. The stream is unused when its output group rate is 65.536 Mbps. Refer to Section 1.4 for rate programming options. The data streams can be selected to be either inverted or non-inverted, programmed by the Group Control Registers (Section 14.4). Unused outputs are tristated and may be left unconnected.
E6, D3, H4, F2, K4, L3, N2, R2, T3, V3, U5, Y4, U8, AB5, AB8, W11, V12, Y15, W16, AA20, U18, V20, T20, T22, N18, L22, J22, J19, H18, F19, E18, F14	SToC0-31	**Serial TDM Output Data 'C' Streams (5 V Tolerant, 3.3 V Tri-state Slew-Rate Controlled Outputs)** The data rate of these output streams can be selected in a group of 4 to be either 8.192 Mbps or 16.384 Mbps. The stream is unused when its output group rate is 65.536 Mbps or 32.678 Mbps. Refer to Section 1.4 for rate programming options. The data streams can be selected to be either inverted or non-inverted, programmed by the Group Control Registers (Section 14.4). Unused outputs are tristated and may be left unconnected.

Pin Description (continued)

Pin	Name	Description
D4, F4, G3, G2, G1, L2, N3, T1, U2, T6, V5, AA3, W7, AA7, W10, Y11, Y12, AB17, AA18, W18, V19, AA22, U21, N17, P22, L21, L17, H20, D22, E20, C20, D16	SToD0-31	**Serial TDM Output Data 'D' Streams (5 V Tolerant, 3.3 V Tri-state Slew-Rate Controlled Outputs)** The data rate of these output streams can be selected in a group of 4 to be either 8.192 Mbps or 16.384 Mbps. The stream is unused when its output group rate is 65.536 Mbps or 32.678 Mbps. Refer to Section 1.4 for rate programming options. The data streams can be selected to be either inverted or non-inverted, programmed by the Group Control Registers (Section 14.4). Unused outputs are tristated and may be left unconnected.
W12	$\overline{\text{CKi}}$0	**ST-BUS/GCI-Bus Clock Input (5 V Tolerant Schmitt-Triggered Input)** This pin accepts an 8.192 MHz, 16.384 MHz, 32.678 MHz or 65.536 MHz clock. This clock must be provided for correct operation of the ZL50073. The frequency of the $\overline{\text{CKi}}$0 input is selected by the CK_SEL1-0 inputs. The active clock edge may be either rising or falling, programmed by the Input Clock Control Register (Section 14.5).
AA13	$\overline{\text{FPi}}$0	**ST-BUS/GCI-Bus Frame Pulse Input (5 V Tolerant Input)** This pin accepts the 8 kHz frame pulse which marks the frame boundary of the TDM data streams. The pulse width is nominally one $\overline{\text{CKi}}$0 clock period (assuming ST-BUS mode) selected by the CK_SEL1-0 inputs. The active state of the frame pulse may be either high or low, programmed by the Input Clock Control Register (Section 14.5).
J2, G21	$\overline{\text{CKi}}$1-2	**ST-BUS/GCI-Bus Clock Inputs (5 V Tolerant Schmitt Triggered Inputs)** These optional TDM clock inputs are at 8.192 MHz, 16.384 MHz, 32.678 MHz or 65.536 MHz. The frequency of each clock input is automatically detected by the ZL50073. Refer to Section 2.0 for TDM timing options. The active clock edge may be either rising or falling, programmed by the Input Clock Control Register (Section 14.5). Unused inputs must be connected to a defined logic level.
K3, K19	$\overline{\text{FPi}}$1-2	**ST-BUS/GCI-Bus Frame Pulse Inputs (5 V Tolerant Inputs)** These 8 kHz input pulses correspond to the optional $\overline{\text{CKi}}$2-1 clock inputs. The frame pulses mark the frame boundary of the TDM data streams. Refer to Section 2.0 for TDM timing options. Each pulse width is nominally one $\overline{\text{CKi}}$ clock period (assuming ST-BUS mode). The active state of the frame pulse may be either high or low, programmed by the Input Clock Control Register (Section 14.5). Unused inputs must be connected to a defined logic level.

Pin Description (continued)

Pin	Name	Description
A1, AB4, R18, E14	$\overline{CKo}$0-3	**ST-BUS/GCI-Bus Clock Outputs (3.3 V Outputs with Slew-Rate Control)** These clock outputs can be programmed to generate 8.192 MHz, 16.384 MHz, 32.678 MHz or 65.536 MHz TDM clock outputs. The active edge can be programmed to be either rising or falling. The source of the clock outputs can be derived from either the $\overline{CKi}$2-0 inputs or the internal system clock. The frequency, active edge and source of each clock output can be programmed independently by the Output Clock Control Register (Section 14.6). For 65.536 MHz output clock, the total loading on the output should not be larger than 10pF.
G5, Y6, T19, C17	$\overline{FPo}$0-3	**ST-BUS/GCI-Bus Frame Pulse Outputs (3.3 V Outputs with Slew-Rate Control)** These 8 kHz output pulses mark the frame boundary of the TDM data streams. The pulse width is nominally one clock period of the corresponding $\overline{CKo}$ output. The active state of each frame pulse may be either high or low, independently programmed by the Output Clock Control Register (Section 14.6).
W15, V14	CK_SEL0-1	**Master Clock Input Select (5 V Tolerant Inputs)** Inputs used to select the frequency and frame alignment of $\overline{CKi}$0 and $\overline{FPi}$0: CK_SEL1 = 0, CK_SEL0 = 0, 8.192 MHz CK_SEL1 = 0, CK_SEL0 = 1, 16.384 MHz CK_SEL1 = 1, CK_SEL0 = 0, 32.768 MHz CK_SEL1 = 1, CK_SEL0 = 1, 65.536 MHz
L1	ODE	**Output Drive Enable (5 V Tolerant Input with Internal Pull-up)** This is the asynchronous output enable control for the output streams. When it is high, the streams are enabled. When it is low, the output streams are tristated.
A18, J21, M22, R3, V13, W13, Y13, AA16, AA17	IC	**Internal Connections** In normal mode these pins **MUST** be connected low
AB13, AB14	NC	**No Connection** In normal mode these pins **MUST** be left unconnected
Microprocessor Port and Reset		
A11, C11, E11, B11, A10, B10, C10, A9, D10, B9, F11, A8, C9, B8, E10, A7, A6, D9, E9, C8, A5, B6, C7, D8, E8, A4, B5, C6, D7, F8, A3, B4	D0-31	**Microprocessor Port Data Bus (5 V Tolerant Bi-directional with Slew-Rate Output Control)** 32 or 16 bit bidirectional data bus. Used for microprocessor access to internal memories and registers. When 16 bit mode is selected (D16B is logic 1), D31-16 are unused and must be connected to defined logic levels.
B16, A17, A16, C14, E13, D13, B15, A15, B14, C13, A14, B13, E12, D12, A13, C12, D11, B12, A12	A0-18	**Microprocessor Port Address Bus (5 V Tolerant Inputs)** 19 bit address bus for the internal memories and registers. In 16 bit bus mode (D16B is logic 1), please note A0 is not used and must be connected to a defined logic level. In Intel 32 bit mode: A1 = BE_3, A0 = BE_2

Pin Description (continued)

Pin	Name	Description
C16	$\overline{CS}$	**Chip Select Input (5 V Tolerant Input)** Active low input used with $\overline{DS}$ to enable read and write access to the ZL50073.
D14	$\overline{DS}$	**Data Strobe Input (5 V Tolerant Input)** Active low input used with $\overline{CS}$ to enable read and write access to the ZL50073.
C15	R/$\overline{W}$	**Read/Write Input (5 V Tolerant Input)** This input controls the direction of the data bus lines (D31 - 0) during a microprocessor access. This pin is set high and low for the read and write access respectively.
A19	$\overline{DTA}$	**Data Transfer Acknowledge (5 V Tolerant, 3.3 V Tri-state Output with Slew-Rate)** This active low output indicates that a data bus transfer is complete. Usually used with a Motorola interface. An external pull-up resistor is required to hold this pin HIGH when output is high-impedance.
B17	$\overline{BERR}$	**Transfer Bus Error Output with Slew Rate Control (5 V Tolerant, 3.3 V Tri-state Outputs with Slew-Rate Control)** This pin goes low whenever the microprocessor attempts to access an invalid memory space inside the device. In Motorola bus mode, if this bus error signal is activated, the data transfer acknowledge signal, $\overline{DTA}$, will not be generated. In Intel bus mode, the generation of the $\overline{DTA}$ is not affected by this $\overline{BERR}$ signal. An external pull-up resistor is required to hold a HIGH level when output is high-impedance.
D15	$\overline{WAIT}$	**Data Transfer Wait Output (5 V Tolerant, 3.3 V Tri-state Output with Slew Rate)** Active low wait signal output. It indicates that a data bus transfer is complete when it goes from low to high. Usually used with an Intel interface. An external pull-up resistor is required to hold this pin HIGH when output is high-impedance
B18, E15	SIZ0-1	**Data Transfer Size/Upper and Lower Data Strobe Inputs (5 V Tolerant Inputs)** Motorola 32-bit mode - signals indicate data transfer size, refer to Section 10.0. Motorola 16-bit mode:SIZ0 - $\overline{LDS}$, SIZ1 - $\overline{UDS}$. Active low upper and lower data strobes, $\overline{UDS}$ and $\overline{LDS}$, indicate whether the upper byte, D15 - 8, and/or lower byte, D7 - 0, is being accessed. Intel 32/16-bit mode: SIZ0 - $\overline{BE0}$, SIZ1 - $\overline{BE1}$. Active low Intel type bus-enable signals, $\overline{BE1}$ and $\overline{BE0}$
C5	IM	**Microprocessor Port Bus Mode Select (5 V Tolerant Input)** Control input: 0 = Motorola mode 1 = Intel mode

Pin Description (continued)

Pin	Name	Description
B7	D16B	**Microprocessor Port Bus 16/32 Bit Mode Select (5 V Tolerant Input with Internal Pull-down)** Control input: 0 = 32 bit data bus 1 = 16 bit data bus
A20	$\overline{\text{PWR}}$	**Device Reset (5 V Tolerant Schmitt-Triggered Input)** Asynchronous reset input used to initialize the ZL50073. 0 = Reset 1 = Normal See Section 11.0, Power-up and Initialization of the ZL50073 for detailed description of Reset state.
IEEE 1149.1 Test Access Port (TAP)		
D18	TDi	**Test Data (5 V Tolerant Input with Internal Pull-up)** Serial test data input. When not used, this input may be left unconnected.
B21	TDo	**Test Data (3.3 V Output)** Serial test data output.
A22	TCK	**Test Clock (5 V Tolerant Schmitt-Triggered Input with Internal Pull-up)** Provides the clock to the JTAG test logic
C19	$\overline{\text{TRST}}$	**Test Reset (5 V Tolerant Schmitt-Triggered Input with Internal Pull-up)** Asynchronously initializes the JTAG TAP controller by putting it in the Test-Logic-Reset state. This pin should be pulsed low during power-up to ensure that the device is in the normal functional mode. When JTAG is not being used, this pin should be pulled low during normal operation.
E17	TMS	**Test Mode Select (5 V Tolerant Input with Internal Pull-up)** JTAG signal that controls the state transitions of the TAP controller. When not used, this pin is pulled high by an internal pull-up resistor and may be left unconnected.

1.0 Functional Description

1.1 Overview

The device has 128 ST-BUS/GCI-Bus inputs (STiA0 - 31, STiB0 - 31, STiC0 - 31, STiD0 - 31) and 128 ST-BUS/GCI-Bus outputs (SToA0 - 31, SToB0 - 31, SToC0 - 31, SToD0 - 31). It is a non-blocking digital switch with 32,768 64 kbps channels and is capable of performing rate conversion between groups of 4 inputs and 4 outputs. The inputs accept serial input data streams with data rates of 8.192 Mbps, 16.384 Mbps, 32.768 Mbps or 65.536 Mbps. There are 32 input groups with each group consisting of 4 streams (‘A’, ‘B’, ‘C’ and ‘D’). Each group can be set to any of the data rates. The outputs deliver serial data streams with data rates of 8.192 Mbps, 16.384 Mbps, 32.768 Mbps or 65.536 Mbps. There are 32 output groups with each group consisting of 4 streams (‘A’, ‘B’, ‘C’ and ‘D’). Each group can be set to any of the data rates.

By using Zarlink’s message mode capability, the microprocessor can store data in the connection memory which can be broadcast to the output streams on a per-channel basis. This feature is useful for transferring control and status information for external circuits or other ST-BUS/GCI-Bus devices.

The ZL50073 uses the ST-BUS/GCI-Bus master input frame pulse ($\overline{FPi0}$) and the ST-BUS/GCI-Bus master input clock ($\overline{CKi0}$) to define the input frame boundary and timing for sampling the ST-BUS/GCI-Bus input streams with various data rates (8.192 Mbps, 16.384 Mbps, 32.768 Mbps or 65.536 Mbps). The rate of the input clock is defined by setting the CK_SEL1 - 0 pins. In addition, two more frame pulses and clocks can be accepted. The frequencies of these signals are automatically detected by the ZL50073.

A selectable Motorola or Intel compatible non-multiplexed microprocessor port allows users to program the device to operate in various modes under different switching configurations. Users can use the microprocessor port to perform internal register and memory read and write operations. The microprocessor port can be selectable to be either a 32 bit or 16 bit data bus and to have either a 19 bit or 17 bit address bus. This is selected by setting the D16B pin. There are seven control signals ($\overline{CS}$, $\overline{DS}$, R/$\overline{W}$, $\overline{DTA}$, $\overline{WAIT}$, $\overline{BERR}$ and IM).

The device supports the mandatory requirements for the IEEE 1149.1 (JTAG) standard via the test port.

1.2 Switch Operation

The ZL50073 switches 64 kbps and Nx64 kbps data and voice channels from the TDM input streams, to timeslots in the TDM output streams. The device is non-blocking; all 32 K input channels can be switched through to the outputs. Any input channel can be switched to any available output channel.

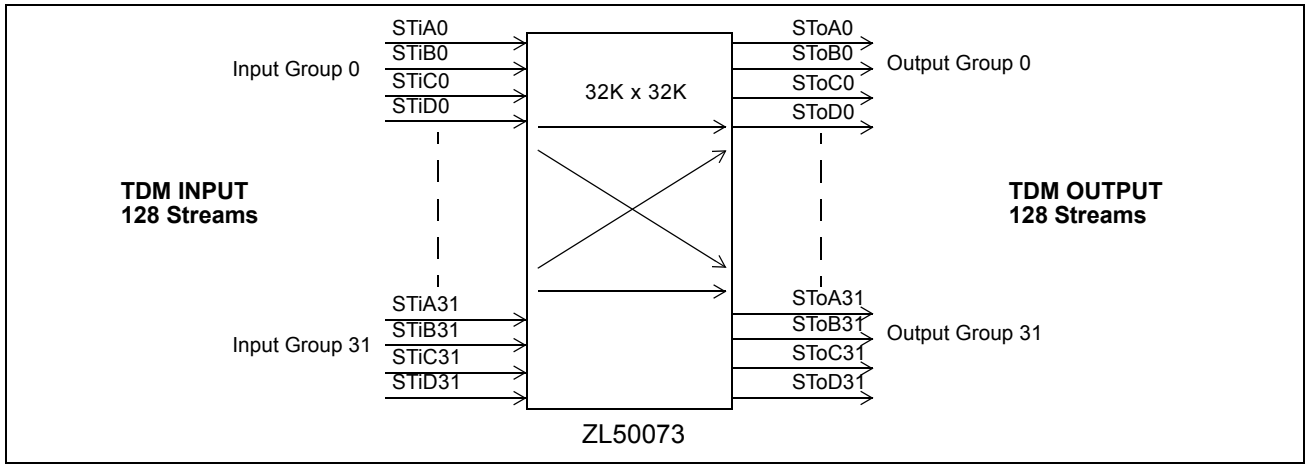

Figure 2 - 32 K x 32 K Channel Basic Switch Configuration

The maximum channel switching capacity is determined by the number of streams and their rate of operation, as shown in Table 1.

TDM Group Data Rate	Maximum Number of Input TDM Data Streams	Maximum Number of Output TDM Data Streams	Number of 64 kbps Channels per Stream	Maximum Switch Capacity† (streams x channels = total)
65.536 Mbps	32	32	1024	32 x 1024 = 32,768
32.768 Mbps	64	64	512	64 x 512 = 32,768
16.384 Mbps	128	128	256	128 x 256 = 32,768
8.192 Mbps	128	128	128	128 x 128 = 16,384‡

Table 1 - Data Rate and Maximum Switch Size

† The maximum capacity shown is when all streams are at the same rate, and none are operating at 8.192 Mbps.

‡ Switch capacity is limited to less than 32 K channels, only when streams are provisioned at 8 Mbps. The maximum switch capacity in this case is given by 32,768 - (N x 128), where N is the number of 8 Mbps input or output streams.

1.3 Stream Provisioning

The ZL50073 is a large switch with a comprehensive list of user configurable, ’per-group’ programmable features. In order to facilitate ease of use, the ZL50073 offers a simple programming model. Streams are grouped in sets of four, with each group sharing the same configured characteristics. In this way it is possible to reduce programming complexity, while still maintaining flexible ’per-group’ configuration options:

- Input and output rate selection; see Section 1.4
- Input stream clock source selection; see Section 2.0
- Output stream clock source selection; see Section 2.0
- Input stream sampling point selection; see Section 5.1
- Output stream fractional bit advance; see Section 5.2
- Input and output stream inversion control; see Section 14.4

The streams are grouped, one from the TDM ’A’ streams, combined with the corresponding ’B’, ’C’ and ’D’ streams. For example, input stream group #12 is STiA12, STiB12, STiC12, STiD12, and output stream group #4 is SToA4, SToB4, SToC4, SToD4. There are 32 input and 32 output groups. Depending on the data rate set for the group there will be between 1 and 4 streams activated. If the data rate is set for 65.536 Mbps, the ‘A’ stream will be activated and the ‘B’, ‘C’ and ‘D’ streams will not be activated. If the data rate is set for 32.768 Mbps, the ‘A’ and ‘B’ streams will be activated and the ‘C’ and ‘D’ streams will not be activated. If the data rate is set for either 16.384 Mbps or 8.192 Mbps all of the streams, ‘A’, ‘B’, ‘C’ and ‘D’ will be activated. The maximum channel capacity of a group is 1024 channels when operating at any data rate except for 8.192 Mbps, in which case the maximum operating channel capacity decreases to 512 channels.

1.4 Input and Output Rate Selection

Table 1 shows the maximum number of streams available at different bit rates. The ZL50073 deactivates unused streams when operating at the higher bit rates as shown in Table 2.

Input or Output Group n (n = 0 - 31)	65 Mbps	32 Mbps	16 Mbps	8 Mbps
STiAn / SToAn	Active	Active	Active	Active
STiBn / SToBn	Not Active	Active	Active	Active
STiCn / SToCn	Not Active	Not Active	Active	Active
STiDn / SToDn	Not Active	Not Active	Active	Active

Table 2 - TDM Stream Bit Rates

For 65 Mbps operation, only those inputs and outputs in the TDM ’A’ streams are active. For 32 Mbps operation, only those inputs and outputs in the TDM ’A’ and ’B’ streams are active. For 16 Mbps and 8 Mbps, inputs and outputs in TDM ’A’, ’B’, ’C’ and ’D’ streams are active.

Note that if the internal system clock is not used as the clock source, there are limitations on the maximum data rate. See Section 2.0 for more details.

1.4.1 Per Group Rate Selection

See Section 14.4, Group Control Registers, for programming details. The data rates are set with the Input Stream Bit Rate (bits 3 - 2) and the Output Stream Bit Rate (bits 19 - 18) in the Group Control Registers 0 - 31 (GCR0 - 31)

For the ZL50073, the bit rates of the inputs and outputs are programmed independently, in groups of 4 streams. Depending on the rate programmed, the active streams in the group will be as indicated in Table 2.

For example:

- if input stream group #1 is programmed for 65 Mbps: STiA1 is active; STiB1, STiC1, STiD1 are not active
- if output stream group #15 is programmed for 32 Mbps: SToA15 and SToB15 are active; SToC15 and SToD15 are not active
- if input stream group #24 is programmed for 16 Mbps or 8 Mbps, STiA24, STiB24, STiC24, STiD24 are all active

An example of ZL50073 mixed rate provisioning is given in Figure 3. In this example, the output streams follow the same data rate as the input streams. The example shows that it is possible to have different groups operating at different data rates. The first eight groups are operating in 65.536 Mbps mode (8192 channels - 8 streams), the next eight groups are operating in 32.768 Mbps (8192 channels - 16 streams with 2 streams in each group) and the remaining sixteen groups are operating in 16.384 Mbps (16384 channels - 64 streams with 4 streams per group). This results in the full capacity usage of the ZL50073.

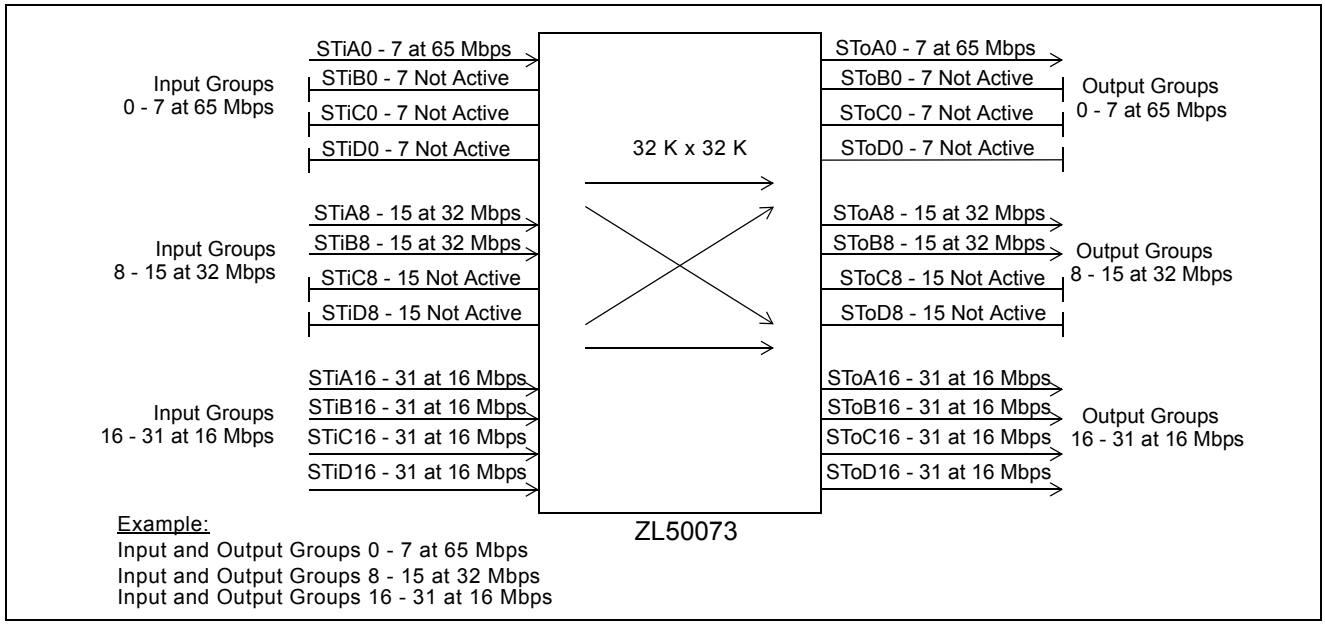

Figure 3 - ZL50073 32 K x 32 K Channel and Stream Provisioning Example at Multiple Rates

Note: Although this example shows the same rate provisioned for corresponding STi and STo streams, programming of input and outputs is independent and different settings are possible.

1.5 Rate Conversion

The ZL50073 supports rate conversion from any input stream rate to any output stream rate.

An example of ZL50073 rate conversion is given in Figure 4. Here the total capacity of both the input and the output is 32,768 channels. The output stream rates do not have to follow the input stream rates. In this example, on the input side of the switch you have 24 streams operating at 65.536 Mbps (24,576 channels - 24 groups with 1 stream in each group), 8 streams operating at 32.768 Mbps (4096 channels - 4 groups with 2 streams in each group) and 16 streams operating at 16.384 Mbps (4096 channels - 4 groups with 4 streams in each group) with no streams operating at 8.192 Mbps. This results in a maximum input capacity of 32,768 input channels. As the output streams do not have to follow the input streams, they can be configured so that 15 streams operate at 65.536 Mbps (15,360 channels - 15 groups with 1 stream in each group), 28 streams operate at 32.768 Mbps (14,336 channels - 14 groups with 2 streams in each group), 12 streams operate at 16.384 Mbps (3076 channels - 3 groups with 4 streams in each group) and no streams at 8.192 Mbps. This results in a maximum output capacity of 32,768 output channels. The reason that no stream is operating at 8.192 Mbps is that as soon as one group is set to this data rate, the capacity of the device will be less than the full 32,768 channels.

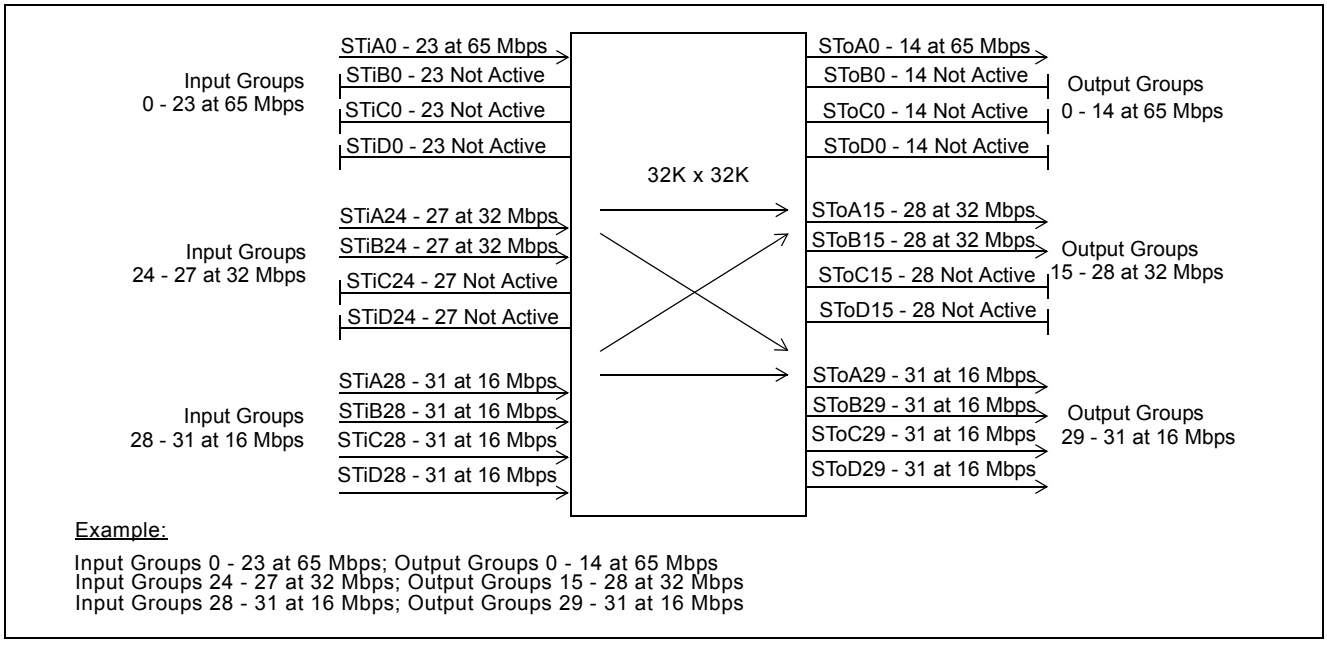

Figure 4 - Input and Output Data Rate Conversion Example

2.0 Input Clock ($\overline{CKi}$) and Input Frame Pulse ($\overline{FPi}$) Timing

The input timing for the ZL50073 can be set for one of four different frequencies. They can also be set for ST-BUS or GCI-Bus mode with positive or negative input. The $\overline{CKi}0$ and $\overline{FPi}0$ input timing must be provided in order for the device to be used. There are two additional input clocks and frame pulses that can be provided. $\overline{CKi}0$ is used to generate the internal clock. This clock is used for all the internal logic and can be used as one of the clocks that defines the timing for the input and output data. The input stream clock source is selected by the ISSRC1 - 0 (bits 1 - 0) in the Group Control Registers. The output stream clock source is selected by the OSSRC1 - 0 (bits 17 - 16) in the Group Control Registers.

The $\overline{CKi}0$ and $\overline{FPi}0$ input frequency is set via the CK_SEL1 - 0 pins as shown in Table 3. By default the $\overline{CKi}0$ and $\overline{FPi}0$ pins accept ST-BUS, negative input timing. The input frame pulse format (ST-BUS/GCI-Bus), frame pulse polarity, and clock polarity can be programmed by the GCISEL0 (bit 2), FPIPOL0 (bit 1), and CKIPSL0 (bit 0) in the Input Clock Control Register (ICCR), as described in Section 14.5.

CK_SEL1	CK_SEL0	Input $\overline{CKi}0$ and $\overline{FPi}0$
0	0	8.192 MHz
0	1	16.384 MHz
1	0	32.768 MHz
1	1	65.536 MHz

Table 3 - $\overline{CKi}0$ and $\overline{FPi}0$ Setting via CK_SEL1 - 0

Two additional input clocks ($\overline{CKi}2$ - 1) and frame pulses ($\overline{FPi}2$ - 1) can be accepted. These signals can be 8.192 MHz, 16.384 MHz, 32.768 MHz or 65.536 MHz and the rates are automatically detected by the device. These clocks and their frame boundaries must be phase aligned with the $\overline{CKi}0$ and its frame boundary within a 30 ns skew but can have different jitter values. The clocks do not have to have the same frequency. If these additional clocks are not used, the pins must be connected to a defined logic level.

These additional input clocks and frame pulses can be used as alternative clock sources for the input streams, output streams, and output clocks / frame pulses. The input streams' clock sources are controlled by the ISSRC1-0 (bits 1 - 0) in the Group Control Registers (GCR). The output streams' clock sources are controlled by the OSSRC1-0 (bits 17 - 16) in the Group Control Registers (GCR). The output clocks' / frame pulses' clock sources are controlled by the CKO3SRC1-0 (bits 22-21), CKO2SRC1-0 (bits 15-14), CKO1SRC1-0 (bits 8-7), and CKO0SRC1-0 (bits 1-0) in the Output Clock Control Register (OCCR). The clock sources can be set to either the internal system clock or one of the three input clock signals. These are used to provide a direct interface to jittery peripherals.

When the internal system clock is not used as the clock source, there are limitations to the data rate and the output clock rate. For all the input and output stream groups that do not use the internal system clock as their clock source, the data rate is limited to be no higher than the selected clock source's rate (e.g. if $\overline{\text{CKi1}}$ runs at 16.384 MHz and it is selected as the clock source for input stream group 3, then the maximum data rate of STiA3, STiB3, STiC3, and STiD3 is 16.384Mbps). Similarly, for all the output clocks that do not use the internal system clock as their clock source, the clock rate is limited to be no higher than the selected clock source's rate (e.g. if $\overline{\text{CKi1}}$ runs at 32.768 MHz and it is selected as the clock source for output clock $\overline{\text{CKo0}}$, then the maximum clock rate of $\overline{\text{CKo0}}$ is 32.768 MHz).

3.0 Output Clock ($\overline{\text{CKo}}$) and Output Frame Pulse ($\overline{\text{FPo}}$) Timing

There are four output timing pairs, $\overline{\text{CKo}}$3 - 0 and $\overline{\text{FPo}}$3 - 0. By default these signals generate ST-BUS, negative timing, and use the internal system clock as reference clock source. Their default clock rates are 65.536 MHz for $\overline{\text{CKo0}}$, 32.768 MHz for $\overline{\text{CKo1}}$, 16.384 MHz for $\overline{\text{CKo2}}$, and 8.192 MHz for $\overline{\text{CKo3}}$. Their properties can also be individually programmed in the Output Clock Control Register (OCCR) to control the frame pulse format (ST-BUS/GCI-Bus), frame pulse polarity, clock polarity, clock rate (8.192 MHz, 16.384 MHz, 32.768 MHz or 65.536 MHz), and reference clock source. Refer to Section 14.6 for programming details. Note that the reference clock source can be set to either the internal system clock or one of the three input clock signals. If one of the three input clock signals is selected as the reference source, the output clock cannot be programmed to generate a higher clock frequency than the reference source. As each output timing pair has its own bit settings, they can be set to provide different output timings. For 65.536 MHz output clock, the total loading on the output should not be larger than 10pF.

4.0 Output Channel Control

To be able to interface with external buffers, the output signals can be set to enter a high impedance or drive high state on a per-channel basis. The Per Channel Function (bits 31 - 29) in the Connection Memory Bits can be set to 001 to drive the channel output high, or to 000, 110 or 111 to set the channel into a high impedance state.

5.0 Data Input Delay and Data Output Advancement

The Group Control Registers (GCR) are used to adjust the input delay and output advancement for each input and output data groups. Each group is independently programmed.

5.1 Input Sampling Point Delay Programming

The input sampling point delay programming feature provides users with the flexibility of handling different wire delays when incoming traffic is from different sources.

By default, all input streams have zero delay, such that bit 7 is the first bit that appears after the input frame boundary (assuming ST-BUS formatting). The nominal input sampling point with zero delay is at the 3/4 bit time. The input delay is enabled by the Input Sample Point Delay (bit 8 - 4) in the Group Control Registers 0 - 31 (GCR0 - 31) as described in Section 14.4 on page 43. The input sampling point delay can range from 0 to 7 3/4 bit delay with a 1/4 bit resolution on a per group basis.

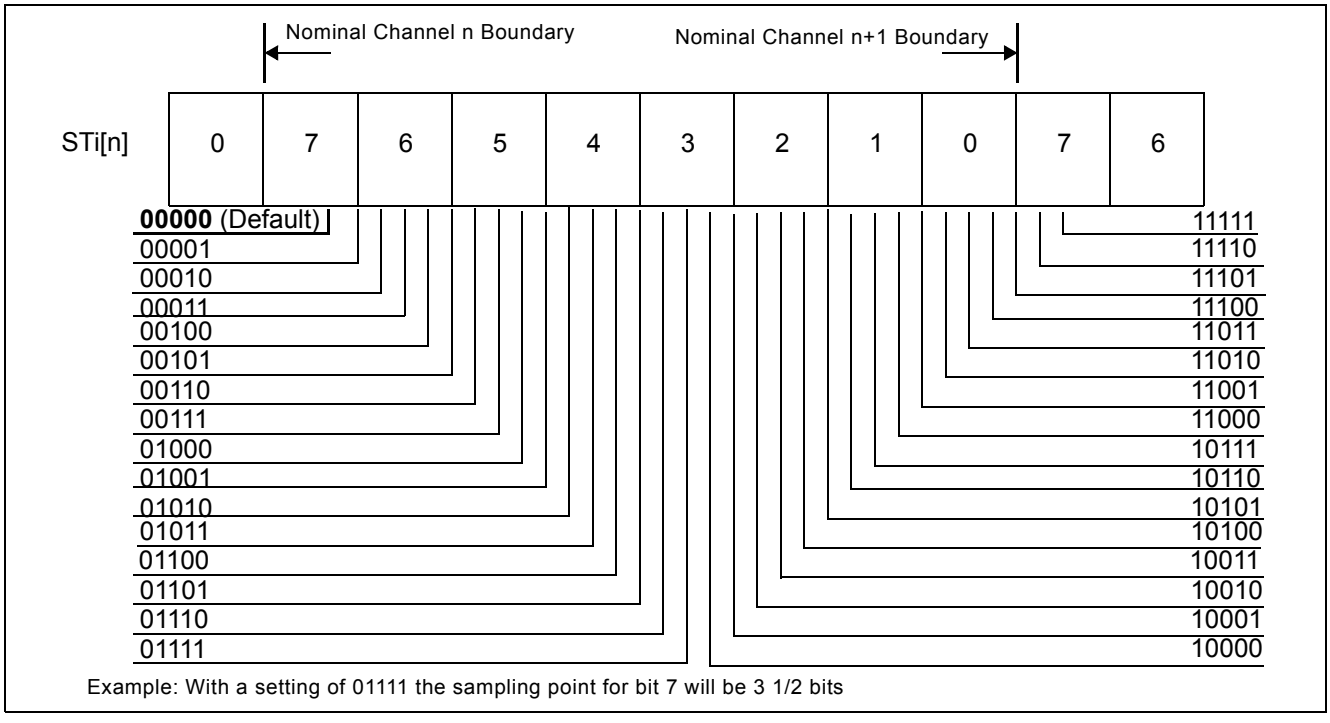

Figure 5 - Input Sampling Point Delay Programming

There are limitations when the ZL50073 is programmed to use $\overline{CKi}$2 - 0 as the input stream clock source as opposed to the internal clock:

- The granularity of the delay becomes 1/2 the selected reference clock period, or 1/4 bit, whichever is longer
- If the selected reference clock frequency is the same as the stream bit rate, the granularity of the delay is 1/2 bit. In this case, the least significant bit of the ISPD register is not used; the remaining 4 bits select the total delay in 1/2 bit increments, to a maximum of 7 1/2 bits. Also, the 0 bit delay reference point changes from the 3/4 bit position to the 1/2 bit position.

5.2 Fractional Bit Advancement on Output

See Section 14.4, Group Control Registers, for programming details.

This feature is used to advance the output data with respect to the output frame boundary. Each group has its own bit advancement value which can be programmed in the Group Control Registers 0 - 31 (GCR0 - 31).

By default all output streams have zero bit advancement such that bit 7 is the first bit that appears after the output frame boundary (assuming ST-BUS formatting). The output advancement is enabled by the Output Stream Bit Advancement (bits 21 - 20) of the Group Control Registers 0 - 31 (GCR0 - 31), as described in Section 14.4. The output delay can vary from 0 to 22.8 ns with a 7.6 ns increment. The exception to this is output streams programmed at 65 Mbps, in which case the increment is 3.8 ns with a total advancement of 11.4 ns.

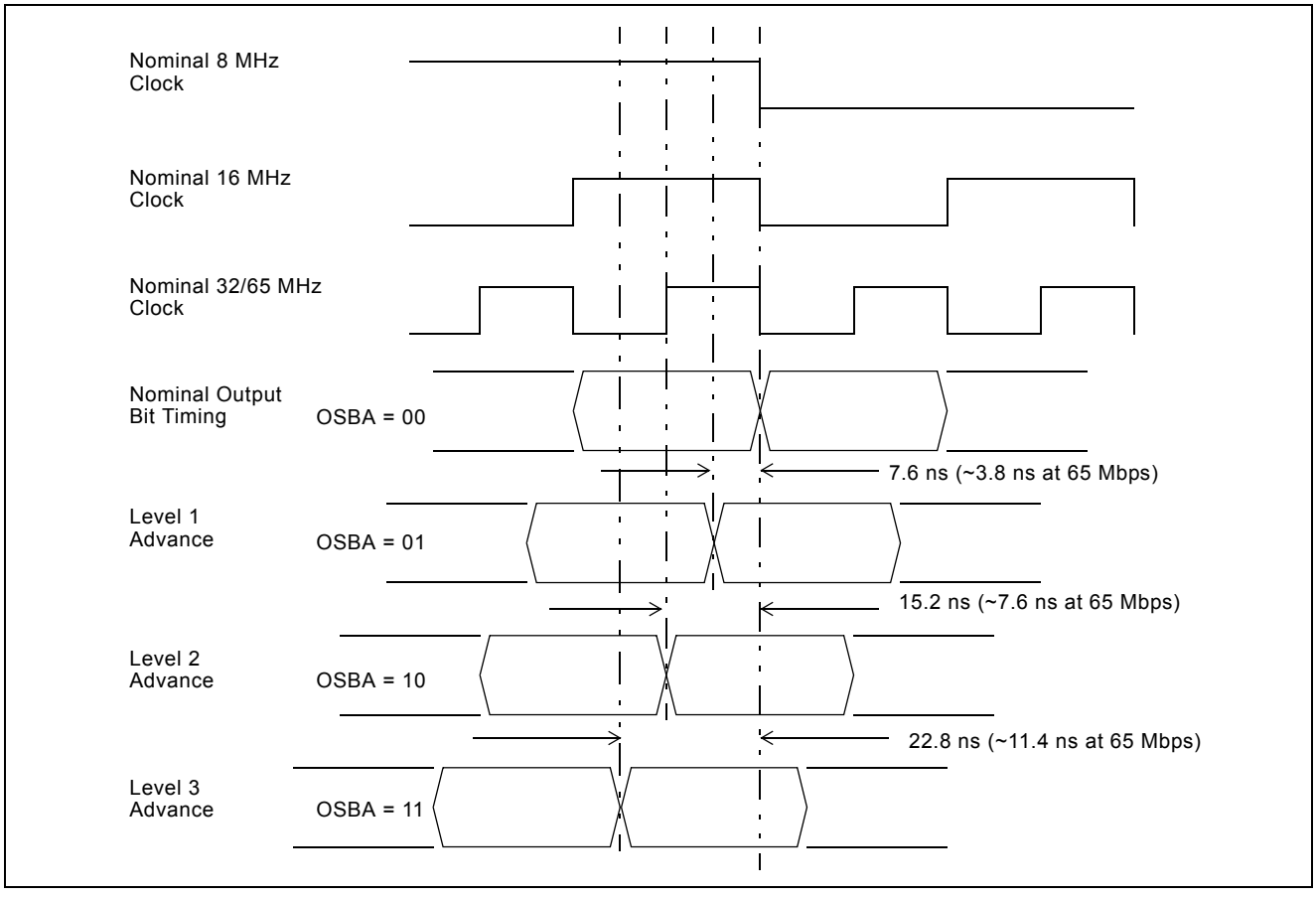

Figure 6 - Output Bit Advancement Timing

This programming feature is provided to assist in designs where per stream routing delays are significant and different.

The OSBA bits in the Group Control Registers are used to set the bit-advancement for each of the corresponding serial output stream groups. Figure 6 illustrates the effect of the OSBA settings on the output timing.

There are limitations when the ZL50073 is programmed to use $\overline{CKi}$2 - 0 as the output stream clock source:

- If the selected reference clock frequency is 65 MHz or 32 MHz, the granularity of the advancement is reduced to 1/2 the clock period
- If the selected reference clock frequency is 16 MHz or 8 MHz, bit advancement is not available and the output streams are driven at the nominal times

6.0 Message Mode

In Message Mode (MSG), microprocessor data can be broadcast to the output data streams on a per-channel basis. This feature is useful for transferring control and status information to external circuits or other TDM devices.

For a given output channel, when the corresponding Per Channel Function (bits 31 - 29) in the Connection Memory are set to Message Mode (010), the Connection Memory's lowest data byte (bits 7 - 0) is output in the timeslot. Refer to Section 14.1.1, Connection Memory Bit Functions, for programming details.

To increase programming bandwidth, the ZL50073 has separate addressable 32 bit memory locations, called Connection Memory Least Significant Bytes (LSB), which provide direct access to the Connection Memories'

Lowest data bytes (bits 7 - 0). Up to four consecutive message mode channels can be set with one Connection Memory LSB access. Refer to Section 14.1.2, Connection Memory LSB, for programming details.

6.1 Data Memory Read

All TDM input channels can be read via the microprocessor port. This feature is useful for receiving control and status information from external circuits or other TDM devices. Each 32 bit Data Memory access enables up to four consecutive input channels to be monitored. The Data Memory field is read only; any attempt to write to this address range will result in a bus error condition signalled back to the host processor. Refer to Section 14.2, Data Memory, for programming details.

The latency of data reads is up to 3 frames, depending on when the input timeslots are sampled.

6.2 Connection Memory Block Programming

See Section 14.7, Block Init Register, and Section 14.8, Block Init Enable Register, for programming details.

This feature allows for fast initialization of the connection memory after power up. When the block programming mode is enabled, the contents of Block Init Register are written to all Connection Memory Bits. This operation completes in one 125 μs frame. During Connection Memory initialization, all TDM output streams are set to high impedance.

7.0 Data Delay Through the Switching Paths

See Section 14.1.1, Connection Memory Bit Functions, for programming details.

The switching of information from the input serial streams to the output serial streams results in a throughput delay. The device can be programmed to perform timeslot interchange functions with different throughput delay capabilities on a per-channel basis. For voice applications, select variable throughput delay to ensure minimum delay between input and output data. In wideband data application, select constant delay to maintain the frame integrity of the information through the switch. The delay through the device varies according to the type of throughput delay selected by programming the Per Channel Function (bits 31 - 29) in the Connection Memories. When these bits are set to 011, the channel is in variable delay mode. When they are set to 100, the channel is in constant delay mode.

7.1 Constant Delay Mode

In this mode the frame integrity is maintained in all switching configurations. The delay though the switch is 2 frames - Input Channel + Output Channel. This can result in a minimum delay of 1 frame + 1 channel if the last channel of a stream is switched to the first channel of a stream. The maximum delay is 1 channel short of 3 frames delay. This occurs when the first channel of a stream is switched to the last channel of a stream.

The data throughput delay is expressed as a function of ST-BUS/GCI-Bus frames, input channel number (n) and output channel number (m). The data throughput delay (T) is:

T = 2 frames + (n - m)

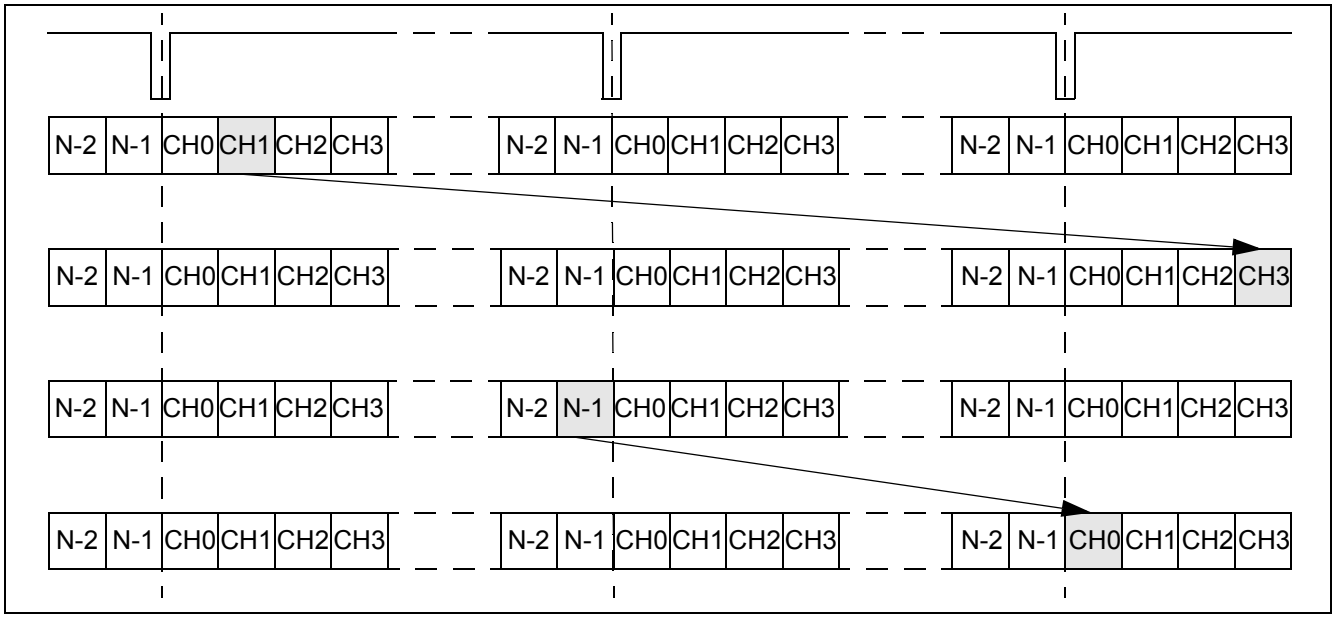

Figure 7 - Data Throughput Delay for Constant Delay

7.2 Variable Delay Mode

Variable delay mode causes the output channel to be transmitted as soon as possible. This is a useful mode for voice applications where the minimum throughput delay is more important than data integrity. The delay through the switch is minimum 3 channels and maximum 1 frame + 2 channels.

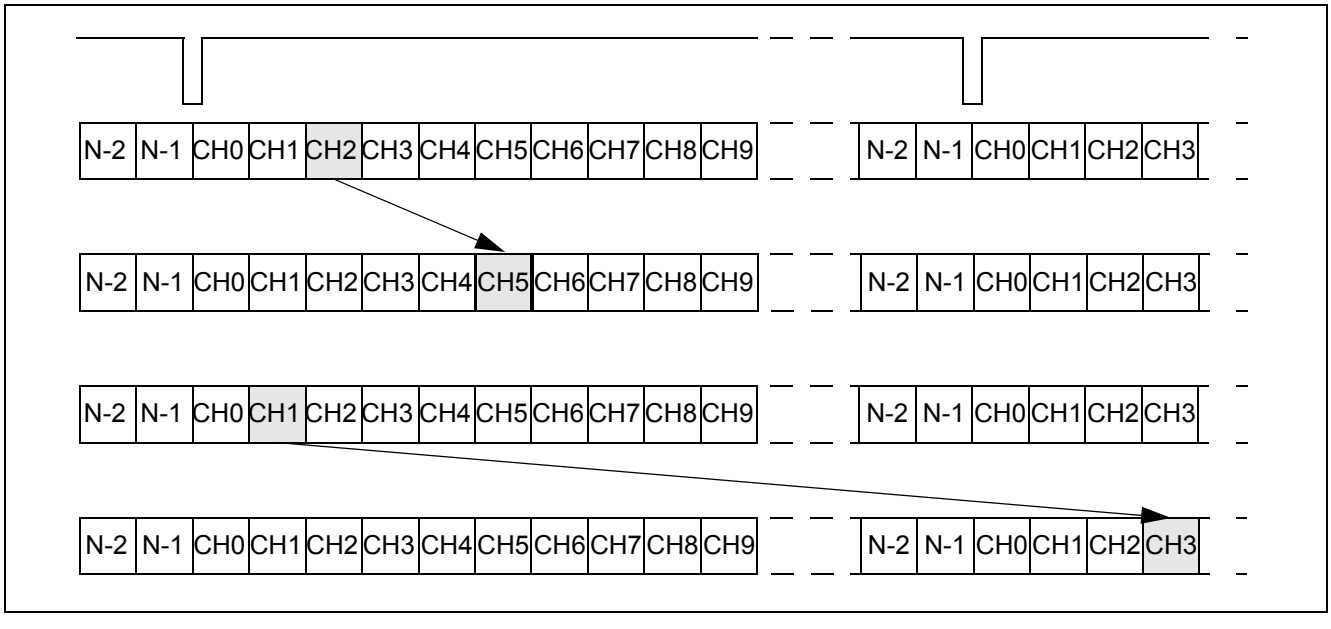

Figure 8 - Data Throughput Delay for Variable Delay

8.0 Per-Channel A-Law/μ-Law Translation

The ZL50073 provides per channel code translation to be used to adapt pulse code modulation (PCM) voice or data traffic between networks which use different encoding laws. Code translation is available in both Connection Modes and Message Mode.

This feature is controlled by the Connection Memories. The $\overline{V}$/D (bit 28) defines if the traffic in the channel is voice or data. The ICL1 - 0 (bits 27 - 26) define the input coding law and the OCL1 - 0 (bits 25 - 24) define the output coding law. The different coding options are shown in Table 4:

Input Coding (ICL1- 0)	Output Coding (OCL1 - 0)	Voice Coding ($\overline{V}$/D bit = 0)	Data Coding ($\overline{V}$/D bit = 1)
00	00	ITU-T G.711 A-Law	No Code
01	01	ITU-T G.711 μ-Law	Alternate Bit Inversion (ABI)
10	10	A-Law without Alternate Bit Inversion (ABI)	Inverted Alternate Bit Inversion (ABI)
11	11	μ-Law without Magnitude Inversion (MI)	All Bits Inverted

Table 4 - Input and Output Voice and Data Coding

For voice coding options, the ITU-T G.711 A-Law and ITU-T G.711 μ-Law are the standard rules for encoding. The A-Law without Alternate Bit Inversion (ABI) is an alternative code that does not invert the even bits (6, 4, 2, 0). The μ-Law without Magnitude Inversion (MI) is an alternative code that does not perform Inversion of magnitude bits (6, 5, 4, 3, 2, 1, 0).

When performing data code options, No Code does not invert the bits. The Alternate Bit Inversion (ABI) option inverts the even bits (6, 4, 2, 0) while the Inverted Alternate Bit Inversion (ABI) inverts the odd bits (7, 5, 3, 1). When All Bits Inverted is selected, all of the bits (7, 6, 5, 4, 3, 2, 1, 0) are inverted.

The input channel and output channel encoding law are configured independently. If the output channel coding is set to be different from the input channel, the ZL50073 performs translation between the two standards. If the input and output encoding laws are set to the same standard, no translation occurs.

9.0 Bit Error Rate Tester

The ZL50073 has one Bit Error Rate (BER) transmitter and one BER receiver for each pair of input and output streams, resulting in 128 transmitters connected to the output streams and 128 receivers associated with the input streams. Each transmitter can generate a BER sequence with a pattern of 2^{15}-1 Pseudo-Random Code (ITU O.151). Each transmitter can start at any location on the stream and will last for a minimum of 1 channel to a maximum of 1 frame time (125 μs). The BER transmitters are enabled by programming the Per Channel Function (bit 31 - 29) to 101 (PRBS Generator mode) in the Connection Memories.

Multiple Connection Memory locations can be programmed for BER tests. These locations are not required to be consecutive. However, when read back, the BER locations must be received in the same order that they were transmitted. If the BER locations are not received in the same order, the BER test will produce errors.

The PRBS bit pattern is sequentially loaded into the output timeslots. An example is shown in Figure 9.

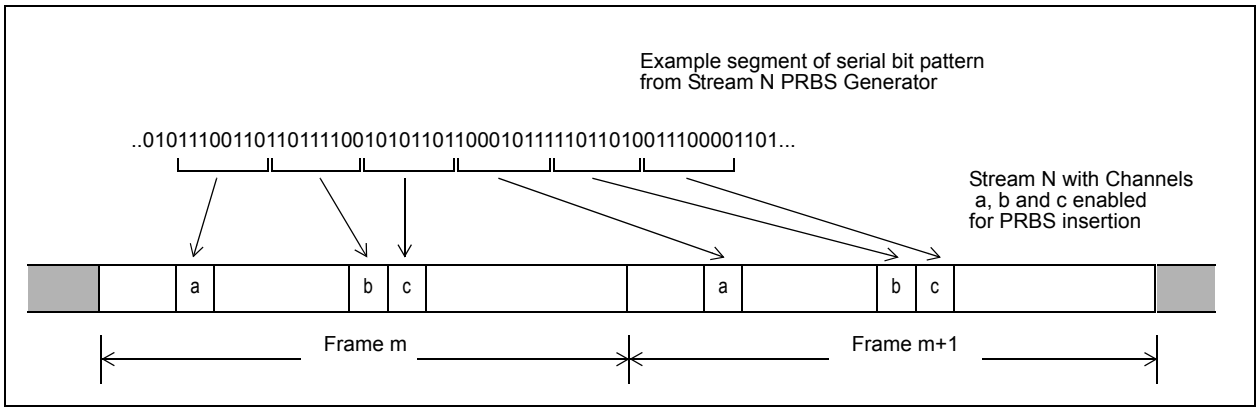

Figure 9 - Example PRBS Timeslot Insertion

Each PRBS detector can be configured to monitor for bit errors in one or more timeslots. The selection of timeslots is configured by the Input BER Enable Control Memory (IBERECM). See Section 14.3.1 for programming details. Each detector has an associated 16 bit error counter accessible via the microprocessor interface, as described in Section 14.3.2, BER Counters. The value of the counter represents the total number of errors detected on the corresponding input stream. Bit errors are accumulated until the counter is either reset (by writing to the counter or by resetting the device), or the counter reaches its maximum value, 65,535 (decimal). If more than 65,535 errors are detected, the counter will hold at the maximum value until reset.

Any number of timeslots may be configured for bit error rate testing; however the user must ensure the following for correct operation of the BER test function:

1. The number of timeslots enabled for PRBS detection on the input stream must equal the number of timeslots enabled for PRBS generation on the source output stream.
2. The arrival order of timeslots at the PRBS detector must be the same as the order in which timeslots were transmitted by the PRBS generator. For example, in Figure 9 above, the timeslot order a,b,c must be maintained through the external path from source TDM output stream to destination TDM input stream.

10.0 Microprocessor Port

The ZL50073 has a generic microprocessor port that provides access to the internal Data Memory (read access only), Connection Memory, and Control Registers.

The port size can be configured to be either 32 bit or 16 bit, controlled by the D16B pin.

The port works with either Motorola or Intel type microprocessor buses, selected by the IM pin.

10.1 Addressing

The Data Memory, Connection Memory and Control Registers are assigned 32 bit fields in the ZL50073 memory space. The Address Bus, A18 - 0, controls access to each 32 bit location. Byte addressing is also provided to give the user programming flexibility, if access to less than 32 bits is required.

Each 32 bit memory or register location spans 4 consecutive addresses. Example:

- The 32 bit Group Control Register for TDM Group 0 is located at address range 40200 - 40203 Hex

The Least Significant address identifies the Most Significant Byte (MSB) in the 32 bit field, as illustrated in Table 5.