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ZL50075

32 K Channel Digital Switch with High Jitter Tolerance, Rate Conversion per Group of 2 Streams (8, 16, 32 or 64 Mbps), and 64 Inputs and 64 Outputs

Data Sheet

Features

January 2006

- 32,768 channel x 32,768 channel non-blocking digital Time Division Multiplex (TDM) switch at 65.536 Mbps or 32.768 Mbps or using a combination of rates
- 16,384 channel x 16,384 channel non-blocking digital TDM switch at 16.384 Mbps
- 8,192 channel x 8,192 channel non-blocking digital TDM switch at 8.192 Mbps
- High jitter tolerance with multiple input clock sources and frequencies
- Up to 64 serial TDM input streams, divided into 32 groups with 2 input streams per group
- Up to 64 serial TDM output streams, divided into 32 groups with 2 output streams per group
- Per-group input and output data rate conversion selection at 65.536 Mbps, 32.768 Mbps, 16.384 Mbps and 8.192 Mbps. Input and output data group rates can differ
- Per-group input bit delay for flexible sampling point selection
- Per-group output fractional bit advancement
- Two sets of output timing signals for interfacing additional devices

Ordering Information

ZL50075GAC	324 Ball PBGA	Trays
ZL50075GAG2	324 Ball PBGA**	Trays

**Pb Free Tin/Silver/Copper

-40°C to +85°C

- Per-channel A-Law/μ-Law Translation
- Per-channel constant or variable throughput delay for frame integrity and low latency applications
- Per-stream Bit Error Rate (BER) test circuits
- Per-channel high impedance output control
- Per-channel force high output control
- Per-channel message mode
- Control interface compatible with Intel and Motorola 16 bit non-multiplexed buses
- Connection memory block programming
- Supports ST-BUS and GCI-Bus standards for input and output timing
- IEEE 1149.1 (JTAG) test port
- 3.3 V I/O with 5V tolerant inputs; 1.8 V core voltage

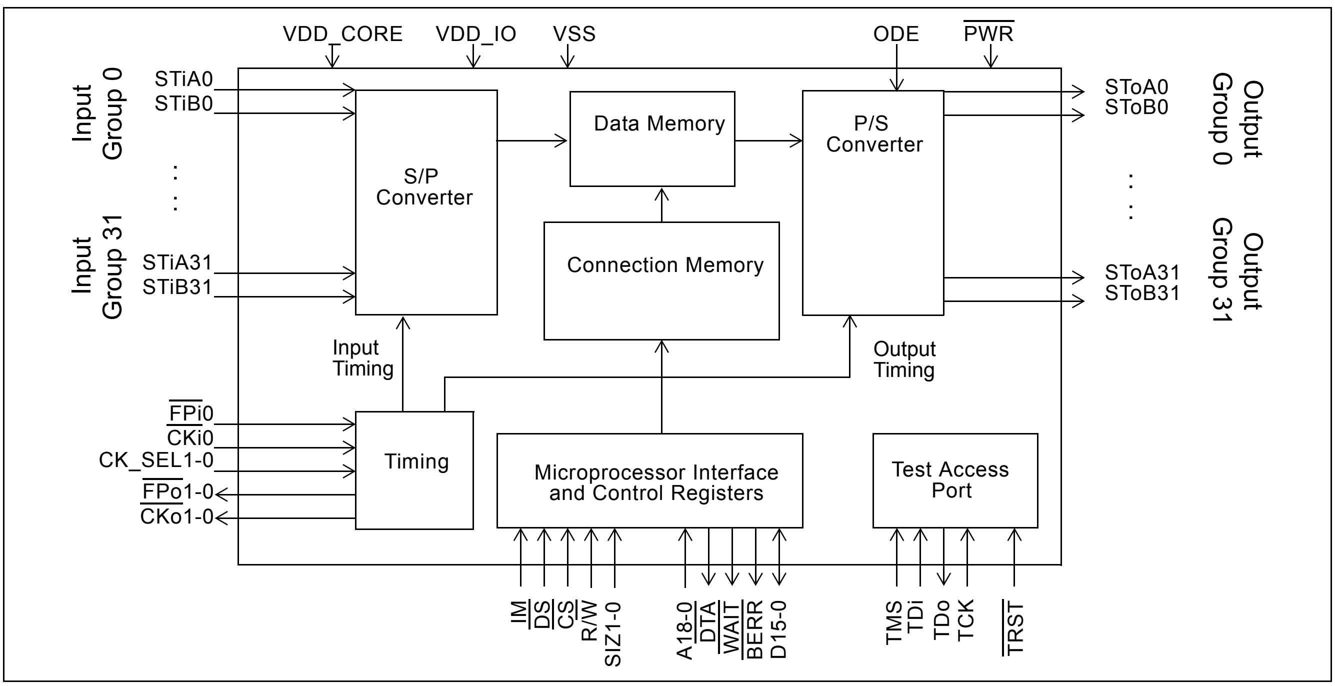

Figure 1 - ZL50075 Functional Block Diagram

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Applications

- Large Switching Platforms
- Central Office Switches
- Wireless Base Stations
- Multi-service Access Platforms
- Media Gateways

Description

The ZL50075 is a non-blocking Time Division Multiplex (TDM) switch with maximum 32,768 x 32,768 channels. The device can switch 64 kbps and Nx64 kbps TDM channels from any input stream to any output stream. With a number of enhanced features, the ZL50075 is designed for high capacity voice and data switching applications.

The ZL50075 has 64 input and 64 output data streams which can operate at 8.192 Mbps, 16.384 Mbps, 32.768 Mbps or 65.536 Mbps. The large number of inputs and outputs maintains full 32 K x 32 K channel switching capacity at bit rates of 65 Mbps and 32 Mbps. Up to 32 input and output data streams may operate at 65 Mbps. Up to 64 input and output data streams may operate at 32 Mbps, 16 Mbps or 8 Mbps. The data rate can be independently set in groups of 2 input or output streams. In this way it is possible to provide rate conversion from input data channel to output data channel.

The ZL50075 uses a master clock ($\overline{\text{CKi}}$0) and frame pulse ($\overline{\text{FPi}}$0) to define the TDM data stream frame boundary and timing. A high speed system clock is derived internally from $\overline{\text{CKi}}$0 and $\overline{\text{FPi}}$0. The input and output data streams can independently reference their timings to the input clock or to the internal system clock.

The ZL50075 has a variety of user configurable options designed to provide flexibility when data streams are connected to multiple TDM components or circuits. These include:

- Variable input bit delay and output advancement, to accommodate delays and frame offsets of streams connected through different data paths
- Two timing outputs, $\overline{\text{CKo}}$1 - 0 and $\overline{\text{FPo}}$1 - 0, which can be configured independently to provide a variety of clock and frame pulse options
- Support of both ST-BUS and GCI-Bus formats

The ZL50075 also has a number of value added features for voice and data applications:

- Per-channel variable delay mode for low latency applications and constant delay mode for frame integrity applications
- Per-channel A-Law/μ-Law Conversions for both voice and data
- 64 separate Pseudo-random Bit Sequence (PRBS) test circuits; one per stream. This provides an integrated Bit Error Rate (BER) test capability to facilitate data path integrity checking

The ZL50075 has two major modes of operation: Connection Mode (normal) and Message Mode. In Connection Mode, data bytes received at the TDM inputs are switched to timeslots in the output data streams, with mapping controlled by the Connection Memories. Using Zarlink's Message Mode capability, microprocessor data can be broadcast to the output data streams on a per-channel basis. This feature is useful for transferring control and status information to external circuits or other TDM devices.

A non-multiplexed microprocessor port provides access to the internal Data Memory, Connection Memory and Control Registers used to program ZL50075 options. The port is configurable to interface with either 16 bit Motorola or Intel-type microprocessors.

The mandatory requirements of IEEE 1149.1 standard are supported via the dedicated Test Access Port.

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Change Summary

The following table captures the changes from the April 2005 issue.

Page	Item	Change
25	10.1.1, “Read Cycle“	Clarified $\overline{\text{WAIT}}$ signal description in Read Cycle.
26	Figure 9 "Read Cycle Operation"	Corrected $\overline{\text{WAIT}}$ signal tristate timing in Read Cycle.
26	10.1.2, “Write Cycle“	Clarified $\overline{\text{WAIT}}$ signal description in Write Cycle.
27	Figure 10 "Write Cycle Operation"	Corrected $\overline{\text{WAIT}}$ signal tristate timing in Write Cycle.
38	Table 21 “BER Counter Group and Stream Address Mapping“	Corrected BER Counter Group and Stream Mapping Addresses.

The following table captures the changes from the July 2004 issue.

Page	Item	Change
10	"Pin Description" - CKo0-1	Added special requirement for using output clock at 65.536 MHz.
11	"Pin Description" - $\overline{\text{DTA}}$, $\overline{\text{WAIT}}$	Added more detailed description to the $\overline{\text{DTA}}$ and $\overline{\text{WAIT}}$ pins.
48	“AC Electrical Characteristics1 - FPi0 and CKi0 Timing“	Added t_{FPIS}, t_{FPIH} (input frame pulse setup and hold) maximum values.
50	(1) “AC Electrical Characteristics1 - FPO0-1 and CKO0-1 (65.536 MHz) Timing“ (2) “AC Electrical Characteristics1 - FPO0-1 and CKO0-1 (32.768 MHz) Timing“ (3) “AC Electrical Characteristics1 - FPO0-1 and CKO0-1 (16.384 MHz) Timing“ (4) “AC Electrical Characteristics1 - FPO0-1 and CKO0-1 (8.192 MHz) Timing“	Added $\overline{\text{CKO}}$0-1 and $\overline{\text{FPO}}$0-1 setup and hold parameters for all different clock rates.
51	“AC Electrical Characteristics - Output Clock Jitter Generation“	Added this table to specify $\overline{\text{CKO}}$0-1 jitter generation.
52	“AC Electrical Characteristics1 - Serial Data Timing2 to CKi“	(1) Values of parameters t_{SIPS}, t_{SIPH}, t_{SINS}, t_{SINH}, t_{SIPV}, t_{SINV}, t_{SIPZ} and t_{SINZ} are revised. (2) Separated parameter t_{CKD} into t_{CKDP} and t_{CKDN}.
53	Figure 14 "Serial Data Timing to CKi"	Added more detail to figure.
54	“AC Electrical Characteristics - Serial Data Timing1 to CKo2“	(1) Values of parameters t_{SOPS}, t_{SOPH}, t_{SONS}, t_{SONH}, t_{SOPV}, t_{SONV}, t_{SOPZ} and t_{SONZ} are revised. (2) Added CKO skew parameter, t_{CKOS}, (clock source to internal APLL).
55	Figure 15 "Serial Data Timing to CKo"	Added more detail and t_{CKOS} to figure.

Pin Diagram - ZL50075 19 mm x 19 mm 324 Ball PBGA (as viewed through top of package)

A1 corner identified by metallized marking.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
A	D[15]	D[14]	D[5]	D[4]	D[3]	A[18]	A[17]	A[13]	A[12]	A[11]	A[8]	A[4]	A[2]	A[0]	R/W	DS	IC	DTA
B	STOA [1]	IM	D[11]	D[10]	D[8]	D[7]	D[6]	D[1]	A[15]	A[10]	A[5]	A[1]	NC	CS	SIZ[0]	PWR	STOA [31]	SIZ[1]
C	STIA [2]	STIB [1]	STIA [0]	STIB [0]	STOA [0]	D[13]	D[9]	D[0]	A[14]	A[9]	A[6]	BERR	WAIT	STIB [31]	TDO	STIA [31]	TRST	NC
D	STOB [2]	CKO [0]	STIA [1]	STOB [0]	VDD_ CORE	D[12]	D[2]	VDD_ CORE	A[16]	VDD_ IO	A[7]	A[3]	VDD_ IO	TCK	VDD_ CORE	TMS	STOB [30]	STOB [31]
E	STIA [3]	STIB [2]	STOB [1]	FPO [0]	VSS	VSS	VDD_ CORE	VDD_ IO	VSS	VDD_ CORE	VDD_ IO	VSS	VDD_ CORE	VDD_ IO	TDI	STOA [30]	STIB [30]	STIA [30]
F	STOB [3]	STIB [3]	STOA [2]	VDD_ CORE	VDD_ IO	VSS	VSS	VDD_ CORE	VDD_ IO	VSS	VDD_ CORE	VDD_ IO	VSS	VDD_ CORE	STOB [29]	STIB [29]	STOA [29]	STIA [29]
G	STOA [3]	STIB [4]	STIA [4]	VDD_ IO	VDD_ CORE	VDD_ IO	VSS	VSS	VSS	VSS	VSS	VSS	VDD_ IO	VSS	VDD_ IO	STIB [28]	STOB [28]	STOA [28]
H	VSS	VSS	STOA [4]	STOB [4]	VSS	VDD_ CORE	VSS	VSS	VSS	VSS	VSS	VSS	VDD_ CORE	VDD_ IO	VSS	STOA [27]	STOB [27]	STIA [28]
J	STIA [5]	STOA [5]	STIB [5]	STOB [5]	VDD_ IO	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD_ CORE	STOA [26]	STOB [26]	VSS	STIB [27]
K	ODE	STIA [6]	STIA [7]	STOA [6]	VDD_ CORE	VDD_ IO	VSS	VSS	VSS	VSS	VSS	VSS	VDD_ IO	VSS	STIB [25]	IC	STOA [25]	STIA [27]
L	STIB [6]	STOB [6]	IC	STIA [8]	VSS	VDD_ CORE	VSS	VSS	VSS	VSS	VSS	VSS	VDD_ CORE	VDD_ IO	STIA [24]	STOA [24]	STOB [24]	IC
M	STIB [7]	STOA [7]	STOB [8]	VDD_ CORE	VDD_ IO	VDD_ IO	VSS	VSS	VSS	VSS	VSS	VSS	VDD_ IO	VDD_ CORE	VDD_ CORE	STIA [23]	STOB [23]	STIB [26]
N	STOB [7]	STIB [8]	STIB [9]	VDD_ IO	VDD_ CORE	VSS	VSS	VDD_ CORE	VDD_ IO	VSS	VDD_ CORE	VDD_ IO	VSS	VSS	VDD_ IO	STOA [22]	STOB [22]	STIA [26]
P	IC	STIA [9]	STIA [10]	STOB [10]	VSS	VSS	VDD_ CORE	VDD_ IO	VSS	VDD_ CORE	VSS	VSS	VDD_ CORE	VDD_ IO	STOA [21]	STOB [21]	NC	STOB [25]
R	STOA [8]	STOB [9]	STOA [10]	STIA [12]	VDD_ IO	STOA [13]	STIA [15]	VDD_ CORE	STOA [15]	VDD_ IO	STIB [17]	IC	VDD_ IO	STIB [19]	VDD_ CORE	STIA [21]	STIA [22]	STIA [25]
T	STOA [9]	STIB [10]	STIA [11]	STOA [11]	STOA [12]	STIA [13]	STOB [13]	STIB [15]	STOB [16]	FPI [0]	STIA [17]	IC	STIA [18]	STIA [19]	STIA [20]	STOA [20]	NC	STIB [24]
U	STIB [11]	STOB [11]	STIB [12]	CKO [1]	STIA [14]	STIB [14]	STOB [15]	STIA [16]	STOA [16]	IC	NC	STOB [17]	CK_ SEL[0	STOB [18]	STOB [19]	STOB [20]	STIB [21]	STOA [23]
V	STOB [12]	FPO [1]	STIB [13]	STOA [14]	STOB [14]	STIB [16]	CKI [0]	NC	IC	IC	STOA [17]	CK_ SEL[1]	STIB [18]	STOA [18]	STOA [19]	STIB [20]	STIB [22]	STIB [23]

Pin Description

Pin	Name	Description
		TDM Interface
C3, D3, C1, E1, G3, J1, K2, K3, L4, P2, P3, T3, R4, T6, U5, R7, U8, T11, T13, T14, T15, R16, R17, M16, L15, R18, N18, K18, H18, F18, E18, C16,	STiA0-31	**Serial TDM Input Data 'A' Streams (5 V Tolerant Input with Internal Pull-down)** The data rate of these input streams can be selected in a group of 2 to be either 8.192 Mbps, 16.384 Mbps, 32.678 Mbps or 65.536 Mbps. Refer to Section 1.4 for rate programming options. The data streams can be selected to be either inverted or non-inverted, programmed by the Group Control Registers (Section 14.4). Unused inputs are pulled low by internal pull-down resistors and may be left unconnected.
C4, C2, E2, F2, G2, J3, L1, M1, N2, N3, T2, U1, U3, V3, U6, T8, V6, R11, V13, R14, V16, U17, V17, V18, T18, K15, M18, J18, G16, F16, E17, C14	STiB0-31	**Serial TDM Input Data 'B' Streams (5 V Tolerant Input with Internal Pull-down)** The data rate of these input streams can be selected in a group of 2 to be either 8.192 Mbps, 16.384 Mbps, or 32.678 Mbps. The stream is unused when its input group rate is 65.536 Mbps. Refer to Section 1.4 for rate programming options. The data streams can be selected to be either inverted or non-inverted, programmed by the Group Control Registers (Section 14.4). Unused inputs are pulled low by internal pull-down resistors and may be left unconnected.
C5, B1, F3, G1, H3, J2, K4, M2, R1, T1, R3, T4, T5, R6, V4, R9, U9, V11, V14, V15, T16, P15, N16, U18, L16, K17, J15, H16, G18, F17, E16, B17	SToA0-31	**Serial TDM Output Data 'A' Streams (5 V Tolerant, 3.3 V Tri-state Slew-Rate Controlled Outputs)** The data rate of these output streams can be selected in a group of 2 to be either 8.192 Mbps, 16.384 Mbps, 32.678 Mbps or 65.536 Mbps. Refer to Section 1.4 for rate programming options. The data streams can be selected to be either inverted or non-inverted, programmed by the Group Control Registers (Section 14.4).
D4, E3, D1, F1, H4, J4, L2, N1, M3, R2, P4, U2, V1, T7, V5, U7, T9, U12, U14, U15, U16, P16, N17, M17, L17, P18, J16, H17, G17, F15, D17, D18	SToB0-31	**Serial TDM Output Data 'B' Streams (5 V Tolerant, 3.3 V Tri-state Slew-Rate Controlled Outputs)** The data rate of these output streams can be selected in a group of 2 to be either 8.192 Mbps, 16.384 Mbps or 32.678 Mbps. The stream is unused when its output group rate is 65.536 Mbps. Refer to Section 1.4 for rate programming options. The data streams can be selected to be either inverted or non-inverted, programmed by the Group Control Registers (Section 14.4). Unused outputs are tristated and may be left unconnected.
V7	$\overline{\text{CKi0}}$	**ST-BUS/GCI-Bus Clock Input (5 V Tolerant Schmitt-Triggered Input)** This pin accepts an 8.192 MHz, 16.384 MHz, 32.678 MHz or 65.536 MHz clock. This clock must be provided for correct operation of the ZL50075. The frequency of the $\overline{\text{CKi0}}$ input is selected by the CK_SEL1-0 inputs. The active clock edge may be either rising or falling, programmed by the Input Clock Control Register (Section 14.5).

Pin Description (continued)

Pin	Name	Description
T10	FPi0	**ST-BUS/GCI-Bus Frame Pulse Input (5 V Tolerant Input)** This pin accepts the 8 kHz frame pulse which marks the frame boundary of the TDM data streams. The pulse width is nominally one CKi0 clock period (assuming ST-BUS mode) selected by the CK_SEL1-0 inputs. The active state of the frame pulse may be either high or low, programmed by the Input Clock Control Register (Section 14.5).
D2, U4	CKo0-1	**ST-BUS/GCI-Bus Clock Outputs (3.3 V Outputs with Slew-Rate Control)** These clock outputs can be programmed to generate 8.192 MHz, 16.384 MHz, 32.678 MHz or 65.536 MHz TDM clock outputs. The active edge can be programmed to be either rising or falling. The source of the clock outputs can be derived from either the CKi0 inputs or the internal system clock. The frequency, active edge and source of each clock output can be programmed independently by the Output Clock Control Register (Section 14.6). For 65.536 MHz output clock, the total loading on the output should not be larger than 10pF.
E4, V2	FPo0-1	**ST-BUS/GCI-Bus Frame Pulse Outputs (3.3 V Outputs with Slew-Rate Control)** These 8 kHz output pulses mark the frame boundary of the TDM data streams. The pulse width is nominally one clock period of the corresponding CKo output. The active state of each frame pulse may be either high or low, independently programmed by the Output Clock Control Register (Section 14.6).
U13, V12	CK_SEL0-1	**TDM Master Clock Input Select** Inputs used to select the frequency and frame alignment of CKi0 and FPi0: CK_SEL1 = 0, CK_SEL0 = 0, 8.192 MHz CK_SEL1 = 0, CK_SEL0 = 1, 16.384 MHz CK_SEL1 = 1, CK_SEL0 = 0, 32.768 MHz CK_SEL1 = 1, CK_SEL0 = 1, 65.536 MHz
K1	ODE	**Output Drive Enable (5 V Tolerant Input with Internal Pull-up)** This is the asynchronous output enable control for the output streams. When it is high, the streams are enabled. When it is low, the output streams are tristated.
Microprocessor Port and Reset		
A1, A2, C6, D6, B3, B4, C7, B5, B6, B7, A3, A4, A5, D7, B8, C8	D15-0	**Microprocessor Port Data Bus (5 V Tolerant Bi-directional with Slew-Rate Output Control)** 16 bit bi-directional data bus. Used for microprocessor access to internal memories and registers.
A6, A7, D9, B9, C9, A8, A9, A10, B10, C10, A11, D11, C11, B11, A12, D12, A13, B12, A14	A18-0	**Microprocessor Port Address Bus (5 V Tolerant Inputs)** 19 bit address bus for the internal memories and registers. Note A0 is not used and should be connected to a defined logic level.

Pin Description (continued)

Pin	Name	Description
B14	$\overline{CS}$	**Chip Select Input (5 V Tolerant Input)** Active low input used with $\overline{DS}$ to enable read and write access to the ZL50075.
A16	$\overline{DS}$	**Data Strobe Input (5 V Tolerant Input)** Active low input used with $\overline{CS}$ to enable read and write access to the ZL50075.
A15	R/$\overline{W}$	**Read/Write Input (5 V Tolerant Input)** Input signal that controls the type of microprocessor access: 0 - Microprocessor write to the ZL50075 1 - Microprocessor read from the ZL50075
A18	$\overline{DTA}$	**Data Transfer Acknowledge (5 V Tolerant, 3.3 V Tri-state Output with Slew-Rate)** Active low output which indicates that a data bus transfer is complete. An external pull-up resistor is required to hold this pin HIGH when output is high-impedance.
C12	$\overline{BERR}$	**Transfer Bus Error Output with Slew Rate Control (5 V Tolerant, 3.3 V Tri-state Outputs with Slew-Rate Control)** This pin goes low whenever the microprocessor attempts to access an invalid memory space inside the device. In Motorola bus mode, if this bus error signal is activated, the data transfer acknowledge signal, $\overline{DTA}$, will not be generated. In Intel bus mode, the generation of the $\overline{DTA}$ is not affected by this $\overline{BERR}$ signal. An external pull-up resistor is required to hold a HIGH level when output is high-impedance.
C13	$\overline{WAIT}$	**Data Transfer Wait Output (5 V Tolerant, 3.3 V Tri-state Output with Slew Rate)** Active low wait signal output. An external pull-up resistor is required to hold a HIGH level when output is high-impedance.
B15, B18	SIZ0-1	**Data Transfer Size/Upper and Lower Data Strobe Inputs (5 V Tolerant Inputs)** Motorola mode: SIZ0 - $\overline{LDS}$, SIZ1 - $\overline{UDS}$. Active low upper and lower data strobes, $\overline{UDS}$ and $\overline{LDS}$, indicate whether the upper byte, D15-8, and/or lower byte, D7-0, is being transferred. Intel mode: SIZ0 - $\overline{BE0}$, SIZ1 - $\overline{BE1}$. Active low Intel type bus-enable signal $\overline{BE1}$ and $\overline{BE0}$ signals
B2	IM	**Microprocessor Port Bus Mode Select (5 V Tolerant Input)** Control input: 0 = Motorola mode 1 = Intel mode
B16	$\overline{PWR}$	**Device Reset (5 V Tolerant Schmitt-Triggered Input)** Asynchronous reset input used to initialize the ZL50075. 0 = Reset 1 = Normal See Section 11.0, Power-up and Initialization of the ZL50075 for detailed description of Reset state.

Pin Description (continued)

Pin	Name	Description
IEEE 1149.1 (JTAG) Test Access Port (TAP)		
E15	TDI	**Test Data (5 V Tolerant Input with Internal Pull-up)** Serial test data input. When not used, this input may be left unconnected.
C15	TDO	**Test Data (3.3 V Output)** Serial test data output.
D14	TCK	**Test Clock (5 V Tolerant Schmitt-Triggered Input with Internal Pull-up)** Clock input used by TAP Controller. When not used, this input may be left unconnected.
D16	TMS	**Test Reset (5 V Tolerant Schmitt-Triggered Input with Internal Pull-up)** Input which controls the state transitions of the TAP Controller. When not used, this pin is pulled high by an internal pull-up resistor and may be left unconnected.
C17	$\overline{\text{TRST}}$	**Test Mode Select (5 V Tolerant Input with Internal Pull-up)** Asynchronously initializes the JTAG TAP controller by putting it in the Test-Logic-Reset state. This pin should be pulsed low during power-up to ensure that the device is in the normal functional mode. When JTAG is not being used, this pin should be pulled low during normal operation.
Unused		
U10, V9, V10, R12, L18, A17, L3, P1, T12, K16	IC	**Internal Connections** In normal mode these pins **MUST** be connected low.
B13, C18, P17, T17, U11, V8	NC	**No Connection** In normal mode these pins **MUST** be left unconnected.
Power		
E5, E6, E9, E12, F6, F7, F10, F13, G7, G8, G9, G10, G11, G12, G14, H1, H2, H5, H7, H8, H9, H10, H11, H12, H15, J6, J7, J8, J9, J10, J11, J12, J13, J17, K7, K8, K9, K10, K11, K12, K14, L5, L7, L8, L9, L10, L11, L12, M7, M8, M9, M10, M11, M12, N6, N7, N10, N13, N14, P5, P6, P9, P11, P12	V_{SS}	**Ground**
D5, D8, D15, E7, E10, E13, F4, F8, F11, F14, G5, H6, H13, J14, K5, L13, L6, M4, M14, M15, N5, N8, N11, P7, P10, P13, R8, R15	V_{DD_CORE}	**Power Supply for the Core Logic:** +1.8 V

Pin Description (continued)

Pin	Name	Description
D10, D13, E8, E11, E14, F5, F9, F12, G4, G6, G13, G15, H14, J5, K6, K13, L14, M5, M6, M13, N4, N9, N12, N15, P8, P14, R5, R10, R13	V_{DD_IO}	**Power Supply for the I/O:** +3.3 V

1.0 Functional Description

1.1 Overview

The device has 64 ST-BUS/GCI-Bus inputs (STiA0 - 31 and STiB0 - 31) and 64 ST-BUS/GCI-Bus outputs (SToA0 - 31 and SToB0 - 31). It is a non-blocking digital switch with 32,768 64 kbps channels and is capable of performing rate conversion between groups of 2 inputs and 2 outputs. The inputs accept serial input data streams with data rates of 8.192 Mbps, 16.384 Mbps, 32.768 Mbps or 65.536 Mbps. There are 32 input groups with each group consisting of 2 streams (‘A’ and ‘B’). Each group can be set to any of the data rates. The outputs deliver serial data streams with data rates of 8.192 Mbps, 16.384 Mbps, 32.768 Mbps or 65.536 Mbps. There are 32 output groups with each group consisting of 2 streams (‘A’ and ‘B’). Each group can be set to any of the data rates.

By using Zarlink’s message mode capability, the microprocessor can store data in the connection memory which can be broadcast to the output streams on a per-channel basis. This feature is useful for transferring control and status information for external circuits or other ST-BUS/GCI-Bus devices.

The ZL50075 uses the ST-BUS/GCI-Bus master input frame pulse ($\overline{\text{FPi}}$0) and the ST-BUS/GCI-Bus master input clock (CKi0) to define the input frame boundary and timing for sampling the ST-BUS/GCI-Bus input streams with various data rates (8.192 Mbps, 16.384 Mbps, 32.768 Mbps or 65.536 Mbps). The rate of the input clock is defined by setting the CK_SEL1 - 0 pins.

A selectable Motorola or Intel compatible non-multiplexed microprocessor port allows users to program the device to operate in various modes under different switching configurations. Users can use the microprocessor port to perform internal register and memory read and write operations. The microprocessor port has 16 bit data bus and 17 bit address bus (in A18-0, A0 is not used, and A1 is used for word alignment). There are seven control signals ($\overline{\text{CS}}$, $\overline{\text{DS}}$, R/$\overline{\text{W}}$, $\overline{\text{DTA}}$, $\overline{\text{WAIT}}$, $\overline{\text{BERR}}$ and IM).

The device supports the mandatory requirements for the IEEE 1149.1 (JTAG) standard via the test port.

1.2 Switch Operation

The ZL50075 switches 64 kbps and Nx64 kbps data and voice channels from the TDM input streams, to timeslots in the TDM output streams. The device is non-blocking; all 32 K input channels can be switched through to the outputs. Any input channel can be switched to any available output channel.

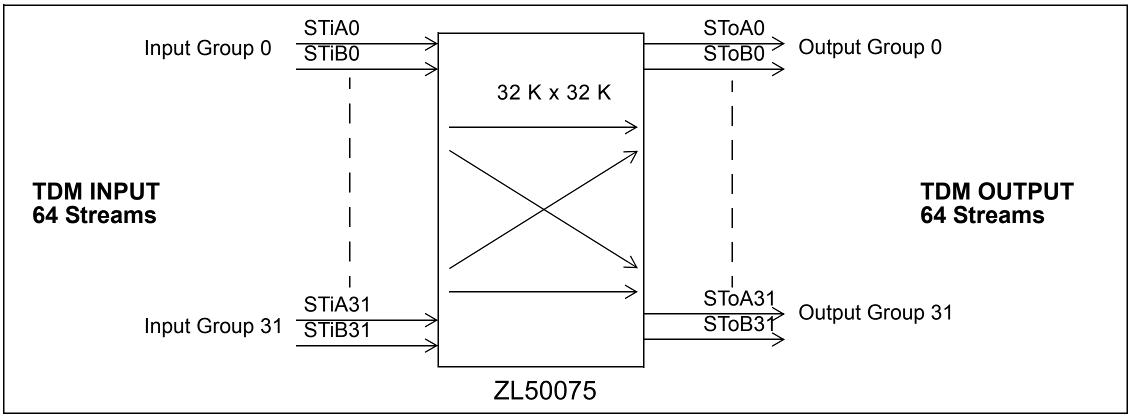

Figure 2 - 32 K x 32 K Channel Basic Switch Configuration

The maximum channel switching capacity is determined by the number of streams and their rate of operation, as shown in Table 1.

TDM Group Data Rate	Maximum Number of Input TDM Data Streams	Maximum Number of Output TDM Data Streams	Number of 64 kbps Channels per Stream	Maximum Switch Capacity† (streams x channels = total)
65.536 Mbps	32	32	1024	32 x 1024 = 32,768
32.768 Mbps	64	64	512	64 x 512 = 32,768
16.384 Mbps	64	64	256	64 x 256 = 16,384‡
8.192 Mbps	64	64	128	64 x 128 = 8,192‡

Table 1 - Data Rate and Maximum Switch Size

† The maximum capacity shown is when all streams are at the same rate, and none are operating at 16.384 Mbps or 8.192 Mbps.

‡ Switch capacity is limited to less than 32 K channels, only when streams are provisioned at 16 Mbps or 8 Mbps. The maximum switch capacity in this case is given by 32,768 - (M x 256) - (N x 384), where M is the number of 16 Mbps input or output streams, and N is the number of 8 Mbps input or output streams.

1.3 Stream Provisioning

The ZL50075 is a large switch with a comprehensive list of user configurable, 'per-group' programmable features. In order to facilitate ease of use, the ZL50075 offers a simple programming model. Streams are grouped in sets of two, with each group sharing the same configured characteristics. In this way it is possible to reduce programming complexity, while still maintaining flexible 'per-stream' configuration options:

- Input and output rate selection, see Section 1.4
- Input stream clock source selection, see Section 2.0
- Output stream clock source selection, see Section 2.0
- Input stream sampling point selection, see Section 5.1
- Output stream fractional bit advance, see Section 5.2
- Input and output stream inversion control, see Section 14.4

The streams are grouped, one from the TDM 'A' streams, combined with the corresponding 'B' streams. For example, input stream group #12 is STiA12 and STiB12, and output stream group #4 is SToA4 and SToB4. There are 32 input and 32 output groups. Depending on the data rate set for the group there will be between 1 and 2 streams activated. If the data rate is set for 65.536 Mbps, the 'A' stream will be activated and the 'B' stream will not be activated. If the data rate is set for 32.768 Mbps, 16.384 Mbps or 8.192 Mbps, the 'A' and 'B' streams will be activated. The maximum channel capacity of a group is 1024 channels when operating at 65 Mbps or 32 Mbps. The switch capacity is reduced to 512 channels when operating at 16 Mbps and to 256 channels when operating at 8 Mbps.

1.4 Input and Output Rate Selection

Table 1 shows the maximum number of streams available at different bit rates. The ZL50075 deactivates unused streams when operating at the higher bit rates as shown in Table 2.

Input or Output Group n (n = 0 - 31)	65 Mbps	32 Mbps	16 Mbps	8 Mbps
STiAn / SToAn	Active	Active	Active	Active
STiBn / SToBn	Not Active	Active	Active	Active

Table 2 - TDM Stream Bit Rates

For 65 Mbps operation, only those inputs and outputs in the TDM ’A’ streams are active. For 32 Mbps, 16 Mbps and 8 Mbps operation, the inputs and outputs in the TDM ’A’ and ’B’ streams are active.

Note that if the internal system clock is not used as the clock source, there are limitations on the maximum data rate. See Section 2.0 for more details.

1.4.1 Per Group Rate Selection

See Section 14.4, Group Control Registers, for programming details. The data rates are set with the Input Stream Bit Rate (bits 3 - 2) and the Output Stream Bit Rate (bits 19 - 18) in the Group Control Registers 0 - 31 (GCR0 - 31).

For the ZL50075, the bit rates of the inputs and outputs are programmed independently, in groups of 2 streams. Depending on the rate programmed, the active streams in the group will be as indicated in Table 2.

For example:

- if input stream group #1 is programmed for 65 Mbps: STiA1 is active; STiB1 is not active
- if output stream group #15 is programmed for 32 Mbps, 16 Mbps or 8 Mbps: SToA15 and SToB15 are active

1.5 Rate Conversion

The ZL50075 supports rate conversion from any input stream rate to any output stream rate.

An example of ZL50075 rate conversion is given in Figure 3. The output stream rates do not have to follow the input stream rates. In this example, on the input side of the switch you can have 24 streams operating at 65.536 Mbps (24,576 channels - 24 groups with 1 stream in each group), 8 streams operating at 32.768 Mbps (4096 channels - 4 groups with 2 streams in each group) and 8 streams operating at 16.384 Mbps (2048 channels - 4 groups with 2 streams in each group) with no streams operating at 8.192 Mbps. This results in an input capacity of 30,720 input channels. This is less than the full capacity of the device as some groups are operating at less than 32 Mbps. As the output streams do not have to follow the input streams, they can be configured so that 15 streams operate at 65.536 Mbps (15,360 channels - 15 groups with 1 stream in each group), 28 streams operate at 32.768 Mbps (14,336 channels - 14 groups with 2 streams in each group), 2 streams operate at 16.384 Mbps (512 channels - 1 group with 2 streams in the group) and 4 streams operate at 8.192 Mbps (512 channels - 2 groups with 2 streams in each group). This results in an output capacity of 30,720 output channels. This is less than the full capacity of the device as some groups are operating at less than 32 Mbps.

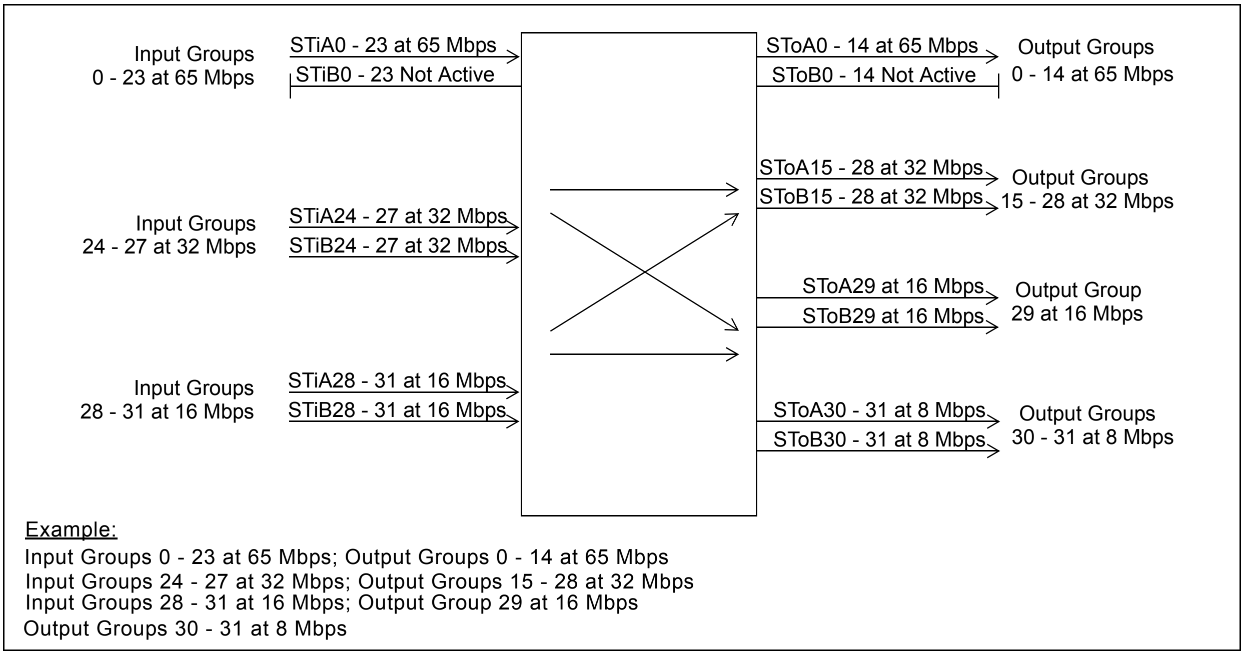

Figure 3 - Input and Output Data Rate Conversion Example

2.0 Input Clock ($\overline{\text{CKi}}$) and Input Frame Pulse ($\overline{\text{FPi}}$) Timing

The input timing for the ZL50075 can be set for one of four different frequencies. They can also be set for ST-BUS or GCI-Bus mode with positive or negative input. The $\overline{\text{CKi0}}$ and $\overline{\text{FPi0}}$ input timing must be provided in order for the device to be used. $\overline{\text{CKi0}}$ is used to generate the internal clock. This clock is used for all the internal logic and can be used as one of the clocks that defines the timing for the input and output data. The input stream clock source is selected by the ISSRC1 - 0 (bits 1 - 0) in the Group Control Register. The output stream clock source is selected by the OSSRC1 - 0 (bits 17 - 16) in the Group Control Register.

The $\overline{\text{CKi0}}$ and $\overline{\text{FPi0}}$ input frequency is set via the CK_SEL1 - 0 pins as shown in Table 3. By default the $\overline{\text{CKi0}}$ and $\overline{\text{FPi0}}$ pins accept ST-BUS, negative input timing. The input frame pulse format (ST-BUS/GCI-Bus), frame pulse polarity, and clock polarity can be programmed by the GCISEL0 (bit 2), FPIPOL0 (bit 1), and CKIPSL0 (bit 0) in the Input Clock Control Register (ICCR), as described in Section 14.5.

CK_SEL1	CK_SEL0	Input $\overline{\text{CKi0}}$ and $\overline{\text{FPi0}}$
0	0	8.192 MHz
0	1	16.384 MHz
1	0	32.768 MHz
1	1	65.536 MHz

Table 3 - $\overline{\text{CKi0}}$ and $\overline{\text{FPi0}}$ Setting via CK_SEL1 - 0

The input streams, output streams, and output clocks / frame pulses can use either the internal system clock or the input $\overline{\text{CKi0}}$ and $\overline{\text{FPi0}}$ as clock sources. The input streams' clock sources are controlled by the ISSRC1-0 (bits 1 - 0) in the Group Control Registers (GCR). The output streams' clock sources are controlled by the OSSRC1-0 (bits 17 - 16) in the Group Control Registers (GCR). The output clocks' / frame pulses' clock sources are controlled by the CKO1SRC1-0 (bits 8-7) and CKO0SRC1-0 (bits 1-0) in the Output Clock Control Register (OCCR). Using the input $\overline{\text{CKi0}}$ and $\overline{\text{FPi0}}$ as clock source provides a direct interface to jittery peripherals, while using the internal system clock as clock source provides the best data rate and clock rate flexibility.

When the internal system clock is not used as the clock source, there are limitations to the data rate and the output clock rate. For all the input and output stream groups that do not use the internal system clock as their clock source, the data rate is limited to be no higher than the selected clock source's rate (e.g., if CKi0 runs at 16.384 MHz and it is selected as the clock source for input stream group 3, then the maximum data rate of STiA3 and STiB3 is 16.384 Mbps). Similarly, for all the output clocks that do not use the internal system clock as their clock source, the clock rate is limited to be no higher than the selected clock source's rate (e.g., if CKi0 runs at 32.768 MHz and it is selected as the clock source for output clock CKo0, then the maximum clock rate of CKo0 is 32.768 MHz).

3.0 Output Clock (CKo) and Output Frame Pulse (FPo) Timing

There are two output timing pairs, CKo1 - 0 and FPo1 - 0. By default these signals generate ST-BUS, negative timing, and use the internal system clock as reference clock source. Their default clock rates are 65.536 MHz for CKo0 and 32.768 MHz for CKo1. Their properties can also be individually programmed in the Output Clock Control Register (OCCR) to control the frame pulse format (ST-BUS/GCI-Bus), frame pulse polarity, clock polarity, clock rate (8.192 MHz, 16.384 MHz, 32.768 MHz or 65.536 MHz), and reference clock source. Refer to Section 14.6 for programming details. Note that the reference clock source can be set to either the internal system clock or the input CKi0 and FPi0 signals. If the input CKi0 and FPi0 is selected as the reference source, the output clock cannot be programmed to generate a higher clock frequency than the reference source. As each output timing pair has its own bit settings, they can be set to provide different output timings. For 65.536 MHz output clock, the total loading on the output should not be larger than 10pF.

4.0 Output Channel Control

To be able to interface with external buffers, the output signals can be set to enter a high impedance or drive high state on a per-channel basis. The Per Channel Function (bits 31 - 29) in the Connection Memory Bits can be set to 001 to drive the channel output high, or to 000, 110 or 111 to set the channel into a high impedance state.

5.0 Data Input Delay and Data Output Advancement

The Group Control Registers (GCR) are used to adjust the input delay and output advancement for each input and output data groups. Each group is independently programmed.

5.1 Input Sampling Point Delay Programming

The input sampling point delay programming feature provides users with the flexibility of handling different wire delays when incoming traffic is from different sources.

By default, all input streams have zero delay, such that bit 7 is the first bit that appears after the input frame boundary (assuming ST-BUS formatting). The nominal input sampling point with zero delay is at the 3/4 bit time. The input delay is enabled by the Input Sample Point Delay (bit 8 - 4) in the Group Control Registers 0 - 31 (GCR0 - 31) as described in Section 14.4 on page 39. The input sampling point delay can range from 0 to 7 3/4 bit delay with a 1/4 bit resolution on a per group basis.

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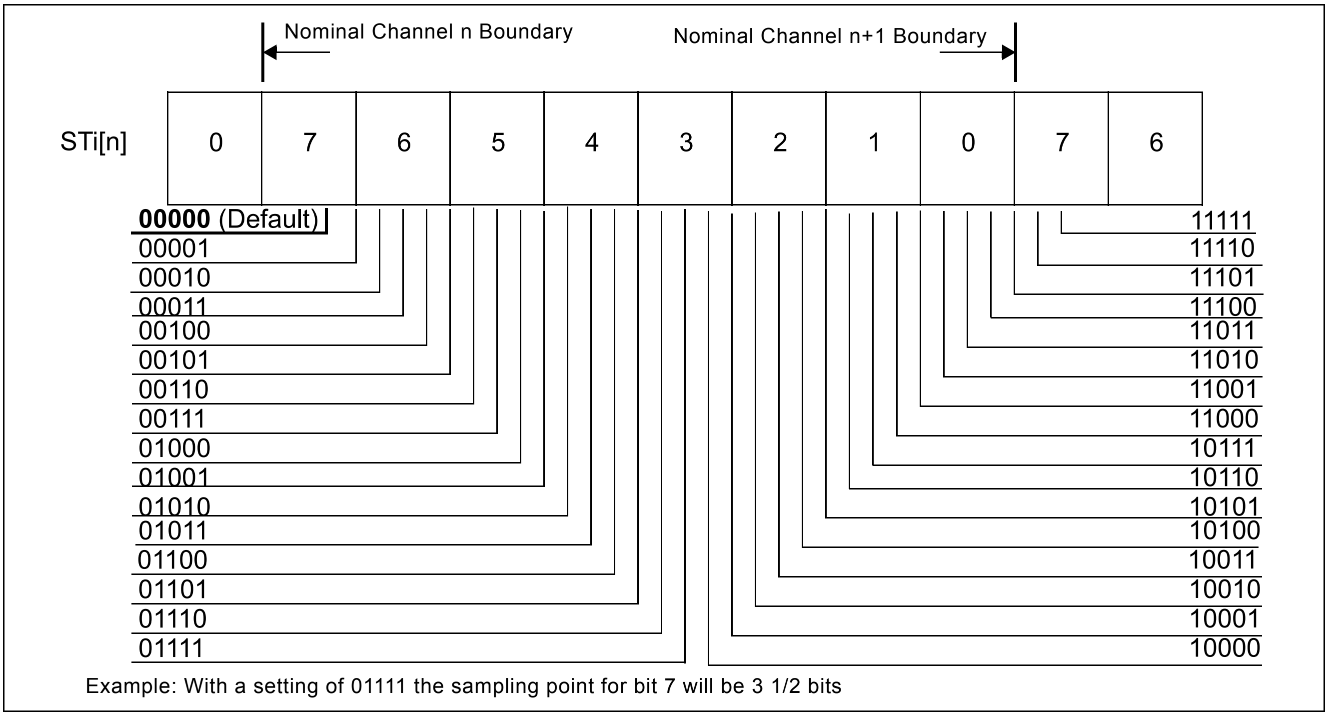

Figure 4 - Input Sampling Point Delay Programming

There are limitations when the ZL50075 is programmed to use $\overline{\text{CKi0}}$ as the input stream clock source as opposed to the internal clock:

- The granularity of the delay becomes 1/2 the selected reference clock period, or 1/4 bit, whichever is longer
- If the selected reference clock frequency is the same as the stream bit rate, the granularity of the delay is 1/2 bit. In this case, the least significant bit of the ISPD register is not used; the remaining 4 bits select the total delay in 1/2 bit increments, to a maximum of 7 1/2 bits. Also, the 0 bit delay reference point changes from the 3/4 bit position to the 1/2 bit position.

5.2 Fractional Bit Advancement on Output

See Section 14.4, Group Control Registers, for programming details.

This feature is used to advance the output data with respect to the output frame boundary. Each group has its own bit advancement value which can be programmed in the Group Control Registers 0 - 31 (GCR0 - 31).

By default all output streams have zero bit advancement such that bit 7 is the first bit that appears after the output frame boundary (assuming ST-BUS formatting). The output advancement is enabled by the Output Stream Bit Advancement (bits 21 - 20) of the Group Control Registers 0 - 31 (GCR0 - 31), as described in Section 14.4. The output delay can vary from 0 to 22.8 ns with a 7.6 ns increment. The exception to this is output streams programmed at 65 Mbps, in which case the increment is 3.8 ns with a total advancement of 11.4 ns.

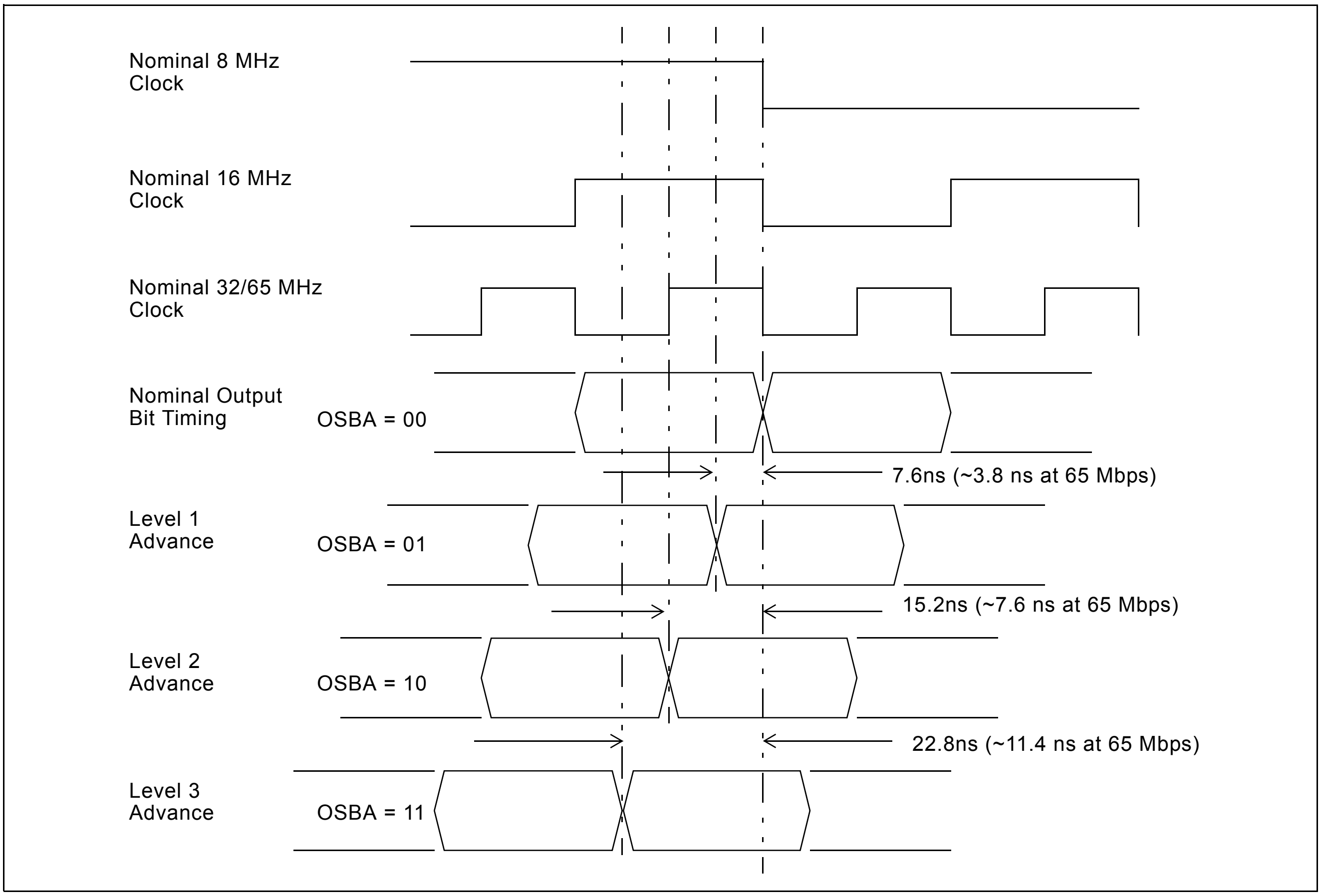

Figure 5 - Output Bit Advancement Timing

This programming feature is provided to assist in designs where per stream routing delays are significant and different.

The OSBA bits in the Group Control Registers are used to set the bit-advancement for each of the corresponding serial output stream groups. Figure 5 illustrates the effect of the OSBA settings on the output timing.

There are limitations when the ZL50075 is programmed to use $\overline{\text{CKi}}$0 as the output stream clock source:

- If the selected reference clock frequency is 65 MHz or 32 MHz, the granularity of the advancement is reduced to 1/2 the clock period
- If the selected reference clock frequency is 16 MHz or 8 MHz, bit advancement is not available and the output streams are driven at the nominal times

6.0 Message Mode

In Message Mode (MSG), microprocessor data can be broadcast to the output data streams on a per-channel basis. This feature is useful for transferring control and status information to external circuits or other TDM devices.

For a given output channel, when the corresponding Per Channel Function (bits 31 - 29) in the Connection Memory are set to Message Mode (010), the Connection Memory's lowest data byte (bits 7 - 0) is output in the timeslot. Refer to Section 14.1.1, Connection Memory Bit Functions, for programming details

To increase programming bandwidth, the ZL50075 has separate addressable 32 bit memory locations, called Connection Memory Least Significant Bytes (LSB), which provide direct access to the Connection Memories' Lowest data bytes (bits 7 - 0). Up to four consecutive message mode channels can be set with one Connection Memory LSB access. Refer to Section 14.1.2, Connection Memory LSB, for programming details.

6.1 Data Memory Read

All TDM input channels can be read via the microprocessor port. This feature is useful for receiving control and status information from external circuits or other TDM devices. Each 32 bit Data Memory access enables up to four consecutive input channels to be monitored. The Data Memory field is read only; any attempt to write to this address range will result in a bus error condition signalled back to the host processor. Refer to Section 14.2, Data Memory, for programming details.

The latency of data reads is up to 3 frames, depending on when the input timeslots are sampled.

6.2 Connection Memory Block Programming

See Section 14.7, Block Init Register, and Section 14.8, Block Init Enable Register, for programming details.

This feature allows for fast initialization of the connection memory after power up. When the block programming mode is enabled, the contents of Block Init Register are written to all Connection Memory Bits. This operation completes in one 125 μs frame. During Connection Memory initialization, all TDM output streams are set to high impedance.

7.0 Data Delay Through the Switching Paths

See Section 14.1.1, Connection Memory Bit Functions, for programming details.

The switching of information from the input serial streams to the output serial streams results in a throughput delay. The device can be programmed to perform timeslot interchange functions with different throughput delay capabilities on a per-channel basis. For voice applications, select variable throughput delay to ensure minimum delay between input and output data. In wideband data application, select constant delay to maintain the frame integrity of the information through the switch. The delay through the device varies according to the type of throughput delay selected by programming the Per Channel Function (bits 31 - 29) in the Connection Memories. When these bits are set to 011, the channel is in variable delay mode. When they are set to 100, the channel is in constant delay mode.

7.1 Constant Delay Mode

In this mode the frame integrity is maintained in all switching configurations. The delay though the switch is 2 frames - Input Channel + Output Channel. This can result in a minimum delay of 1 frame + 1 channel if the last channel of a stream is switched to the first channel of a stream. The maximum delay is 1 channel short of 3 frames delay. This occurs when the first channel of a stream is switched to the last channel of a stream.

The data throughput delay is expressed as a function of ST-BUS/GCI-Bus frames, input channel number (n) and output channel number (m). The data throughput delay (T) is:

$$\mathbf{T = 2\ frames + (n - m)}$$

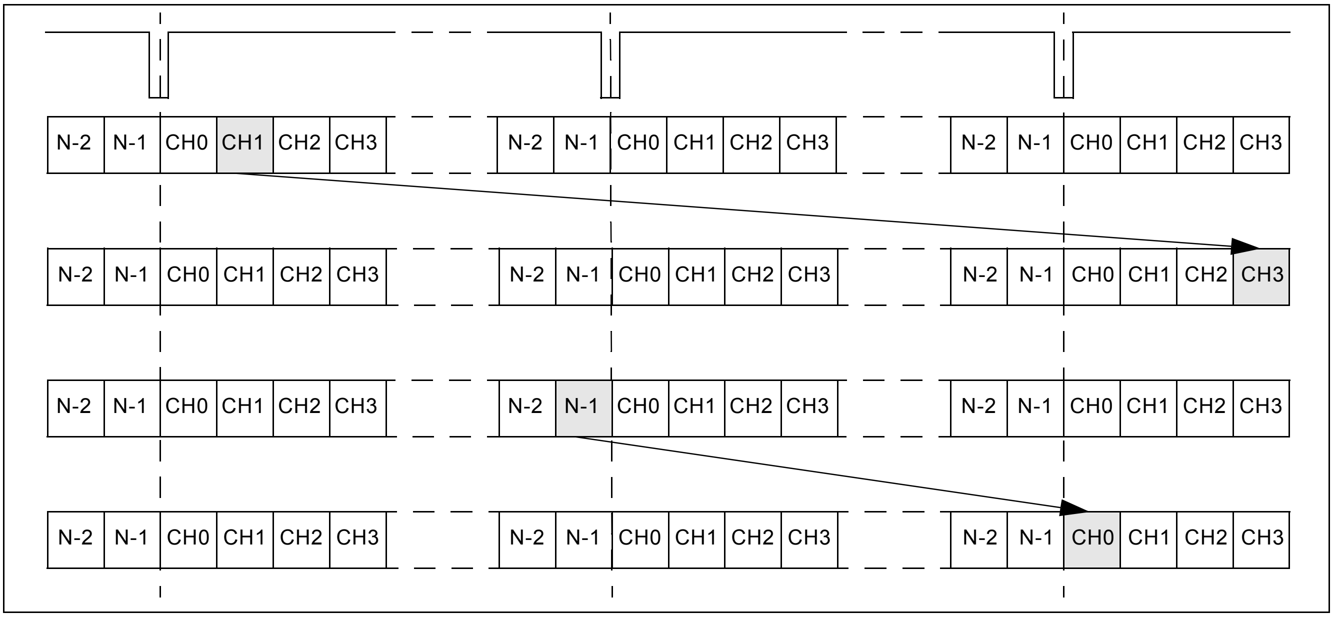

Figure 6 - Data Throughput Delay for Constant Delay

7.2 Variable Delay Mode

Variable delay mode causes the output channel to be transmitted as soon as possible. This is a useful mode for voice applications where the minimum throughput delay is more important than data integrity. The delay through the switch is minimum 3 channels and maximum 1 frame + 2 channels.

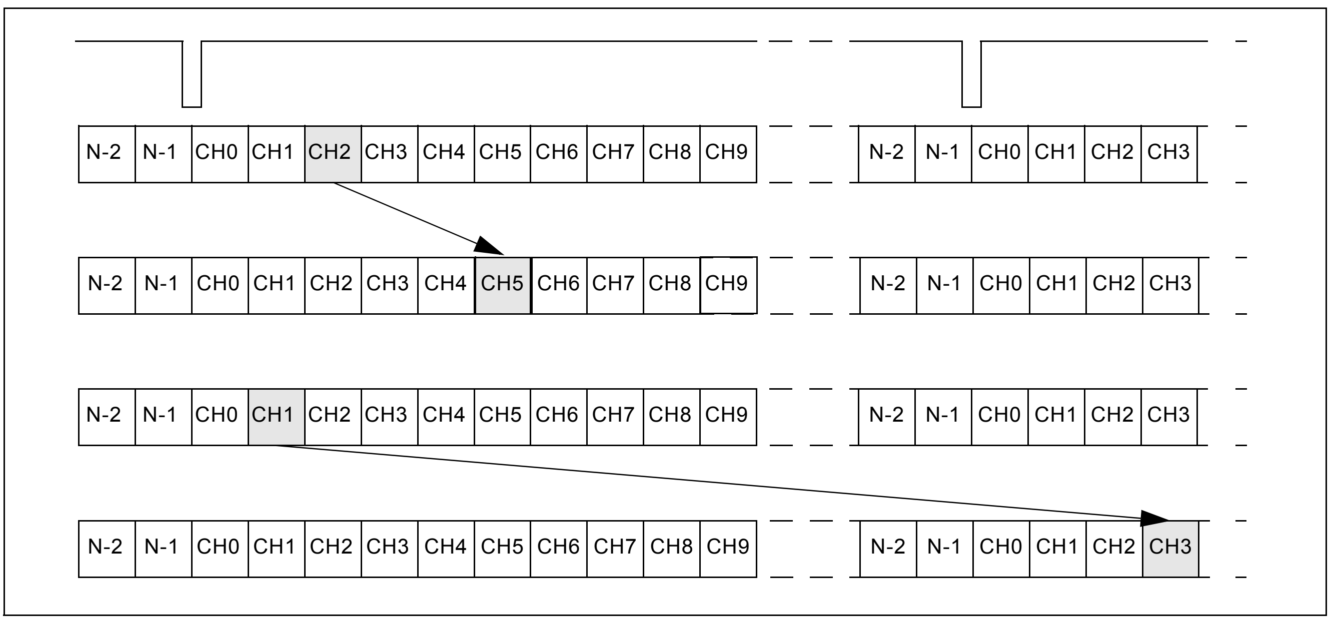

Figure 7 - Data Throughput Delay for Variable Delay

8.0 Per-Channel A-Law/μ-Law Translation

The ZL50075 provides per channel code translation to be used to adapt pulse code modulation (PCM) voice or data traffic between networks which use different encoding laws. Code translation is available in both Connection Mode and Message Mode.

This feature is controlled by the Connection Memories. The $\overline{V}$/D (bit 28) defines if the traffic in the channel is voice or data. The ICL1 - 0 (bits 27 - 26) define the input coding law and the OCL1 - 0 (bits 25 - 24) define the output coding law. The different coding options are shown in Table 4:

Input Coding (ICL1- 0)	**Output Coding (OCL1 - 0)**	**Voice Coding ($\overline{V}$/D bit = 0)**	**Data Coding ($\overline{V}$/D bit = 1)**
00	00	ITU-T G.711 A-Law	No Code
01	01	ITU-T G.711 μ-Law	Alternate Bit Inversion (ABI)
10	10	A-Law without Alternate Bit Inversion (ABI)	Inverted Alternate Bit Inversion (ABI)
11	11	μ-Law without Magnitude Inversion (MI)	All Bits Inverted

Table 4 - Input and Output Voice and Data Coding

For voice coding options, the ITU-T G.711 A-Law and ITU-T G.711 μ-Law are the standard rules for encoding. The A-Law without Alternate Bit Inversion (ABI) is an alternative code that does not invert the even bits (6, 4, 2, 0). The μ-Law without Magnitude Inversion (MI) is an alternative code that does not perform Inversion of magnitude bits (6, 5, 4, 3, 2, 1, 0).

When performing data code options, No Code does not invert the bits. The Alternate Bit Inversion (ABI) option inverts the even bits (6, 4, 2, 0) while the Inverted Alternate Bit Inversion (ABI) inverts the odd bits (7, 5, 3, 1). When All Bits Inverted is selected, all of the bits (7, 6, 5, 4, 3, 2, 1, 0) are inverted.

The input channel and output channel encoding law are configured independently. If the output channel coding is set to be different from the input channel, the ZL50075 performs translation between the two standards. If the input and output encoding laws are set to the same standard, no translation occurs.

9.0 Bit Error Rate Tester

The ZL50075 has one Bit Error Rate (BER) transmitter and one BER receiver for each pair of input and output streams, resulting in 64 transmitters connected to the output streams and 64 receivers associated with the input streams. Each transmitter can generate a BER sequence with a pattern of 2^{15}-1 Pseudo-Random Code (ITU O.151). Each transmitter can start at any location on the stream and will last for a minimum of 1 channel to a maximum of 1 frame time (125 μs). The BER transmitters are enabled by programming the Per Channel Function (bit 31 - 29) to 101 (PRBS Generator mode) in the Connection Memories.

Multiple Connection Memory locations can be programmed for BER tests. These locations are not required to be consecutive. However, when read back, the BER locations must be received in the same order that they were transmitted. If the BER locations are not received in the same order, the BER test will produce errors.

The PRBS bit pattern is sequentially loaded into the output timeslots. An example is shown in Figure 8.

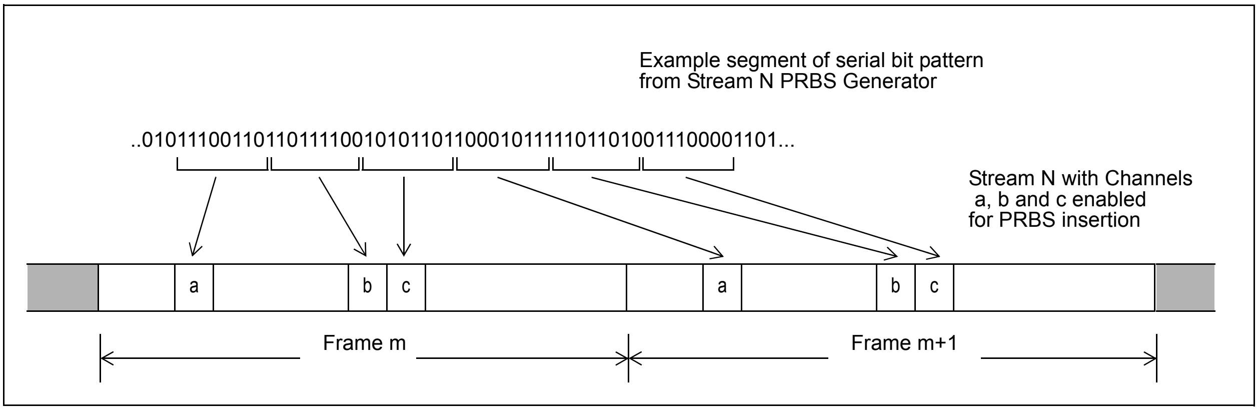

Figure 8 - Example PRBS Timeslot Insertion

Each PRBS detector can be configured to monitor for bit errors in one or more timeslots. The selection of timeslots is configured by the Input BER Enable Control Memory (IBERECM). See Section 14.3.1 for programming details, Each detector has an associated 16 bit error counter accessible via the microprocessor interface, as described in Section 14.3.2, BER Counters. The value of the counter represents the total number of errors detected on the corresponding input stream. Bit errors are accumulated until the counter is either reset (by writing to the counter or by resetting the device), or the counter reaches its maximum value, 65,535 (decimal). If more than 65,535 errors are detected, the counter will hold at the maximum value until reset.

Any number of timeslots may be configured for bit error rate testing; however the user must ensure the following for correct operation of the BER test function:

1. The number of timeslots enabled for PRBS detection on the input stream must equal the number of timeslots enabled for PRBS generation on the source output stream
2. The arrival order of timeslots at the PRBS detector must be the same as the order in which timeslots were transmitted by the PRBS generator. For example, in Figure 8 above, the timeslot order a, b, c must be maintained through the external path from source TDM output stream to destination TDM input stream.

10.0 Microprocessor Port

The ZL50075 has a generic 16-bit microprocessor port that provides access to the 32-bit internal Data Memory (read access only), Connection Memory and Control Registers. D15 on the bus maps to Bit 31 and Bit 15 of the internal 32 bit memory or register, D14 maps to Bit 30 and Bit 14, etc.

The IM pin is used to select between Motorola bus control and Intel bus control. If the IM input is low, then a Motorola control is selected. If the IM bit is high, then an Intel control is selected. Regardless of which bus configuration is selected, the bus cycle termination signals $\overline{\text{WAIT}}$ & $\overline{\text{DTA}}$ are both provided.

The Data Memory, Connection Memory and Control Registers are assigned 32 bit fields in the ZL50075 memory space. Each 32 bit memory or register location spans 4 consecutive addresses. Example:

- The 32 bit Group Control Register for TDM Group 0 is located at address range 40200 - 40203 Hex

The Least Significant address identifies the Most Significant Byte (MSB) in the 32 bit field, as illustrated in Table 5.

Address (Hex)	Memory/Register Bits
40200	Bits 31:24 (MSB)
40201	Bits 23:16
40202	Bits 15:8
40203	Bits 7:0 (LSB)

Table 5 - Example of Address and Byte Significance

The Address Bus, A18 - 0, controls access to each 32 bit location. A0 is not used and must be connected to defined logic level. Address bit A1 and the Data Transfer Size inputs, SIZ1 - 0, identify which bytes are being accessed.

In Motorola Bus Mode (IM = 0), SIZ1 - 0 form active low data strobe signals, consistent with $\overline{UDS}$ and $\overline{LDS}$ available on the MC68000 and MC68302 processors, as shown in Table 6.

In Intel Bus Mode (IM = 1), SIZ1 - 0 form active low byte enable signals, consistent with $\overline{BE1}$ and $\overline{BE0}$ available on the Intel i960 processor, as shown in Table 6.

Pin Name	Motorola Mode MC68000, MC68302 Equivalent Function IM = 0	Intel Mode i960 Equivalent Function IM = 1	Data Bus Bytes Enabled
SIZ1	$\overline{UDS}$	$\overline{BE1}$	D15-8
SIZ0	$\overline{LDS}$	$\overline{BE0}$	D7-0

Table 6 - Byte Enable Signals

In both Intel and Motorola modes, the A1 address input is used to identify the word alignment in internal memory, as shown in Table 7.

A1	Memory Data Word Alignment
0	Bits 31:16
1	Bits 15:0

Table 7 - Memory Data Word Alignment

Data bus word alignments are shown in Table 8. An example of byte addressing is given in Table 9.

Microprocessor 16 Bit Data Bus	SIZ1	SIZ0	A1	Internal 32-Bit Memory or Register
D15 - 8	0	1	0	Bits 31:24
	0	1	1	Bits 15:8
D7 - 0	1	0	0	Bits 23:16
	1	0	1	Bits 7:0
D15 - 0	0	0	0	Bits 31:16
	0	0	1	Bits 15:0
	1	1	X[1]	No access

Table 8 - Data Bus Word Alignment

1. X - Don't Care

Address (Hex)	Register Description	Register Byte	A18 - 0 (binary)	SIZ1	SIZ0	Comments
40200 or 40201	Group Control Register (Group 0)	Bits 23:16	100 0000 0010 0000 000X†	1	0	8 bit transfer
40282 or 40283	Input Clock Control Register	Bits 15:8	100 0000 0010 1000 001X†	0	1	8 bit transfer
40286 or 40287	Output Clock Control Register	Bits 15:0	100 0000 0010 1000 011X†	0	0	16 bit transfer
40284 or 40285	Output Clock Control Register	Bits 31:16	100 0000 0010 1000 010X†	0	0	16 bit transfer

Table 9 - Byte Address Examples

† - Don't Care. A0 is not used.

10.1 Bus Operation

10.1.1 Read Cycle

The operation of a read cycle is illustrated in Figure 9.

- The microprocessor asserts the R/W control signal high, to signal a read cycle. It also drives the address A, transfer size, SIZ1 - 0, and chip select logic drives the CS signal active low to select the ZL50075
- The microprocessor then drives the DS signal active low, to signal the start of the bus cycle. The DS signal is held low for the duration of the bus cycle
- WAIT is asserted active low
- The ZL50075 accesses the requested memory or register location(s), and places the requested data onto the data bus, D15 - 0. All data bus pins are driven, whether or not they are being used for the specific data transfer. Unused pins will present unknown data. If the address is to an unused area of the memory space, unknown data is presented on the data bus
- The ZL50075 then de-asserts WAIT, and asserts either DTA or BERR, depending on the validity of the data transfer
- When the microprocessor observes the active low state of the DTA or the BERR signal or the low-to-high transition of the WAIT signal, it terminates the bus cycle by driving the DS pin inactive high
- When the ZL50075 sees the DS signal go inactive high, it removes the assertions on the DTA or BERR signals by driving them inactive high
- When the ZL50075 sees the CS signal go inactive high, it tri-states the data bus, D15 - 0 and the DTA, BERR and WAIT signals. However, if CS goes inactive high before DS goes inactive high, the DTA, BERR and WAIT signals are driven inactive high before they are tri-stated
- In Intel mode, DTA is always driven to signal the end of a bus cycle, regardless of BERR