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ZL50110/11/12/14

128, 256, 512 and 1024 Channel CESoP Processors

Data Sheet

October 2009

Features

General

- Circuit Emulation Services over Packet (CESoP) transport for MPLS, IP and Ethernet networks
- On chip timing & synchronization recovery across a packet network
- Grooming capability for Nx64 Kbps trunking

Circuit Emulation Services

- Supports ITU-T Recommendation Y.1413 and Y.1453
- Supports IETF RFC4553 and RFC5086
- Supports MEF8 and MFA 8.0.0
- Structured, synchronous CESoP with clock recovery
- Unstructured, asynchronous CESoP, with integral per stream clock recovery

TDM Interfaces

- Up to 32 T1/E1, 8 J2, or 2 T3/E3 ports
- H.110, H-MVIP, ST-BUS backplanes
- Up to 1024 bi-directional 64 Kbps channels
- Direct connection to LIUs, framers, backplanes

Ordering Information

ZL50110GAG	552 PBGA	Trays, Bake & Drypack
ZL50111GAG	552 PBGA	Trays, Bake & Drypack
ZL50112GAG	552 PBGA	Trays, Bake & Drypack
ZL50114GAG	552 PBGA	Trays, Bake & Drypack
ZL50110GAG2	552 PBGA**	Trays, Bake & Drypack
ZL50111GAG2	552 PBGA**	Trays, Bake & Drypack
ZL50112GAG2	552 PBGA**	Trays, Bake & Drypack
ZL50114GAG2	552 PBGA**	Trays, Bake & Drypack

**Pb Fee Tin Silver/Copper

-40°C to +85°C

- Dual reference Stratum 4 and 4E DPLL for synchronous operation

Network Interfaces

- Up to 3 x 100 Mbps MII Fast Ethernet or Dual Redundant 1000 Mbps GMII/TBI Ethernet Interfaces

System Interfaces

- Flexible 32 bit host CPU interface (Motorola PowerQUICC™ compatible)
- On-chip packet memory for self-contained operation, with buffer depths of over 16 ms
- Up to 8 Mbytes of off-chip packet memory, supporting buffer depths of over 128 ms

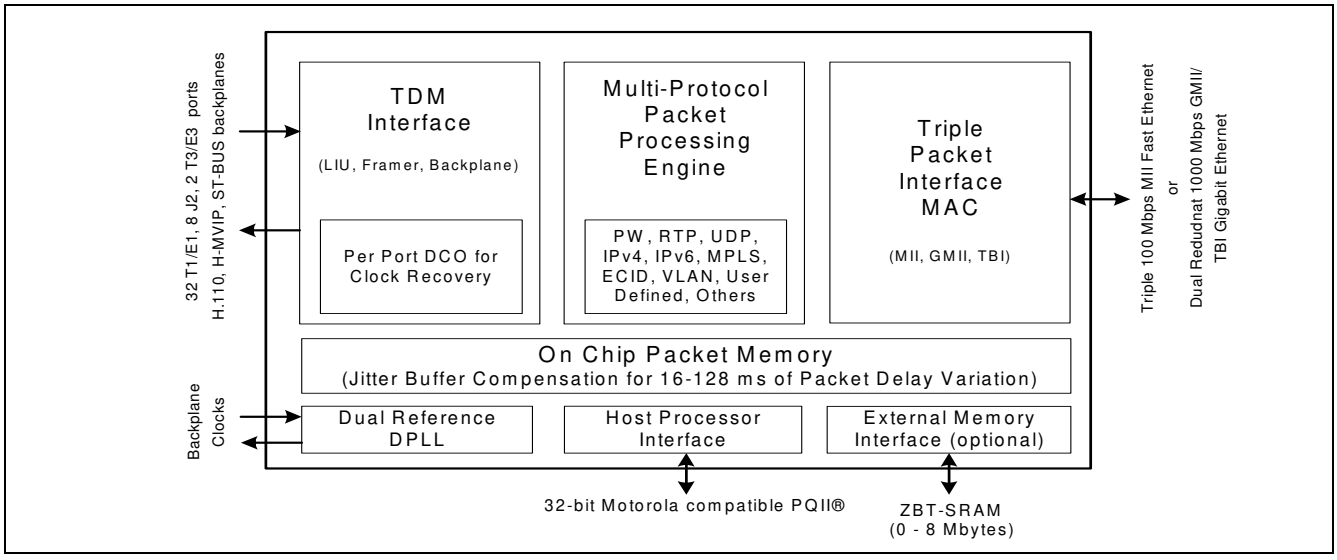

Figure 1 - ZL50111 High Level Overview

Packet Processing Functions

- Flexible, multi-protocol packet encapsulation including support for IPv4, IPv6, RTP, MPLS, L2TPv3, ITU-T Y.1413, RFC4553, RFC5086 and user programmable
- Packet re-sequencing to allow lost packet detection
- Four classes of service with programmable priority mechanisms (WFQ and SP) using egress queues
- Flexible classification of incoming packets at layers 2, 3, 4 and 5
- Supports up to 128 separate CESoP connections across the Packet Switched Network

Applications

- Circuit Emulation Services over Packet Networks
  - Leased Line support over packet networks
  - Multi-Tenant Unit access concentration
  - TDM over Cable
  - Fibre To The Premises G/E-PON
  - Layer 2 VPN services
- Customer-premise and Provider Edge Routers and Switches
- Packet switched backplane applications

Description

The ZL50110/11/12/14 family of CESoP processors are highly functional TDM to Packet bridging devices. The ZL50110/11/12/14 provides both structured and unstructured circuit emulation services over packet (CESoP) for up to 32 T1, 32 E1 and 8 J2 streams across a packet network based on MPLS, IP or Ethernet. The ZL50111 also supports unstructured T3 and E3 streams.

The circuit emulation features in the ZL50110/11/12/14 family supports the ITU Recommendations Y.1413 and Y.1453, as well as the CESoP standards from the Metro Ethernet Forum (MEF)–and MPLS and Frame Relay Alliance. The ZL50110/11/14 also supports IETF RFC4553 and RFC5086.

The ZL50110/11/12/14 provides up to triple 100 Mbps MII ports or dual redundant 1000 Mbps GMII/TBI ports.

The ZL50110/11/12/14 incorporates a range of powerful clock recovery mechanisms for each TDM stream, allowing the frequency of the source clock to be faithfully generated at the destination, enabling greater system performance and quality. Timing is carried using RTP or similar protocols, and both adaptive and differential clock recovery schemes are included, allowing the customer to choose the correct scheme for the application. An externally supplied clock may also be used to drive the TDM interface of the ZL50110/11/12/14.

The ZL50110/11/12/14 incur very low latency for the data flow, thereby increasing QoS when carrying voice services across the Packet Switched Network. Voice, when carried using CESoP, which typically has latencies of less than 10 ms, does not require expensive processing such as compression and echo cancellation.

The ZL50110/11/12/14 is capable of assembling user-defined packets of TDM traffic from the TDM interface and transmitting them out the packet interfaces using a variety of protocols. The ZL50110/11/12/14 supports a range of different packet switched networks, including Ethernet VLANs, IP and MPLS.

The ZL50110/11/12/14 can support up to 4 protocol stacks at the same time, provided that each protocol stack can be uniquely identified by a mask & match approach.

Packets received from the packet interfaces are parsed to determine the egress destination, and are appropriately queued to the TDM interface, they can also be forwarded to the host interface, or back toward the packet interface. Packets queued to the TDM interface can be re-ordered based on sequence number, and lost packets filled in to maintain timing integrity.

The ZL50110/11/12/14 family includes sufficient on-chip memory that external memory is not required in most applications. This reduces system costs and simplifies the design. For applications that do require more memory (e.g., high stream count or high latency), the device supports up to 8 Mbytes of SSRAM.

A comprehensive evaluation system is available upon request from your local Zarlink representative or distributor. This system includes the CESoP processor, various TDM interfaces and a fully featured evaluation software GUI that runs on a Windows PC.

Device Line Up

There are four products within the ZL50110/11/12/14 family, with capacity as shown in the following table:

Device	TDM Interfaces	Ethernet Packet I/F	Notes
ZL50114	4 T1, 4 E1, or 1 J2 streams or 4 MVIP/ST-BUS streams at 2.048 Mbps or 1 H.110/H-MVIP/ST-BUS streams at 8.192 Mbps	Dual 100 Mbps MII or Dual Redundant 1000 Mbps GMII/TBI	Note 1
ZL50110	8 T1, 8 E1 or 2 J2 streams or 8 MVIP/ST-BUS streams at 2.048 Mbps or 2 H.110/H-MVIP/ST-BUS streams at 8.192 Mbps	Dual 100 Mbps MII or Dual Redundant 1000 Mbps GMII/TBI	Note 1
ZL50112	16 T1, 16 E1, 4 J2 streams or 16 MVIP/ST-BUS streams at 2.048 Mbps or 4 H.110/H-MVIP/ST-BUS streams at 8.192 Mbps	Triple 100 Mbps MII or Dual Redundant 1000 Mbps GMII/TBI or Single 100 Mbps MII and Single 1000 Mbps GMII/TBI	Note 1
ZL50111	32 T1, 32 E1, 8 J2, 2 T3, 2 E3 streams or 32 MVIP/ST-BUS streams at 2.048 Mbps or 8 H.110/H-MVIP/ST-BUS streams at 8.192 Mbps	Triple 100 Mbps MII or Dual Redundant 1000 Mbps GMII/TBI or Single 100 Mbps MII and Single 1000 Mbps GMII/TBI	Note 1

Table 1 - Capacity of Devices in the ZL50110/11/14 Family

Note 1: T1/E1/J2 is for unstructured mode, and the H-MVIP/H.110/ST-BUS is for structured mode.

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1.0 Changes Summary

The following table captures the changes from the March 2009 issue.

Page	Item	Change
1	MEF logo	Added MEF logo to show MEF 18 certification.

The following table captures the changes from the January 2009 issue.

Page	Item	Change
61 & 64	Section 5.4 and Section 5.8	Replaced ZLAN-202 with ZL5011x Design Manual section “13.1 Understanding forceDelete”.
67	Section 6.3	Replaced ZLAN-143 with ZL5011x Design Manual section “3.6 System Clock Block.”
69	Section 7.4	Replaced ZLAN-159 with ZL5011x Design Manual section “3.1.1 Connection to LIU”.
94	Section 11.6.5	Replaced ZLAN-239 with ZL5011x Design Manual section “7.1.3.1 TBI Interface Timing”.
109	Section 14.1	Removed references to IETF PWE3 draft-ietf-l2tpext-l2tp-base and IETF PWE3 draft-ietf-pwe3-cesop.

The following table captures the changes from the April 2008 issue.

Page	Item	Change
68	Section 7.3	Add Note 3

The following table captures the changes from the October 2006 issue.

Page	Item	Change
Several	Include ZL50112 device	Add description for ZL50112
1, 2 and 3	Standard	Updated IETF RFC number and standards in general
1, 58, 74, 75 and 77	Stratum 3 DPLL	Updated the description for Stratum 3 DPLL
1, 4, 24, 52 and 59	STS-1 stream	Remove STS-1 stream
14	Section 2.0	Combine the packaged descriptions for all devices
33	Section 3.3	Include more detailed description for the packet interface
49	Section 3.7.2	ZL50112 and ZL50111 share the same JTAG ID
56	Section 4.6	Change the title of the section
57	Section 5.0	Add a note about jumbo packets
59	Section 5.3	Include a paragraph to clarify the support for structure and unstructure modes at the same time
61	Section 5.4	Include more detailed description for the Payload Assembly
63	Section 5.4.2	Add a note at the end of the section
64	Section 5.8	Include more detailed description for the TDM formatter

Page	Item	Change
65	Section 6.0	Include more detailed description for Clock Recovery
65	Section 6.1	Include more detailed description for Differential Clock Recovery
66	Section 6.2	Updated the description of Adaptive Clock Recovery
73	Section 7.9	Added sub sections
87	Table 32	TDM_HDS Input Setup and TDM_HDS Input Hold, Max. time corrected.
94	Section 11.6.5	Updated TXD[9:0] output delay
95	Section 11.6.6	UpdatedSection 11.6.6 Management Interface Timing (M_MDIO hold time and Figure 40)
97	Figure 43 and Figure 44	CPU_$\overline{TS}$_ALE and $\overline{CPU\_TA}$. Added mode details in Figure 43 and Figure 44 Added the $\overline{CPU\_TA}$ assertion time.

The following table captures the changes from the February 2006 issue.

Page	Item	Change
96	Table 41, Table 41 - External Memory Timing	Added Minimum Values

The following table captures the changes from the April 2005 issue.

Page	Item	Change
		Clarified ZL50111 supports 3 MII ports, ZL50110/4 support 2 MII ports.
48, 49	Section 3.6 and Section 3.7.2	Added external pull-up/pull-down resistor recommendations for SYSTEM_RST, SYSTEM_DEBUG, JTAG_TRST, JTAG_TCK.
67	Section 6.3	Added Section 6.3 SYSTEM_CLK Considerations.

The following table captures the changes from the January 2005 issue.

Page	Item	Change
		Clarified data sheet to indicate ZL50110/11/12/14 supports clock recovery in both synchronous and asynchronous modes of operation.
99	Figure 45	Inverted polarity of $\overline{CPU\_DREQ0}$ and $\overline{CPU\_DREQ1}$ to conform with default MPC8260. Polarity of $\overline{CPU\_DREQ}$ and $\overline{CPU\_SDACK}$ remains programmable through API.
99	Figure 46	Inverted polarity of $\overline{CPU\_DREQ0}$ and $\overline{CPU\_DREQ1}$ to conform with default MPC8260. Polarity of $\overline{CPU\_DREQ}$ and $\overline{CPU\_SDACK}$ remains programmable through API.

The following table captures the changes from the October 2004 issue.

Page	Item	Change
49	Section 3.7.1	Added 5 kohm pulldown recommendation to GPIO signals.

The following table captures the changes from the September 2004 issue.

Page	Item	Change
12, 16, 19	Fig. 2 and Ball Signal Assignment Table	Corrected Mx_LINKUP_LED pin assignment.
73	DC Electrical Characteristics Table and Output Levels Table	Changed Electrical Characteristics to differentiate between 3.3 V and 5 V tolerant signals.
98	Section 13.3	New section added; Mx_LINKUP_LED Outputs.

2.0 Physical Specification

The ZL50110/11/12/14 is packaged in a PBGA device.

Features:

- Body Size: 35 mm x 35 mm (typ)
- Ball Count: 552
- Ball Pitch: 1.27 mm (typ)
- Ball Matrix: 26 x 26
- Ball Diameter: 0.75 mm (typ)
- Total Package Thickness: 2.33 mm (typ)

ZL50111 Package view from TOP side. Note that ball A1 is non-chamfered corner.

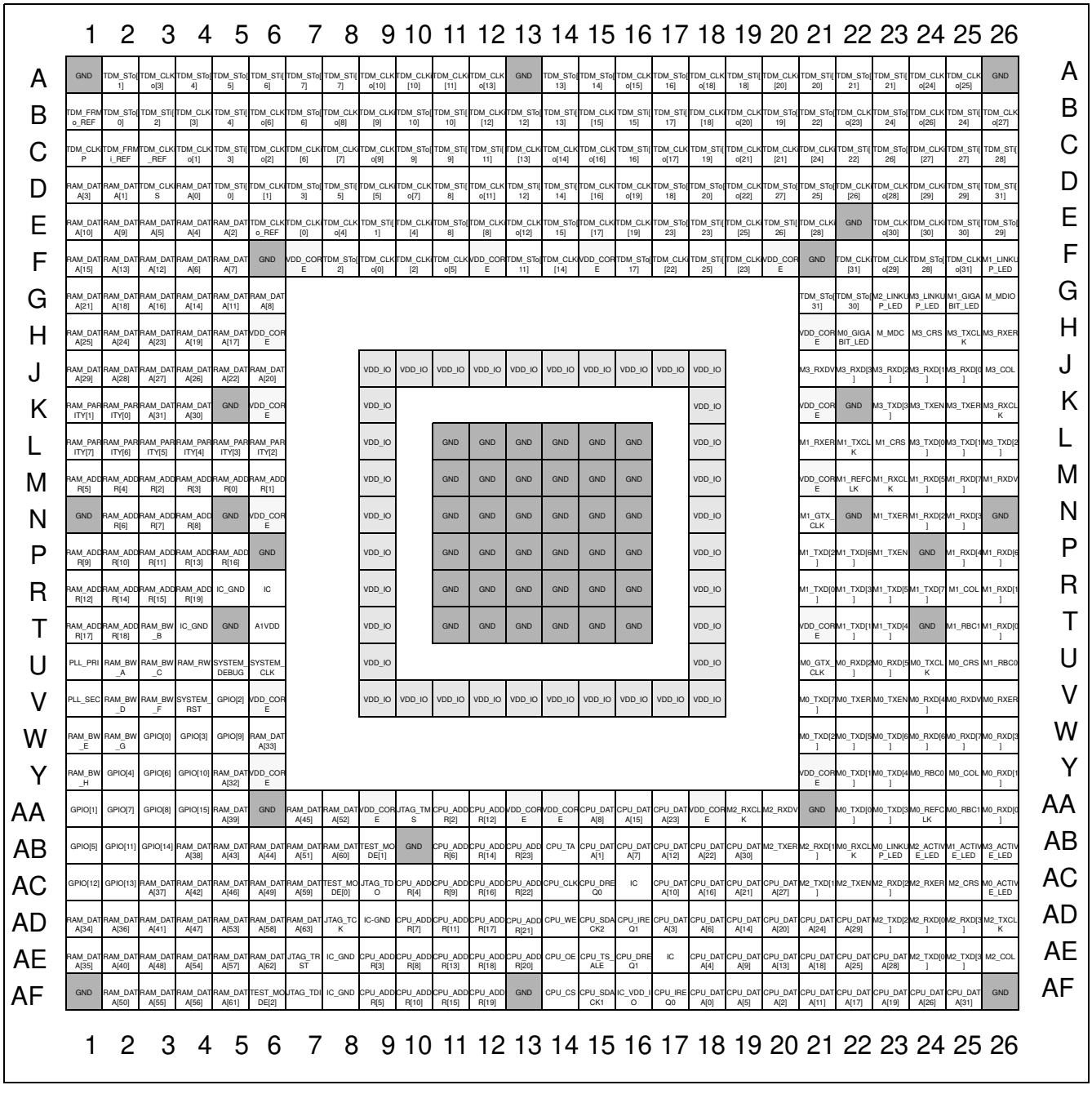
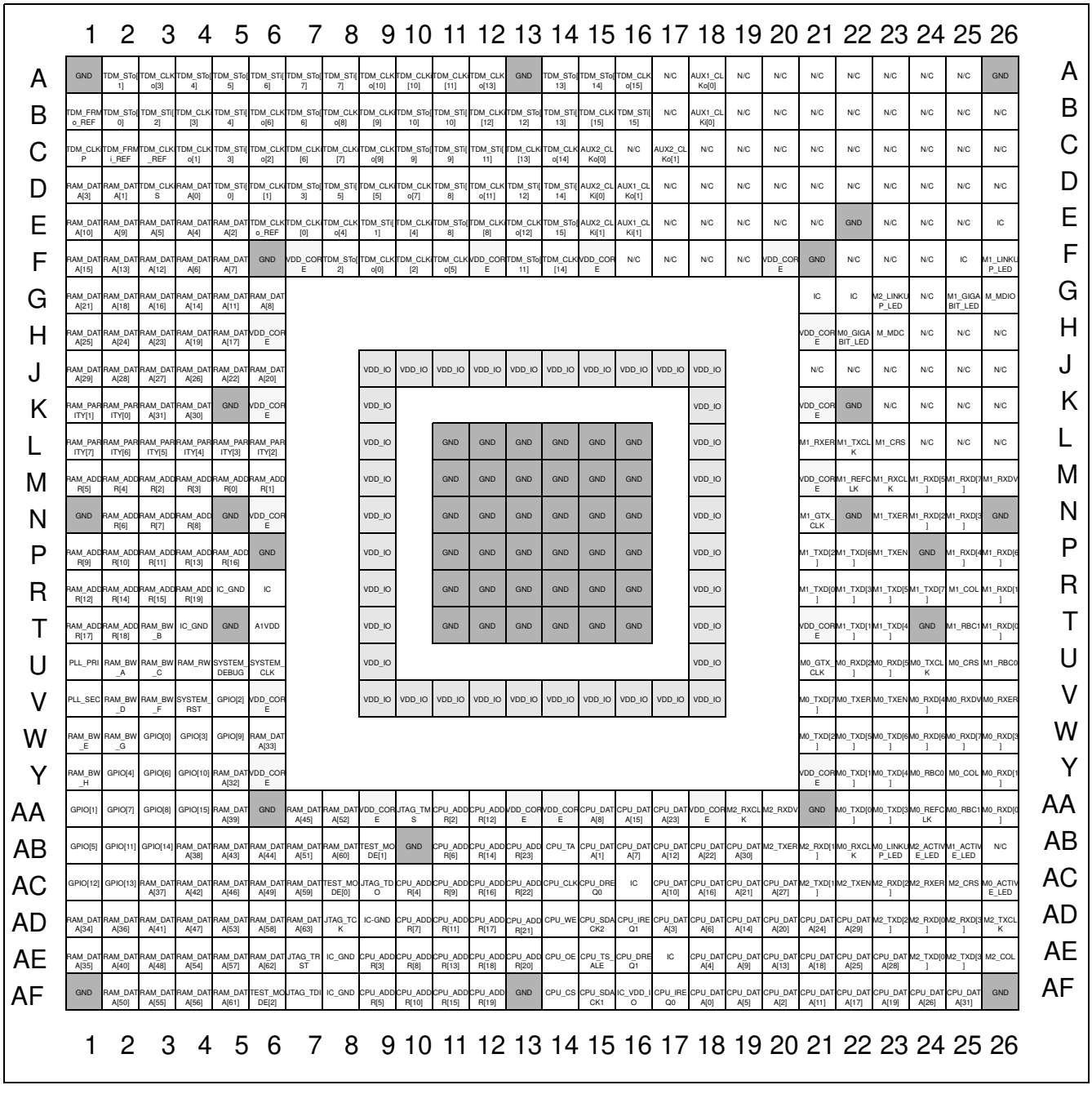


Figure 2 - ZL50111 Package View and Ball Positions

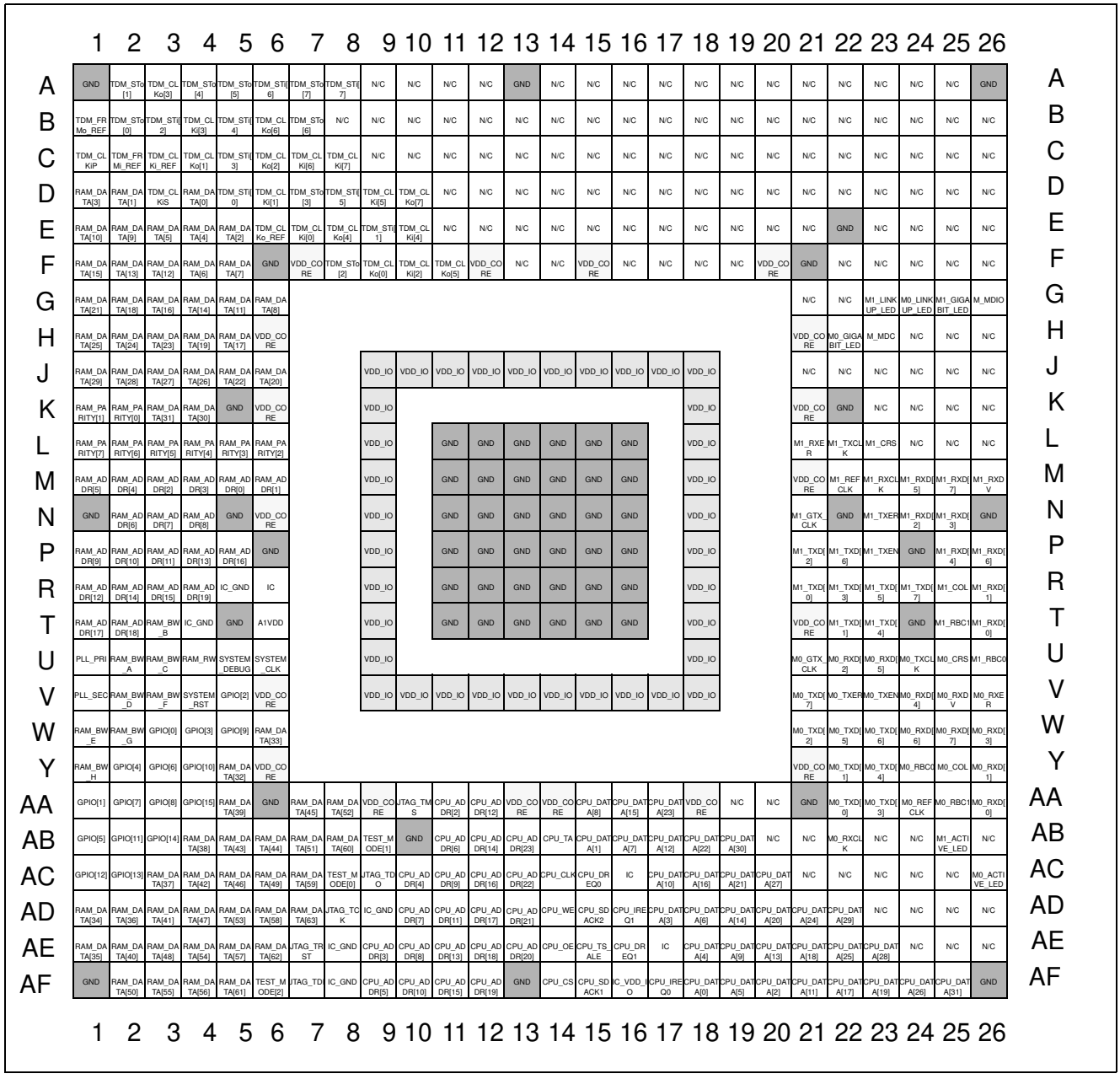
ZL50112 Package view from TOP side. Note that ball A1 is non-chamfered corner.



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
A	GND	TDM_STo[1]	TDM_CLKo[3]	TDM_STo[4]	TDM_STo[5]	TDM_STi[6]	TDM_STo[7]	TDM_STi[7]	TDM_CLKo[10]	TDM_CLK[10]	TDM_CLK[11]	TDM_CLKo[13]	GND	TDM_STo[13]	TDM_STo[14]	TDM_CLKo[15]	N/C	AUX1_CLKo[0]	N/C	N/C	N/C	N/C	N/C	N/C	N/C	GND
B	TDM_FRMo_REF	TDM_STo[0]	TDM_STi[2]	TDM_CLK[3]	TDM_STi[4]	TDM_CLKo[6]	TDM_STo[6]	TDM_CLK[8]	TDM_CLK[9]	TDM_STo[10]	TDM_STi[10]	TDM_CLK[12]	TDM_STo[12]	TDM_STi[13]	TDM_CLK[15]	TDM_STi[15]	N/C	AUX1_CLKi[0]	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C
C	TDM_CLKP	TDM_FRMi_REF	TDM_CLK_REF	TDM_CLKo[1]	TDM_STi[3]	TDM_CLKo[2]	TDM_CLK[6]	TDM_CLK[7]	TDM_CLKo[9]	TDM_STo[9]	TDM_STi[9]	TDM_STi[11]	TDM_CLK[13]	TDM_CLKo[14]	AUX2_CLKo[0]	N/C	AUX2_CLKo[1]	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C
D	RAM_DATA[3]	RAM_DATA[1]	TDM_CLKS	RAM_DATA[0]	TDM_STi[0]	TDM_CLKo[1]	TDM_STo[3]	TDM_STo[5]	TDM_CLKo[5]	TDM_CLKo[7]	TDM_STi[8]	TDM_CLKo[11]	TDM_STo[12]	TDM_STi[14]	AUX2_CLKi[0]	AUX1_CLKo[1]	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C
E	RAM_DATA[10]	RAM_DATA[9]	RAM_DATA[5]	RAM_DATA[4]	RAM_DATA[2]	TDM_CLKo_REF	TDM_CLKo[0]	TDM_CLKo[4]	TDM_STi[1]	TDM_CLK[4]	TDM_STo[8]	TDM_CLKo[12]	TDM_CLKo[15]	TDM_STo[15]	AUX2_CLKi[1]	AUX1_CLKi[1]	N/C	N/C	N/C	N/C	N/C	GND	N/C	N/C	N/C	IC
F	RAM_DATA[15]	RAM_DATA[13]	RAM_DATA[12]	RAM_DATA[6]	RAM_DATA[7]	GND	VDD_CORE	TDM_STo[2]	TDM_CLKo[0]	TDM_CLK[2]	TDM_CLKo[5]	VDD_CORE	TDM_STo[11]	TDM_CLK[14]	VDD_CORE	N/C	N/C	N/C	N/C	VDD_CORE	GND	N/C	N/C	N/C	IC	M1_LINKUP_LED
G	RAM_DATA[21]	RAM_DATA[18]	RAM_DATA[16]	RAM_DATA[14]	RAM_DATA[11]	RAM_DATA[8]															IC	IC	M2_LINKUP_LED	N/C	M1_GIGABIT_LED	M_MDIO
H	RAM_DATA[25]	RAM_DATA[24]	RAM_DATA[23]	RAM_DATA[19]	RAM_DATA[17]	VDD_CORE															VDD_CORE	M0_GIGABIT_LED	M_MDC	N/C	N/C	N/C
J	RAM_DATA[29]	RAM_DATA[28]	RAM_DATA[27]	RAM_DATA[26]	RAM_DATA[22]	RAM_DATA[20]			VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO			N/C	N/C	N/C	N/C	N/C	N/C
K	RAM_PARITY[1]	RAM_PARITY[0]	RAM_DATA[31]	RAM_DATA[30]	GND	VDD_CORE			VDD_IO									VDD_IO			VDD_CORE	GND	N/C	N/C	N/C	N/C
L	RAM_PARITY[7]	RAM_PARITY[6]	RAM_PARITY[5]	RAM_PARITY[4]	RAM_PARITY[3]	RAM_PARITY[2]			VDD_IO	GND	GND	GND	GND	GND	GND	GND		VDD_IO			M1_RXER	M1_TXCLK	M1_CRS	N/C	N/C	N/C
M	RAM_ADDR[5]	RAM_ADDR[4]	RAM_ADDR[2]	RAM_ADDR[3]	RAM_ADDR[0]	RAM_ADDR[1]			VDD_IO	GND	GND	GND	GND	GND	GND	GND		VDD_IO			VDD_CORE	M1_REFCLK	M1_RXCLK	M1_RXD[5]	M1_RXD[7]	M1_RXDV
N	GND	RAM_ADDR[6]	RAM_ADDR[7]	RAM_ADDR[8]	GND	VDD_CORE			VDD_IO	GND	GND	GND	GND	GND	GND	GND		VDD_IO			M1_GTX_CLK	GND	M1_TXER	M1_RXD[2]	M1_RXD[3]	GND
P	RAM_ADDR[9]	RAM_ADDR[10]	RAM_ADDR[11]	RAM_ADDR[13]	RAM_ADDR[16]	GND			VDD_IO	GND	GND	GND	GND	GND	GND	GND		VDD_IO			M1_TXD[2]	M1_TXD[6]	M1_TXEN	GND	M1_RXD[4]	M1_RXD[6]
R	RAM_ADDR[12]	RAM_ADDR[14]	RAM_ADDR[15]	RAM_ADDR[19]	IC_GND	IC			VDD_IO	GND	GND	GND	GND	GND	GND	GND		VDD_IO			M1_TXD[0]	M1_TXD[3]	M1_TXD[5]	M1_TXD[7]	M1_COL	M1_RXD[1]
T	RAM_ADDR[17]	RAM_ADDR[18]	RAM_BW_B	IC_GND	GND	A1VDD			VDD_IO	GND	GND	GND	GND	GND	GND	GND		VDD_IO			VDD_CORE	M1_TXD[1]	M1_TXD[4]	GND	M1_RBC1	M1_RXD[0]
U	PLL_PRI	RAM_BW_A	RAM_BW_C	RAM_RW	SYSTEM_DEBUG	SYSTEM_CLK			VDD_IO									VDD_IO			M0_GTX_CLK	M0_RXD[2]	M0_RXD[5]	M0_TXCLK	M0_CRS	M1_RBC0
V	PLL_SEC	RAM_BW_D	RAM_BW_F	SYSTEM_RST	GPIO[2]	VDD_CORE			VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO			M0_TXD[7]	M0_TXER	M0_TXEN	M0_RXD[4]	M0_RXDV	M0_RXER
W	RAM_BW_E	RAM_BW_G	GPIO[0]	GPIO[3]	GPIO[9]	RAM_DATA[33]															M0_TXD[2]	M0_TXD[5]	M0_TXD[6]	M0_RXD[6]	M0_RXD[7]	M0_RXD[3]
Y	RAM_BW_H	GPIO[4]	GPIO[6]	GPIO[10]	RAM_DATA[32]	VDD_CORE															VDD_CORE	M0_TXD[1]	M0_TXD[4]	M0_RBC0	M0_COL	M0_RXD[1]
AA	GPIO[1]	GPIO[7]	GPIO[8]	GPIO[15]	RAM_DATA[39]	GND	RAM_DATA[45]	RAM_DATA[52]	VDD_CORE	JTAG_TMS	CPU_ADDR[2]	CPU_ADDR[12]	VDD_CORE	VDD_CORE	CPU_DATA[8]	CPU_DATA[15]	CPU_DATA[23]	VDD_CORE	M2_RXCLK	M2_RXDV	GND	M0_TXD[0]	M0_TXD[3]	M0_REFCLK	M0_RBC1	M0_RXD[0]
AB	GPIO[5]	GPIO[11]	GPIO[14]	RAM_DATA[38]	RAM_DATA[43]	RAM_DATA[44]	RAM_DATA[51]	RAM_DATA[60]	TEST_MODE[1]	GND	CPU_ADDR[6]	CPU_ADDR[14]	CPU_ADDR[23]	CPU_TA	CPU_DATA[1]	CPU_DATA[7]	CPU_DATA[12]	CPU_DATA[22]	CPU_DATA[30]	M2_TXER	M2_RXD[1]	M0_RXCLK	M0_LINKUP_LED	M2_ACTIVE_LED	M1_ACTIVE_LED	N/C
AC	GPIO[12]	GPIO[13]	RAM_DATA[37]	RAM_DATA[42]	RAM_DATA[46]	RAM_DATA[49]	RAM_DATA[59]	TEST_MODE[0]	JTAG_TDO	CPU_ADDR[4]	CPU_ADDR[9]	CPU_ADDR[16]	CPU_ADDR[22]	CPU_CLK	CPU_DREQ0	IC	CPU_DATA[10]	CPU_DATA[16]	CPU_DATA[21]	CPU_DATA[27]	M2_TXD[1]	M2_TXEN	M2_RXD[2]	M2_RXER	M2_CRS	M0_ACTIVE_LED
AD	RAM_DATA[34]	RAM_DATA[36]	RAM_DATA[41]	RAM_DATA[47]	RAM_DATA[53]	RAM_DATA[58]	RAM_DATA[63]	JTAG_TCK	IC-GND	CPU_ADDR[7]	CPU_ADDR[11]	CPU_ADDR[17]	CPU_ADDR[21]	CPU_WE	CPU_SDACK2	CPU_IREQ1	CPU_DATA[3]	CPU_DATA[6]	CPU_DATA[14]	CPU_DATA[20]	CPU_DATA[24]	CPU_DATA[25]	M2_TXD[2]	M2_RXD[0]	M2_RXD[3]	M2_TXCLK
AE	RAM_DATA[35]	RAM_DATA[40]	RAM_DATA[48]	RAM_DATA[54]	RAM_DATA[57]	RAM_DATA[62]	JTAG_TRST	IC_GND	CPU_ADDR[3]	CPU_ADDR[8]	CPU_ADDR[13]	CPU_ADDR[18]	CPU_ADDR[20]	CPU_OE	CPU_TSALE	CPU_DREQ1	IC	CPU_DATA[4]	CPU_DATA[9]	CPU_DATA[13]	CPU_DATA[18]	CPU_DATA[28]	M2_TXD[0]	M2_TXD[3]	M2_COL	
AF	GND	RAM_DATA[50]	RAM_DATA[55]	RAM_DATA[56]	RAM_DATA[61]	TEST_MODE[2]	JTAG_TDI	IC_GND	CPU_ADDR[5]	CPU_ADDR[10]	CPU_ADDR[15]	CPU_ADDR[19]	GND	CPU_CS	CPU_SDACK1	IC_VDD_IO	CPU_IREQ0	CPU_DATA[0]	CPU_DATA[5]	CPU_DATA[2]	CPU_DATA[11]	CPU_DATA[17]	CPU_DATA[19]	CPU_DATA[26]	CPU_DATA[31]	GND

Figure 3 - ZL50112 Package View and Ball Positions

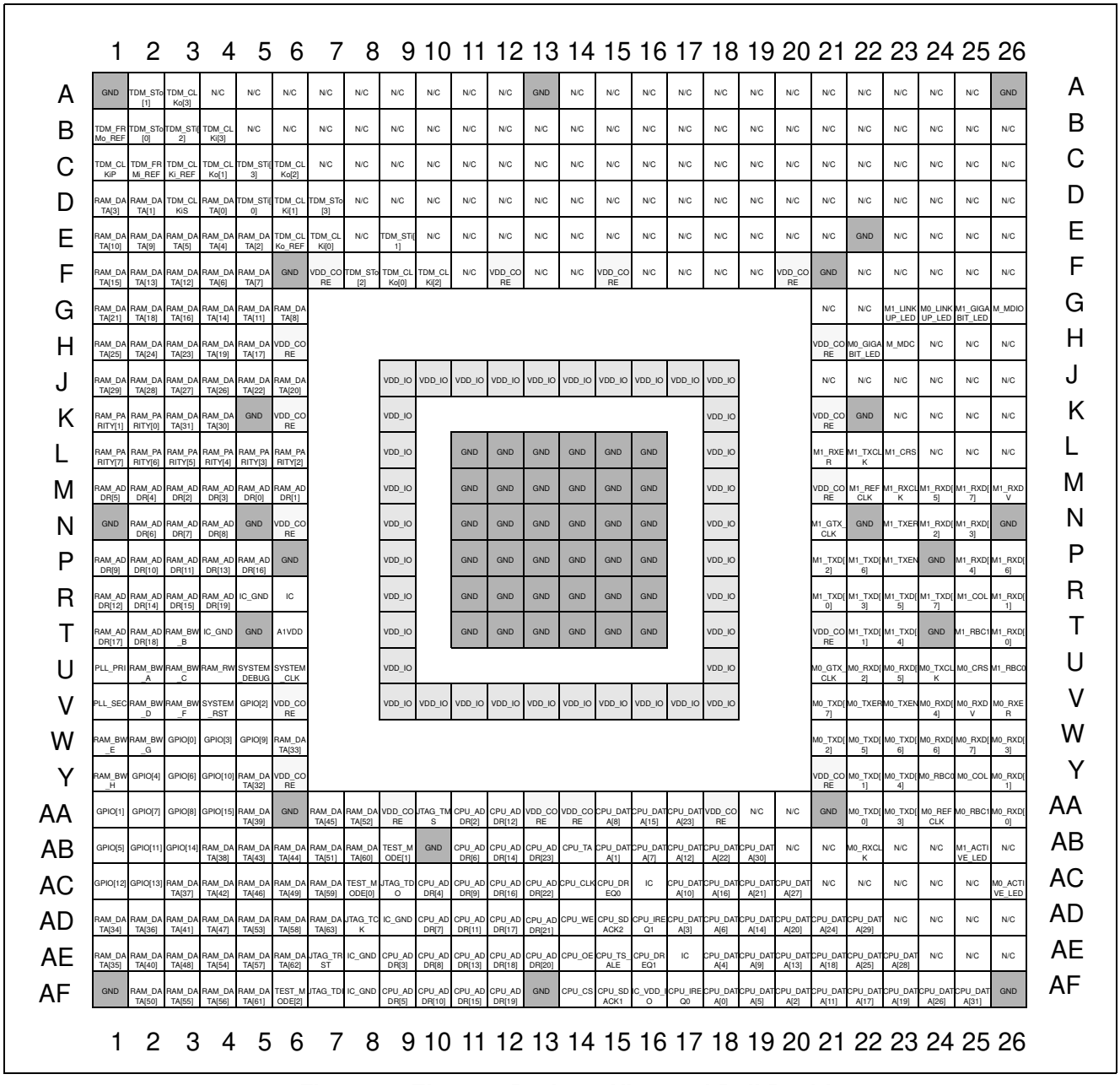
ZL50110 Package view from TOP side. Note that ball A1 is non-chamfered corner.



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	
A	GND	TDM_STo[1]	TDM_CLKo[3]	TDM_STo[4]	TDM_STo[5]	TDM_STi[6]	TDM_STo[7]	TDM_STi[7]	N/C	N/C	N/C	N/C	GND	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	GND	A
B	TDM_FRMo_REF	TDM_STo[0]	TDM_STi[2]	TDM_CLKi[3]	TDM_STi[4]	TDM_CLKo[6]	TDM_STo[6]	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	B
C	TDM_CLKiP	TDM_FRMi_REF	TDM_CLKi_REF	TDM_CLKo[1]	TDM_STi[3]	TDM_CLKo[2]	TDM_CLKi[6]	TDM_CLKi[7]	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	C
D	RAM_DATA[3]	RAM_DATA[1]	TDM_CLKiS	RAM_DATA[0]	TDM_STi[0]	TDM_CLKi[1]	TDM_STo[3]	TDM_STo[5]	TDM_CLKi[5]	TDM_CLKo[7]	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	D
E	RAM_DATA[10]	RAM_DATA[9]	RAM_DATA[5]	RAM_DATA[4]	RAM_DATA[2]	TDM_CLKo_REF	TDM_CLKi[0]	TDM_CLKo[4]	TDM_STi[1]	TDM_CLKi[4]	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	GND	N/C	N/C	N/C	N/C	E
F	RAM_DATA[15]	RAM_DATA[13]	RAM_DATA[12]	RAM_DATA[6]	RAM_DATA[7]	GND	VDD_CORE	TDM_STo[2]	TDM_CLKo[0]	TDM_CLKi[2]	TDM_CLKo[5]	VDD_CORE	N/C	N/C	VDD_CORE	N/C	N/C	N/C	N/C	VDD_CORE	GND	N/C	N/C	N/C	N/C	N/C	F
G	RAM_DATA[21]	RAM_DATA[18]	RAM_DATA[16]	RAM_DATA[14]	RAM_DATA[11]	RAM_DATA[8]															N/C	N/C	M1_LINKUP_LED	M0_LINKUP_LED	M1_GIGABIT_LED	M_MDIO	G
H	RAM_DATA[25]	RAM_DATA[24]	RAM_DATA[23]	RAM_DATA[19]	RAM_DATA[17]	VDD_CORE															VDD_CORE	M0_GIGABIT_LED	M_MDC	N/C	N/C	N/C	H
J	RAM_DATA[29]	RAM_DATA[28]	RAM_DATA[27]	RAM_DATA[26]	RAM_DATA[22]	RAM_DATA[20]			VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO			N/C	N/C	N/C	N/C	N/C	N/C	J
K	RAM_PARITY[1]	RAM_PARITY[0]	RAM_DATA[31]	RAM_DATA[30]	GND	VDD_CORE			VDD_IO									VDD_IO			VDD_CORE	GND	N/C	N/C	N/C	N/C	K
L	RAM_PARITY[7]	RAM_PARITY[6]	RAM_PARITY[5]	RAM_PARITY[4]	RAM_PARITY[3]	RAM_PARITY[2]			VDD_IO		GND	GND	GND	GND	GND	GND		VDD_IO			M1_RXER	M1_TXCLK	M1_CRS	N/C	N/C	N/C	L
M	RAM_ADDR[5]	RAM_ADDR[4]	RAM_ADDR[2]	RAM_ADDR[3]	RAM_ADDR[0]	RAM_ADDR[1]			VDD_IO		GND	GND	GND	GND	GND	GND		VDD_IO			VDD_CORE	M1_REFCLK	M1_RXCLK	M1_RXD[5]	M1_RXD[7]	M1_RXDV	M
N	GND	RAM_ADDR[6]	RAM_ADDR[7]	RAM_ADDR[8]	GND	VDD_CORE			VDD_IO		GND	GND	GND	GND	GND	GND		VDD_IO			M1_GTX_CLK	GND	M1_TXER	M1_RXD[2]	M1_RXD[3]	GND	N
P	RAM_ADDR[9]	RAM_ADDR[10]	RAM_ADDR[11]	RAM_ADDR[13]	RAM_ADDR[16]	GND			VDD_IO		GND	GND	GND	GND	GND	GND		VDD_IO			M1_TXD[2]	M1_TXD[6]	M1_TXEN	GND	M1_RXD[4]	M1_RXD[6]	P
R	RAM_ADDR[12]	RAM_ADDR[14]	RAM_ADDR[15]	RAM_ADDR[19]	IC_GND	IC			VDD_IO		GND	GND	GND	GND	GND	GND		VDD_IO			M1_TXD[0]	M1_TXD[3]	M1_TXD[5]	M1_TXD[7]	M1_COL	M1_RXD[1]	R
T	RAM_ADDR[17]	RAM_ADDR[18]	RAM_BW_B	IC_GND	GND	A1VDD			VDD_IO		GND	GND	GND	GND	GND	GND		VDD_IO			VDD_CORE	M1_TXD[1]	M1_TXD[4]	GND	M1_RBC1	M1_RXD[0]	T
U	PLL_PRI	RAM_BW_A	RAM_BW_C	RAM_RW	SYSTEM_DEBUG	SYSTEM_CLK			VDD_IO									VDD_IO			M0_GTX_CLK	M0_RXD[2]	M0_RXD[5]	M0_TXCLK	M0_CRS	M1_RBC0	U
V	PLL_SEC	RAM_BW_D	RAM_BW_F	SYSTEM_RST	GPIO[2]	VDD_CORE			VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO			M0_TXD[7]	M0_TXER	M0_TXEN	M0_RXD[4]	M0_RXDV	M0_RXER	V
W	RAM_BW_E	RAM_BW_G	GPIO[0]	GPIO[3]	GPIO[9]	RAM_DATA[33]															M0_TXD[2]	M0_TXD[5]	M0_TXD[6]	M0_RXD[6]	M0_RXD[7]	M0_RXD[3]	W
Y	RAM_BW_H	GPIO[4]	GPIO[6]	GPIO[10]	RAM_DATA[32]	VDD_CORE															VDD_CORE	M0_TXD[1]	M0_TXD[4]	M0_RBC0	M0_COL	M0_RXD[1]	Y
AA	GPIO[1]	GPIO[7]	GPIO[8]	GPIO[15]	RAM_DATA[39]	GND	RAM_DATA[45]	RAM_DATA[52]	VDD_CORE	JTAG_TMS	CPU_ADDR[2]	CPU_ADDR[12]	VDD_CORE	VDD_CORE	CPU_DATA[8]	CPU_DATA[15]	CPU_DATA[23]	VDD_CORE	N/C	N/C	GND	M0_TXD[0]	M0_TXD[3]	M0_REFCLK	M0_RBC1	M0_RXD[0]	AA
AB	GPIO[5]	GPIO[11]	GPIO[14]	RAM_DATA[38]	RAM_DATA[43]	RAM_DATA[44]	RAM_DATA[51]	RAM_DATA[60]	TEST_MODE[1]	GND	CPU_ADDR[6]	CPU_ADDR[14]	CPU_ADDR[23]	CPU_TA	CPU_DATA[1]	CPU_DATA[7]	CPU_DATA[12]	CPU_DATA[22]	CPU_DATA[30]	N/C	N/C	M0_RXCLK	N/C	N/C	M1_ACTIVE_LED	N/C	AB
AC	GPIO[12]	GPIO[13]	RAM_DATA[37]	RAM_DATA[42]	RAM_DATA[46]	RAM_DATA[49]	RAM_DATA[59]	TEST_MODE[0]	JTAG_TDO	CPU_ADDR[4]	CPU_ADDR[9]	CPU_ADDR[16]	CPU_ADDR[22]	CPU_CLK	CPU_DREQ0	IC	CPU_DATA[10]	CPU_DATA[16]	CPU_DATA[21]	CPU_DATA[27]	N/C	N/C	N/C	N/C	N/C	M0_ACTIVE_LED	AC
AD	RAM_DATA[34]	RAM_DATA[36]	RAM_DATA[41]	RAM_DATA[47]	RAM_DATA[53]	RAM_DATA[58]	RAM_DATA[63]	JTAG_TCK	IC_GND	CPU_ADDR[7]	CPU_ADDR[11]	CPU_ADDR[17]	CPU_ADDR[21]	CPU_WE	CPU_SDACK2	CPU_IREQ1	CPU_DATA[3]	CPU_DATA[6]	CPU_DATA[14]	CPU_DATA[20]	CPU_DATA[24]	CPU_DATA[29]	N/C	N/C	N/C	N/C	AD
AE	RAM_DATA[35]	RAM_DATA[40]	RAM_DATA[48]	RAM_DATA[54]	RAM_DATA[57]	RAM_DATA[62]	JTAG_TRST	IC_GND	CPU_ADDR[3]	CPU_ADDR[8]	CPU_ADDR[13]	CPU_ADDR[18]	CPU_ADDR[20]	CPU_OE	CPU_TSALE	CPU_DREQ1	IC	CPU_DATA[4]	CPU_DATA[9]	CPU_DATA[13]	CPU_DATA[18]	CPU_DATA[25]	CPU_DATA[28]	N/C	N/C	N/C	AE
AF	GND	RAM_DATA[50]	RAM_DATA[55]	RAM_DATA[56]	RAM_DATA[61]	TEST_MODE[2]	JTAG_TDI	IC_GND	CPU_ADDR[5]	CPU_ADDR[10]	CPU_ADDR[15]	CPU_ADDR[19]	GND	CPU_CS	CPU_SDACK1	IC_VDD_IO	CPU_IREQ0	CPU_DATA[0]	CPU_DATA[5]	CPU_DATA[2]	CPU_DATA[11]	CPU_DATA[17]	CPU_DATA[19]	CPU_DATA[26]	CPU_DATA[31]	GND	AF

Figure 4 - ZL50110 Package View and Ball Positions

ZL50114 Package view from TOP side. Note that ball A1 is non-chamfered corner.



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	
A	GND	TDM_STo[1]	TDM_CLKo[3]	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	GND	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	GND	A
B	TDM_FRMo_REF	TDM_STo[0]	TDM_STi[2]	TDM_CLKi[3]	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	B
C	TDM_CLKiP	TDM_FRMi_REF	TDM_CLKi_REF	TDM_CLKo[1]	TDM_STi[3]	TDM_CLKo[2]	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	C
D	RAM_DATA[3]	RAM_DATA[1]	TDM_CLKiS	RAM_DATA[0]	TDM_STi[0]	TDM_CLKi[1]	TDM_STo[3]	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	D
E	RAM_DATA[10]	RAM_DATA[9]	RAM_DATA[5]	RAM_DATA[4]	RAM_DATA[2]	TDM_CLKo_REF	TDM_CLKi[0]	N/C	TDM_STi[1]	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	GND	N/C	N/C	N/C	N/C	E
F	RAM_DATA[15]	RAM_DATA[13]	RAM_DATA[12]	RAM_DATA[6]	RAM_DATA[7]	GND	VDD_CORE	TDM_STo[2]	TDM_CLKo[0]	TDM_CLKi[2]	N/C	VDD_CORE	N/C	N/C	VDD_CORE	N/C	N/C	N/C	N/C	VDD_CORE	GND	N/C	N/C	N/C	N/C	N/C	F
G	RAM_DATA[21]	RAM_DATA[18]	RAM_DATA[16]	RAM_DATA[14]	RAM_DATA[11]	RAM_DATA[8]															N/C	N/C	M1_LINKUP_LED	M0_LINKUP_LED	M1_GIGABIT_LED	M_MDIO	G
H	RAM_DATA[25]	RAM_DATA[24]	RAM_DATA[23]	RAM_DATA[19]	RAM_DATA[17]	VDD_CORE															VDD_CORE	M0_GIGABIT_LED	M_MDC	N/C	N/C	N/C	H
J	RAM_DATA[29]	RAM_DATA[28]	RAM_DATA[27]	RAM_DATA[26]	RAM_DATA[22]	RAM_DATA[20]			VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO			N/C	N/C	N/C	N/C	N/C	N/C	J
K	RAM_PARITY[1]	RAM_PARITY[0]	RAM_DATA[31]	RAM_DATA[30]	GND	VDD_CORE			VDD_IO									VDD_IO			VDD_CORE	GND	N/C	N/C	N/C	N/C	K
L	RAM_PARITY[7]	RAM_PARITY[6]	RAM_PARITY[5]	RAM_PARITY[4]	RAM_PARITY[3]	RAM_PARITY[2]			VDD_IO		GND	GND	GND	GND	GND	GND		VDD_IO			M1_RXER	M1_TXCLK	M1_CRS	N/C	N/C	N/C	L
M	RAM_ADDR[5]	RAM_ADDR[4]	RAM_ADDR[2]	RAM_ADDR[3]	RAM_ADDR[0]	RAM_ADDR[1]			VDD_IO		GND	GND	GND	GND	GND	GND		VDD_IO			VDD_CORE	M1_REFCLK	M1_RXCLK	M1_RXD[5]	M1_RXD[7]	M1_RXDV	M
N	GND	RAM_ADDR[6]	RAM_ADDR[7]	RAM_ADDR[8]	GND	VDD_CORE			VDD_IO		GND	GND	GND	GND	GND	GND		VDD_IO			M1_GTX_CLK	GND	M1_TXER	M1_RXD[2]	M1_RXD[3]	GND	N
P	RAM_ADDR[9]	RAM_ADDR[10]	RAM_ADDR[11]	RAM_ADDR[13]	RAM_ADDR[16]	GND			VDD_IO		GND	GND	GND	GND	GND	GND		VDD_IO			M1_TXD[2]	M1_TXD[6]	M1_TXEN	GND	M1_RXD[4]	M1_RXD[6]	P
R	RAM_ADDR[12]	RAM_ADDR[14]	RAM_ADDR[15]	RAM_ADDR[19]	IC_GND	IC			VDD_IO		GND	GND	GND	GND	GND	GND		VDD_IO			M1_TXD[0]	M1_TXD[3]	M1_TXD[5]	M1_TXD[7]	M1_COL	M1_RXD[1]	R
T	RAM_ADDR[17]	RAM_ADDR[18]	RAM_BW_B	IC_GND	GND	A1VDD			VDD_IO		GND	GND	GND	GND	GND	GND		VDD_IO			VDD_CORE	M1_TXD[1]	M1_TXD[4]	GND	M1_RBC1	M1_RXD[0]	T
U	PLL_PRI	RAM_BW_A	RAM_BW_C	RAM_RW	SYSTEM_DEBUG	SYSTEM_CLK			VDD_IO									VDD_IO			M0_GTX_CLK	M0_RXD[2]	M0_RXD[5]	M0_TXCLK	M0_CRS	M1_RBC0	U
V	PLL_SEC	RAM_BW_D	RAM_BW_F	SYSTEM_RST	GPIO[2]	VDD_CORE			VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO			M0_TXD[7]	M0_TXER	M0_TXEN	M0_RXD[4]	M0_RXDV	M0_RXER	V
W	RAM_BW_E	RAM_BW_G	GPIO[0]	GPIO[3]	GPIO[9]	RAM_DATA[33]															M0_TXD[2]	M0_TXD[5]	M0_TXD[6]	M0_RXD[6]	M0_RXD[7]	M0_RXD[3]	W
Y	RAM_BW_H	GPIO[4]	GPIO[6]	GPIO[10]	RAM_DATA[32]	VDD_CORE															VDD_CORE	M0_TXD[1]	M0_TXD[4]	M0_RBC0	M0_COL	M0_RXD[1]	Y
AA	GPIO[1]	GPIO[7]	GPIO[8]	GPIO[15]	RAM_DATA[39]	GND	RAM_DATA[45]	RAM_DATA[52]	VDD_CORE	JTAG_TMS	CPU_ADDR[2]	CPU_ADDR[12]	VDD_CORE	VDD_CORE	CPU_DATA[8]	CPU_DATA[15]	CPU_DATA[23]	VDD_CORE	N/C	N/C	GND	M0_TXD[0]	M0_TXD[3]	M0_REFCLK	M0_RBC1	M0_RXD[0]	AA
AB	GPIO[5]	GPIO[11]	GPIO[14]	RAM_DATA[38]	RAM_DATA[43]	RAM_DATA[44]	RAM_DATA[51]	RAM_DATA[60]	TEST_MODE[1]	GND	CPU_ADDR[6]	CPU_ADDR[14]	CPU_ADDR[23]	CPU_TA	CPU_DATA[1]	CPU_DATA[7]	CPU_DATA[12]	CPU_DATA[22]	CPU_DATA[30]	N/C	N/C	M0_RXCLK	N/C	N/C	M1_ACTIVE_LED	N/C	AB
AC	GPIO[12]	GPIO[13]	RAM_DATA[37]	RAM_DATA[42]	RAM_DATA[46]	RAM_DATA[49]	RAM_DATA[59]	TEST_MODE[0]	JTAG_TDO	CPU_ADDR[4]	CPU_ADDR[9]	CPU_ADDR[16]	CPU_ADDR[22]	CPU_CLK	CPU_DREQ0	IC	CPU_DATA[10]	CPU_DATA[16]	CPU_DATA[21]	CPU_DATA[27]	N/C	N/C	N/C	N/C	N/C	M0_ACTIVE_LED	AC
AD	RAM_DATA[34]	RAM_DATA[36]	RAM_DATA[41]	RAM_DATA[47]	RAM_DATA[53]	RAM_DATA[58]	RAM_DATA[63]	JTAG_TCK	IC_GND	CPU_ADDR[7]	CPU_ADDR[11]	CPU_ADDR[17]	CPU_ADDR[21]	CPU_WE	CPU_SDACK2	CPU_IREQ1	CPU_DATA[3]	CPU_DATA[6]	CPU_DATA[14]	CPU_DATA[20]	CPU_DATA[24]	CPU_DATA[29]	N/C	N/C	N/C	N/C	AD
AE	RAM_DATA[35]	RAM_DATA[40]	RAM_DATA[48]	RAM_DATA[54]	RAM_DATA[57]	RAM_DATA[62]	JTAG_TRST	IC_GND	CPU_ADDR[3]	CPU_ADDR[8]	CPU_ADDR[13]	CPU_ADDR[18]	CPU_ADDR[20]	CPU_OE	CPU_TSALE	CPU_DREQ1	IC	CPU_DATA[4]	CPU_DATA[9]	CPU_DATA[13]	CPU_DATA[18]	CPU_DATA[25]	CPU_DATA[28]	N/C	N/C	N/C	AE
AF	GND	RAM_DATA[50]	RAM_DATA[55]	RAM_DATA[56]	RAM_DATA[61]	TEST_MODE[2]	JTAG_TDI	IC_GND	CPU_ADDR[5]	CPU_ADDR[10]	CPU_ADDR[15]	CPU_ADDR[19]	GND	CPU_CS	CPU_SDACK1	IC_VDD_IO	CPU_IREQ0	CPU_DATA[0]	CPU_DATA[5]	CPU_DATA[2]	CPU_DATA[11]	CPU_DATA[17]	CPU_DATA[19]	CPU_DATA[26]	CPU_DATA[31]	GND	AF
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	

Figure 5 - ZL50114 Package View and Ball Positions

Ball Signal Assignment

Ball Number	Signal Name
A1	GND
A2	TDM_STo[1]
A3	TDM_CLKo[3]
A4‡	TDM_STo[4]
A5‡	TDM_STo[5]
A6‡	TDM_STi[6]
A7‡	TDM_STo[7]
A8‡	TDM_STi[7]
A9†	TDM_CLKo[10]
A10†	TDM_CLKi[10]
A11†	TDM_CLKi[11]
A12†	TDM_CLKo[13]
A13	GND
A14†	TDM_STo[13]
A15†	TDM_STo[14]
A16†	TDM_CLKo[15]
A17*	TDM_STo[16]
A18†*	TDM_CLKo[18]
A19*	TDM_STi[18]
A20*	TDM_CLKi[20]
A21*	TDM_STi[20]
A22*	TDM_STo[21]
A23*	TDM_STi[21]
A24*	TDM_CLKo[24]
A25*	TDM_CLKo[25]
A26	GND
B1	TDM_FRMo_REF
B2	TDM_STo[0]
B3	TDM_STi[2]
B4	TDM_CLKi[3]
B5‡	TDM_STi[4]
B6‡	TDM_CLKo[6]
B7‡	TDM_STo[6]
B8†	TDM_CLKo[8]
B9†	TDM_CLKi[9]
B10†	TDM_STo[10]
B11†	TDM_STi[10]
B12†	TDM_CLKi[12]
B13†	TDM_STo[12]
B14†	TDM_STi[13]
B15†	TDM_CLKi[15]
B16†	TDM_STi[15]
B17*	TDM_STi[17]
B18†*	TDM_CLKi[18]
B19*	TDM_CLKo[20]
B20*	TDM_STo[19]
B21*	TDM_STo[22]
B22*	TDM_CLKo[23]
B23*	TDM_STo[24]
B24*	TDM_CLKo[26]
B25*	TDM_STi[24]
B26*	TDM_CLKo[27]
C1	TDM_CLKiP
C2	TDM_FRMi_REF
C3	TDM_CLKi_REF
C4	TDM_CLKo[1]
C5	TDM_STi[3]
C6	TDM_CLKo[2]
C7‡	TDM_CLKi[6]
C8‡	TDM_CLKi[7]
C9†	TDM_CLKo[9]
C10†	TDM_STo[9]
C11†	TDM_STi[9]
C12†	TDM_STi[11]
C13†	TDM_CLKi[13]
C14†	TDM_CLKo[14]
C15*	TDM_CLKo[16]
C16*	TDM_STi[16]
C17*	TDM_CLKo[17]
C18*	TDM_STi[19]
C19*	TDM_CLKo[21]
C20*	TDM_CLKi[21]
C21*	TDM_CLKi[24]
C22*	TDM_STi[22]
C23*	TDM_STo[26]
C24*	TDM_CLKi[27]
C25*	TDM_STi[27]
C26*	TDM_STi[28]
D1	RAM_DATA[3]
D2	RAM_DATA[1]
D3	TDM_CLKiS
D4	RAM_DATA[0]
D5	TDM_STi[0]
D6	TDM_CLKi[1]
D7	TDM_STo[3]
D8‡	TDM_STi[5]
D9‡	TDM_CLKi[5]
D10‡	TDM_CLKo[7]
D11†	TDM_STi[8]
D12†	TDM_CLKo[11]
D13†	TDM_STi[12]
D14†	TDM_STi[14]
D15†*	TDM_CLKi[16]
D16†	TDM_CLKo[19]
D17*	TDM_STo[18]
D18*	TDM_STo[20]
D19*	TDM_CLKo[22]
D20*	TDM_STo[27]
D21*	TDM_STo[25]
D22*	TDM_CLKi[26]
D23*	TDM_CLKo[28]
D24*	TDM_CLKi[29]
D25*	TDM_STi[29]
D26*	TDM_STi[31]
E1	RAM_DATA[10]
E2	RAM_DATA[9]
E3	RAM_DATA[5]
E4	RAM_DATA[4]
E5	RAM_DATA[2]
E6	TDM_CLKo_REF
E7	TDM_CLKi[0]
E8‡	TDM_CLKo[4]
E9	TDM_STi[1]

Ball Number	Signal Name
E10‡	TDM_CLKi[4]
E11†	TDM_STo[8]
E12†	TDM_CLKi[8]
E13†	TDM_CLKo[12]
E14†	TDM_STo[15]
E15*	TDM_CLKi[17]
E16*	TDM_CLKi[19]
E17*	TDM_STo[23]
E18*	TDM_STi[23]
E19*	TDM_CLKi[25]
E20*	TDM_STi[26]
E21*	TDM_CLKi[28]
E22	GND
E23*	TDM_CLKo[30]
E24*	TDM_CLKi[30]
E25*	TDM_STi[30]
E26†*	TDM_STo[29]
F1	RAM_DATA[15]
F2	RAM_DATA[13]
F3	RAM_DATA[12]
F4	RAM_DATA[6]
F5	RAM_DATA[7]
F6	GND
F7	VDD_CORE
F8	TDM_STo[2]
F9	TDM_CLKo[0]
F10	TDM_CLKi[2]
F11‡	TDM_CLKo[5]
F12	VDD_CORE
F13†	TDM_STo[11]
F14†	TDM_CLKi[14]
F15	VDD_CORE
F16*	TDM_STo[17]
F17*	TDM_CLKi[22]
F18*	TDM_STi[25]
F19*	TDM_CLKi[23]
F20	VDD_CORE
F21	GND

Ball Number	Signal Name
F22*	TDM_CLKi[31]
F23*	TDM_CLKo[29]
F24*	TDM_STo[28]
F25*	TDM_CLKo[31]
F26†	M1_LINKUP_LED
G1	RAM_DATA[21]
G2	RAM_DATA[18]
G3	RAM_DATA[16]
G4	RAM_DATA[14]
G5	RAM_DATA[11]
G6	RAM_DATA[8]
G21*	TDM_STo[31]
G22*	TDM_STo[30]
G23	M1/2_LINKUP_LED
G24	M0/3_LINKUP_LED
G25	M1_GIGABIT_LED
G26	M_MDIO
H1	RAM_DATA[25]
H2	RAM_DATA[24]
H3	RAM_DATA[23]
H4	RAM_DATA[19]
H5	RAM_DATA[17]
H6	VDD_CORE
H21	VDD_CORE
H22	M0_GIGABIT_LED
H23	M_MDC
H24*	M3_CRS
H25*	M3_TXCLK
H26*	M3_RXER
J1	RAM_DATA[29]
J2	RAM_DATA[28]
J3	RAM_DATA[27]
J4	RAM_DATA[26]
J5	RAM_DATA[22]
J6	RAM_DATA[20]
J9	VDD_IO
J10	VDD_IO
J11	VDD_IO

Ball Number	Signal Name
J12	VDD_IO
J13	VDD_IO
J14	VDD_IO
J15	VDD_IO
J16	VDD_IO
J17	VDD_IO
J18	VDD_IO
J21*	M3_RXDV
J22*	M3_RXD[3]
J23*	M3_RXD[2]
J24*	M3_RXD[1]
J25*	M3_RXD[0]
J26*	M3_COL
K1	RAM_PARITY[1]
K2	RAM_PARITY[0]
K3	RAM_DATA[31]
K4	RAM_DATA[30]
K5	GND
K6	VDD_CORE
K9	VDD_IO
K18	VDD_IO
K21	VDD_CORE
K22	GND
K23*	M3_TXD[3]
K24*	M3_TXEN
K25*	M3_TXER
K26*	M3_RXCLK
L1	RAM_PARITY[7]
L2	RAM_PARITY[6]
L3	RAM_PARITY[5]
L4	RAM_PARITY[4]
L5	RAM_PARITY[3]
L6	RAM_PARITY[2]
L9	VDD_IO
L11	GND
L12	GND
L13	GND
L14	GND

Ball Number	Signal Name
L15	GND
L16	GND
L18	VDD_IO
L21	M1_RXER
L22	M1_TXCLK
L23	M1_CRS
L24*	M3_TXD[0]
L25*	M3_TXD[1]
L26*	M3_TXD[2]
M1	RAM_ADDR[5]
M2	RAM_ADDR[4]
M3	RAM_ADDR[2]
M4	RAM_ADDR[3]
M5	RAM_ADDR[0]
M6	RAM_ADDR[1]
M9	VDD_IO
M11	GND
M12	GND
M13	GND
M14	GND
M15	GND
M16	GND
M18	VDD_IO
M21	VDD_CORE
M22	M1_REFCLK
M23	M1_RXCLK
M24	M1_RXD[5]
M25	M1_RXD[7]
M26	M1_RXDV
N1	GND
N2	RAM_ADDR[6]
N3	RAM_ADDR[7]
N4	RAM_ADDR[8]
N5	GND
N6	VDD_CORE
N9	VDD_IO
N11	GND
N12	GND

Ball Number	Signal Name
N13	GND
N14	GND
N15	GND
N16	GND
N18	VDD_IO
N21	M1_GTX_CLK
N22	GND
N23	M1_TXER
N24	M1_RXD[2]
N25	M1_RXD[3]
N26	GND
P1	RAM_ADDR[9]
P2	RAM_ADDR[10]
P3	RAM_ADDR[11]
P4	RAM_ADDR[13]
P5	RAM_ADDR[16]
P6	GND
P9	VDD_IO
P11	GND
P12	GND
P13	GND
P14	GND
P15	GND
P16	GND
P18	VDD_IO
P21	M1_TXD[2]
P22	M1_TXD[6]
P23	M1_TXEN
P24	GND
P25	M1_RXD[4]
P26	M1_RXD[6]
R1	RAM_ADDR[12]
R2	RAM_ADDR[14]
R3	RAM_ADDR[15]
R4	RAM_ADDR[19]
R5	IC_GND
R6	IC
R9	VDD_IO

Ball Number	Signal Name
R11	GND
R12	GND
R13	GND
R14	GND
R15	GND
R16	GND
R18	VDD_IO
R21	M1_TXD[0]
R22	M1_TXD[3]
R23	M1_TXD[5]
R24	M1_TXD[7]
R25	M1_COL
R26	M1_RXD[1]
T1	RAM_ADDR[17]
T2	RAM_ADDR[18]
T3	RAM_BW_B
T4	IC_GND
T5	GND
T6	A1VDD
T9	VDD_IO
T11	GND
T12	GND
T13	GND
T14	GND
T15	GND
T16	GND
T18	VDD_IO
T21	VDD_CORE
T22	M1_TXD[1]
T23	M1_TXD[4]
T24	GND
T25	M1_RBC1
T26	M1_RXD[0]
U1	PLL_PRI
U2	RAM_BW_A
U3	RAM_BW_C
U4	RAM_RW
U5	SYSTEM_DEBUG

Ball Number	Signal Name
U6	SYSTEM_CLK
U9	VDD_IO
U18	VDD_IO
U21	M0_GTX_CLK
U22	M0_RXD[2]
U23	M0_RXD[5]
U24	M0_TXCLK
U25	M0_CRS
U26	M1_RBC0
V1	PLL_SEC
V2	RAM_BW_D
V3	RAM_BW_F
V4	SYSTEM_RST
V5	GPIO[2]
V6	VDD_CORE
V9	VDD_IO
V10	VDD_IO
V11	VDD_IO
V12	VDD_IO
V13	VDD_IO
V14	VDD_IO
V15	VDD_IO
V16	VDD_IO
V17	VDD_IO
V18	VDD_IO
V21	M0_TXD[7]
V22	M0_TXER
V23	M0_TXEN
V24	M0_RXD[4]
V25	M0_RXDV
V26	M0_RXER
W1	RAM_BW_E
W2	RAM_BW_G
W3	GPIO[0]
W4	GPIO[3]
W5	GPIO[9]
W6	RAM_DATA[33]
W21	M0_TXD[2]

Ball Number	Signal Name
W22	M0_TXD[5]
W23	M0_TXD[6]
W24	M0_RXD[6]
W25	M0_RXD[7]
W26	M0_RXD[3]
Y1	RAM_BW_H
Y2	GPIO[4]
Y3	GPIO[6]
Y4	GPIO[10]
Y5	RAM_DATA[32]
Y6	VDD_CORE
Y21	VDD_CORE
Y22	M0_TXD[1]
Y23	M0_TXD[4]
Y24	M0_RBC0
Y25	M0_COL
Y26	M0_RXD[1]
AA1	GPIO[1]
AA2	GPIO[7]
AA3	GPIO[8]
AA4	GPIO[15]
AA5	RAM_DATA[39]
AA6	GND
AA7	RAM_DATA[45]
AA8	RAM_DATA[52]
AA9	VDD_CORE
AA10	JTAG_TMS
AA11	CPU_ADDR[2]
AA12	CPU_ADDR[12]
AA13	VDD_CORE
AA14	VDD_CORE
AA15	CPU_DATA[8]
AA16	CPU_DATA[15]
AA17	CPU_DATA[23]
AA18	VDD_CORE
AA19†	M2_RXCLK
AA20†	M2_RXDV
AA21	GND

Ball Number	Signal Name
AA22	M0_TXD[0]
AA23	M0_TXD[3]
AA24	M0_REFCLK
AA25	M0_RBC1
AA26	M0_RXD[0]
AB1	GPIO[5]
AB2	GPIO[11]
AB3	GPIO[14]
AB4	RAM_DATA[38]
AB5	RAM_DATA[43]
AB6	RAM_DATA[44]
AB7	RAM_DATA[51]
AB8	RAM_DATA[60]
AB9	TEST_MODE[1]
AB10	GND
AB11	CPU_ADDR[6]
AB12	CPU_ADDR[14]
AB13	CPU_ADDR[23]
AB14	CPU_TA
AB15	CPU_DATA[1]
AB16	CPU_DATA[7]
AB17	CPU_DATA[12]
AB18	CPU_DATA[22]
AB19	CPU_DATA[30]
AB20†	M2_TXER
AB21†	M2_RXD[1]
AB22	M0_RXCLK
AB23†	M0_LINKUP_LED
AB24†	M2_ACTIVE_LED
AB25	M1_ACTIVE_LED
AB26*	M3_ACTIVE_LED
AC1	GPIO[12]
AC2	GPIO[13]
AC3	RAM_DATA[37]
AC4	RAM_DATA[42]
AC5	RAM_DATA[46]
AC6	RAM_DATA[49]
AC7	RAM_DATA[59]

Ball Number	Signal Name
AC8	TEST_MODE[0]
AC9	JTAG_TDO
AC10	CPU_ADDR[4]
AC11	CPU_ADDR[9]
AC12	CPU_ADDR[16]
AC13	CPU_ADDR[22]
AC14	CPU_CLK
AC15	CPU_DREQ0
AC16	IC
AC17	CPU_DATA[10]
AC18	CPU_DATA[16]
AC19	CPU_DATA[21]
AC20	CPU_DATA[27]
AC21†	M2_TXD[1]
AC22†	M2_TXEN
AC23†	M2_RXD[2]
AC24†	M2_RXER
AC25†	M2_CRS
AC26	M0_ACTIVE_LED
AD1	RAM_DATA[34]
AD2	RAM_DATA[36]
AD3	RAM_DATA[41]
AD4	RAM_DATA[47]
AD5	RAM_DATA[53]
AD6	RAM_DATA[58]
AD7	RAM_DATA[63]
AD8	JTAG_TCK
AD9	IC_GND
AD10	CPU_ADDR[7]
AD11	CPU_ADDR[11]
AD12	CPU_ADDR[17]
AD13	CPU_ADDR[21]
AD14	CPU_WE
AD15	CPU_SDACK2
AD16	CPU_IREQ1
AD17	CPU_DATA[3]
AD18	CPU_DATA[6]
AD19	CPU_DATA[14]

Ball Number	Signal Name
AD20	CPU_DATA[20]
AD21	CPU_DATA[24]
AD22	CPU_DATA[29]
AD23†	M2_TXD[2]
AD24†	M2_RXD[0]
AD25†	M2_RXD[3]
AD26†	M2_TXCLK
AE1	RAM_DATA[35]
AE2	RAM_DATA[40]
AE3	RAM_DATA[48]
AE4	RAM_DATA[54]
AE5	RAM_DATA[57]
AE6	RAM_DATA[62]
AE7	JTAG_TRST
AE8	IC_GND
AE9	CPU_ADDR[3]
AE10	CPU_ADDR[8]
AE11	CPU_ADDR[13]
AE12	CPU_ADDR[18]
AE13	CPU_ADDR[20]
AE14	CPU_OE
AE15	CPU_TS_ALE
AE16	CPU_DREQ1
AE17	IC
AE18	CPU_DATA[4]
AE19	CPU_DATA[9]
AE20	CPU_DATA[13]
AE21	CPU_DATA[18]
AE22	CPU_DATA[25]
AE23	CPU_DATA[28]
AE24†	M2_TXD[0]
AE25†	M2_TXD[3]
AE26†	M2_COL
AF1	GND
AF2	RAM_DATA[50]
AF3	RAM_DATA[55]
AF4	RAM_DATA[56]
AF5	RAM_DATA[61]

Ball Number	Signal Name
AF6	TEST_MODE[2]
AF7	JTAG_TDI
AF8	IC_GND
AF9	CPU_ADDR[5]
AF10	CPU_ADDR[10]
AF11	CPU_ADDR[15]
AF12	CPU_ADDR[19]
AF13	GND
AF14	CPU_CS
AF15	CPU_SDACK1
AF16	IC_VDD_IO
AF17	CPU_IREQ0
AF18	CPU_DATA[0]
AF19	CPU_DATA[5]
AF20	CPU_DATA[2]
AF21	CPU_DATA[11]
AF22	CPU_DATA[17]
AF23	CPU_DATA[19]
AF24	CPU_DATA[26]
AF25	CPU_DATA[31]
AF26	GND

* Not connected on ZL50112, ZL50110 and ZL50114 - leave open circuit.

† Not Connected on ZL50110 and ZL50114 - leave open circuit.

‡ Not Connected on ZL50114 - leave open circuit.

N/C - Not Connected - leave open circuit.

* Internally Connected on ZL50112 - leave open circuit.

IC - Internally Connected - leave open circuit.

IC_GND - tie to ground

IC_VDD_IO - tie to VDD_IO

3.0 External Interface Description

The following key applies to all tables:

I	Input
O	Output
D	Internal 100 kΩ pull-down resistor present
U	Internal 100 kΩ pull-up resistor present
T	Tri-state Output

3.1 TDM Interface

All TDM Interface signals are 5 V tolerant.

All TDM Interface inputs (including data, clock and frame pulse) have internal pull-down resistors so they can be safely left unconnected if not used.

3.1.1 ZL50111 Variant TDM Stream Connection

Signal	I/O	Package Balls				Description
TDM_STi[31:0]	I D	[31]	D26	[15]	B16	TDM port serial data input streams. For different standards these pins are given different identities: ST-BUS: TDM_STi[31:0] H.110: TDM_D[31:0] H-MVIP: TDM_HDS[31:0] Triggered on rising edge or falling edge depending on standard. At 8.192 Mbps only streams [7:0] are used, with 128 channels per stream. Streams [7:0] are used for J2, and streams [1:0] are used for T3 and E3.
		[30]	E25	[14]	D14	
		[29]	D25	[13]	B14	
		[28]	C26	[12]	D13	
		[27]	C25	[11]	C12	
		[26]	E20	[10]	B11	
		[25]	F18	[9]	C11	
		[24]	B25	[8]	D11	
		[23]	E18	[7]	A8	
		[22]	C22	[6]	A6	
		[21]	A23	[5]	D8	
		[20]	A21	[4]	B5	
		[19]	C18	[3]	C5	
		[18]	A19	[2]	B3	
		[17]	B17	[1]	E9	
		[16]	C16	[0]	D5	

Table 2 - TDM Interface ZL50111 Stream Pin Definition

Signal	I/O	Package Balls				Description
TDM_STo[31:0]	OT	[31]	G21	[15]	E14	TDM port serial data output streams. For different standards these pins are given different identities: ST-BUS: TDM_STo[31:0] H.110: TDM_D[31:0] H-MVIP: TDM_HDS[31:0] Triggered on rising edge or falling edge depending on standard. At 8.192 Mbps only streams [7:0] are used, with 128 channels per stream. Streams [7:0] are used for J2, and streams [1:0] are used for T3 and E3.
		[30]	G22	[14]	A15	
		[29]	E26	[13]	A14	
		[28]	F24	[12]	B13	
		[27]	D20	[11]	F13	
		[26]	C23	[10]	B10	
		[25]	D21	[9]	C10	
		[24]	B23	[8]	E11	
		[23]	E17	[7]	A7	
		[22]	B21	[6]	B7	
		[21]	A22	[5]	A5	
		[20]	D18	[4]	A4	
		[19]	B20	[3]	D7	
		[18]	D17	[2]	F8	
		[17]	F16	[1]	A2	
		[16]	A17	[0]	B2	
TDM_CLKi[31:0]	I D	[31]	F22	[15]	B15	TDM port clock inputs. Programmable as active high or low. Can accept frequencies of 1.544 MHz, 2.048 MHz, 4.096 MHz, 6.312 MHz, 8.192 MHz, 16.384 MHz, 34.368 MHz or 44.736 MHz depending on standard used. At 8.192 Mbps only streams [7:0] are used. Streams [7:0] are used for J2, and streams [1:0] are used for T3 and E3.
		[30]	E24	[14]	F14	
		[29]	D24	[13]	C13	
		[28]	E21	[12]	B12	
		[27]	C24	[11]	A11	
		[26]	D22	[10]	A10	
		[25]	E19	[9]	B9	
		[24]	C21	[8]	E12	
		[23]	F19	[7]	C8	
		[22]	F17	[6]	C7	
		[21]	C20	[5]	D9	
		[20]	A20	[4]	E10	
		[19]	E16	[3]	B4	
		[18]	B18	[2]	F10	
		[17]	E15	[1]	D6	
		[16]	D15	[0]	E7	

Table 2 - TDM Interface ZL50111 Stream Pin Definition (continued)