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ZL50115/16/17/18/19/20

32, 64 and 128 Channel CESoP Processors

Data Sheet

October 2009

Features

General

- Circuit Emulation Services over Packet (CESoP) transport for MPLS, IP and Ethernet networks
- On chip timing & synchronization recovery across a packet network
- On chip dual reference Stratum 4 DPLL (Stratum 3 Holdover accuracy)
- Grooming capability for Nx64 Kbps trunking
- Fully compatible with Zarlink's ZL50110, ZL50111, ZL50112 and ZL50114 CESoP processors

Circuit Emulation Services

- Supports ITU-T recommendation Y.1413 and Y.1453
- Supports IETF RFC4553 and RFC5086
- Supports MEF8 and MFA 8.0.0
- Structured, synchronous CESoP with clock recovery
- Unstructured, asynchronous CESoP, with integral per stream clock recovery

Ordering Information

ZL50115GAG	324 Ball PBGA	trays, bake & dry pack
ZL50116GAG	324 Ball PBGA	trays, bake & dry pack
ZL50117GAG	324 Ball PBGA	trays, bake & dry pack
ZL50118GAG	324 Ball PBGA	trays, bake & dry pack
ZL50119GAG	324 Ball PBGA	trays, bake & dry pack
ZL50120GAG	324 Ball PBGA	trays, bake & dry pack
ZL50115GAG2	324 Ball PBGA**	trays, bake & dry pack
ZL50116GAG2	324 Ball PBGA**	trays, bake & dry pack
ZL50117GAG2	324 Ball PBGA**	trays, bake & dry pack
ZL50118GAG2	324 Ball PBGA**	trays, bake & dry pack
ZL50119GAG2	324 Ball PBGA**	trays, bake & dry pack
ZL50120GAG2	324 Ball PBGA**	trays, bake & dry pack

**Pb Free Tin/Silver/Copper

-40°C to +85°C

Customer Side TDM Interfaces

- Up to 4 T1/E1, 1 J2 or 1 T3/E3 ports
- H.110, H-MVIP, ST-BUS backplane
- Up to 128 bi-directional 64 Kbps channels
- Direct connection to LIUs, framers, backplanes

Customer Side Packet Interfaces

- 100 Mbps MII Fast Ethernet (ZL50118/19/20 only)

(may also be used as a second provider side packet interface)

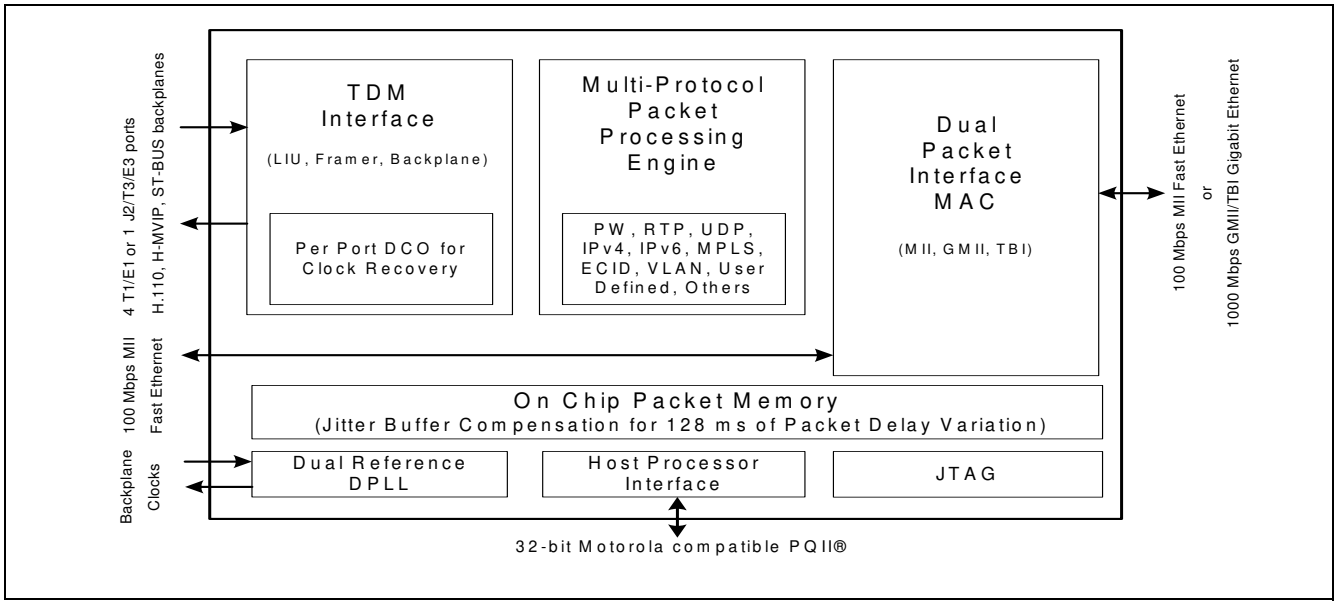

Figure 1 - ZL50115/16/17/18/19/20 High Level Overview

Provider Side Packet Interfaces

- 100 Mbps MII Fast Ethernet or 1000 Mbps GMII/TBI Gigabit Ethernet

System Interfaces

- Flexible 32 bit Motorola host interface
- On-chip packet memory with jitter buffer compensation for over 128 ms of packet delay variation

Packet Processing Functions

- Flexible, multi-protocol packet encapsulation including IPv4, IPv6, RTP, MPLS, L2TPv3, ITU-T Y.1413, IETF CESoPSN, IETF SAToP and user programmable
- Packet re-sequencing to allow lost packet detection and re-ordering
- Four classes of service with programmable priority mechanisms (WFQ and SP) using egress queues
- Programmable classification of incoming packets at layers 2 through 5
- Wire speed processing of all packets regardless of classification providing low latency
- Supports up to 128 separate CESoP connections across the Packet Switched Network

Applications

- Circuit Emulation Services over Packet Networks
  - Leased Line support over packet networks
  - TDM over Cable
  - TDM over WiFi (802.11x)
  - TDM over WiMAX (802.16)
  - Fibre To The Premises G/E-PON
  - Layer 2 VPN services
- Customer-premise and Provider Edge Routers and Switches
- Ethernet and IP based IADs

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1.0 Change Summary

The following table captures the changes from the March 2009 issue.

Page	Item	Change
1	MEF logo	Added MEF logo to show MEF 18 certification.

The following table captures the changes from the May 2008 issue.

Page	Item	Change
50	Section 6.3	Replaced ZLAN-143 with ZL5011x Design Manual section “3.6 System Clock Block”.
52 & 55	Section 6.5 and Section 6.8	Replaced ZLAN-202 with ZL5011x Design Manual section “13.1 Understanding forceDelete”.
60	Section 8.4	Replaced ZLAN-159 with ZL5011x Design Manual section “3.1.1 Connection to LIU.
81	Section 12.6.5	Replaced ZLAN-239 with ZL5011x Design Manual section "7.1.3.1 TBI Interface Timing"
92	Section 15.1	Removed reference to IETF PWE3 draft-ietf-l2tpext-l2tp-base-02”

The following table captures the changes from the February 2006 issue.

Page	Item	Change
1, 2 and 11	Standard	Updated IETF RFC number and standards in general
1, 51,62, 63 and 66	Stratum 3 DPLL	Updated the description for Stratum 3 DPLL
1,10, 11, 27, 28 and 49	STS-1 stream	Remove STS-1 stream
31	Section 4.3	Include more detailed description for the packet interface
49	Section 6	Add a note about jumbo packets
50	Section 6.4	Include a paragraph to clarify the support for structure and unstructure modes at the same time
53	Section 6.5	Include more detailed description for the Payload Assembly
55	Section 6.5.2	Add a note at the end of the section
56	Section 6.9	Include more detailed description for the TDM formatter
57	Section 7	Include more detailed description for Clock Recovery
57	Section 7.1	Include more detailed description for Differential Clock Recovery
58	Section 7.2	Updated the description of Adaptive Clock Recovery
60	Section 8.5	Update Power Up Sequence
80	Section 12.6.3	Updated values for t_{DV}, t_{EV} and t_{ER} in Table 32

Page	Item	Change
82	Section 12.6.5	Updated TXD[9:0] output delay
83	Section 12.6.6	Updated Section 12.6.6 Management Interface Timing (M_MDIO hold time and Figure 39)
85	CPU_$\overline{TS}$_ALE and $\overline{CPU\_TA}$	Added mode details in Figure 40 and Figure 41 Added the $\overline{CPU\_TA}$ assertion time

The following table captures the changes from the July 2005 issue.

Page	Item	Change
39, 40	Section 4.5 and Section 4.6.2	Added external pull-up/pull-down resistor recommendations for SYSTEM_RST, SYSTEM_DEBUG, JTAG_TRST, JTAG_TCK.

The following table captures the changes from the April 2005 issue.

Page	Item	Change
50	Section 6.3	Added Section 6.3 SYSTEM_CLK Considerations.

The following table captures the changes from the January 2005 issue.

Page	Item	Change
		Clarified data sheet to indicate ZL5011x supports clock recovery in both synchronous and asynchronous modes of operation.
85	Figure 42	Inverted polarity of $\overline{CPU\_DREQ0}$ and $\overline{CPU\_DREQ1}$ to conform with default MPC8260. Polarity of $\overline{CPU\_DREQ}$ and $\overline{CPU\_SDACK}$ remains programmable through API.
85	Figure 43	Inverted polarity of $\overline{CPU\_DREQ0}$ and $\overline{CPU\_DREQ1}$ to conform with default MPC8260. Polarity of $\overline{CPU\_DREQ}$ and $\overline{CPU\_SDACK}$ remains programmable through API.

The following table captures the changes from the November 2004 issue.

Page	Item	Change
39	Section 4.6.1	Added 5 kohm pulldown recommendation to GPIO signals.

2.0 Device Line Up

There are six products within the ZL5011x family, with capacities as shown in Table 1.

Product Number	TDM Interface	Provider Side Packet Interface	Customer Side Packet Interface
ZL50115	1 T1 or 1 E1 stream or 1 MVIP/ST-BUS stream at 2.048 Mbps or 1 H.110/H-MVIP/ST-BUS streams at 8.192 Mbps (Maximum of 32 DS0 or Nx64 kbps channels)	100 Mbps MII or 1000 Mbps GMII/TBI	None
ZL50116	2 T1 or 2 E1 streams or 2 MVIP/ST-BUS streams at 2.048 Mbps or 1 H.110/H-MVIP/ST-BUS streams at 8.192 Mbps (Maximum of 64 DS0 or Nx64 kbps channels)	100 Mbps MII or 1000 Mbps GMII/TBI	None
ZL50117	4 T1 or 4 E1 streams or 1 J2, 1 T3 or 1 E3 or 4 MVIP/ST-BUS streams at 2.048 Mbps or 1 H.110/H-MVIP/ST-BUS streams at 8.192 Mbps	100 Mbps MII or 1000 Mbps GMII/TBI	None
ZL50118	1 T1 or 1 E1 stream or 1 MVIP/ST-BUS stream at 2.048 Mbps or 1 H.110/H-MVIP/ST-BUS streams at 8.192 Mbps (Maximum of 32 DS0 or Nx64 kbps channels)	100 Mbps MII or 1000 Mbps GMII/TBI	100 Mbps MII
ZL50119	2 T1 or 2 E1 streams or 2 MVIP/ST-BUS streams at 2.048 Mbps or 1 H.110/H-MVIP/ST-BUS streams at 8.192 Mbps (Maximum of 64 DS0 or Nx64 kbps channels)	100 Mbps MII or 1000 Mbps GMII/TBI	100 Mbps MII
ZL50120	4 T1 or 4 E1 streams or 1 J2, 1 T3 or 1 E3 or 4 MVIP/ST-BUS streams at 2.048 Mbps or 1 H.110/H-MVIP/ST-BUS streams at 8.192 Mbps	100 Mbps MII or 1000 Mbps GMII/TBI	100 Mbps MII

Table 1 - Capacity of Devices in the ZL50115/16/17/18/19/20 Family

2.0 Description

The ZL5011x family (ZL50115, ZL50116, ZL50117, ZL50118, ZL50119, ZL50120) of CESoP processors are highly functional TDM to Packet bridging devices. The ZL5011x provides both structured and unstructured circuit emulation services (CESoP) for T1 and E1 streams across a packet network based on MPLS, IP or Ethernet. The ZL50117/20 also supports unstructured J2, T3 and E3.

The circuit emulation features in the ZL5011x supports the ITU Recommendation Y.1413 and Y.1453, as well as the CESoP standards from the Metro Ethernet Forum (MEF) and the MPLS and Frame Relay Alliance. The ZL5011x also supports IETF RFC4553 and RFC5086.

The ZL50118/19/20 provides a customer side 100 Mbps MII port to aggregate data traffic with voice traffic to the provider side 1000 Mbps GMII/TBI port, thereby eliminating the need for an external Ethernet switch.

The ZL5011x incorporates a range of powerful clock recovery mechanisms for each TDM stream, allowing the frequency of the source clock to be faithfully generated at the destination, enabling greater system performance and quality. Timing is carried using RTP or similar protocols, and both adaptive and differential clock recovery schemes are included, allowing the customer to choose the correct scheme for the application. An externally supplied clock may also be used to drive the TDM interface of the ZL5011x.

The ZL5011x incur very low latency for the data flow, thereby increasing QoS when carrying voice services across the Packet Switched Network. Voice, when carried using CESoP, which typically has latencies of less than 10 ms, does not require expensive processing such as compression and echo cancellation.

The ZL5011x are cost effective devices aimed at the low density applications such as customer premise routers, IADs, ePON termination and Broadband DLCs. For network systems, the ZL5011x is fully compatible and interoperable with the ZL50110/11/12/14 family.

The ZL5011x is capable of assembling user-defined packets of TDM traffic from the TDM interface and transmitting them out the packet interfaces using a variety of protocols. The ZL5011x supports a range of different packet switched networks, including Ethernet VLANs, IP and MPLS. The devices also supports four different classes of service on packet egress, allowing priority treatment of TDM-based traffic. This can be used to help minimize latency variation in the TDM data.

The ZL5011x can support up to 4 protocol stacks at the same time, provided that each protocol stack can be uniquely identified by a mask & match approach.

Packets received from the packet interfaces are parsed to determine the egress destination, and are appropriately queued to the TDM interface, they can also be forwarded to the host interface, or back toward the packet interface. Packets queued to the TDM interface can be re-ordered based on sequence number, and lost packets filled in to maintain timing integrity.

The ZL5011x includes on-chip memory sufficient for all applications, thereby reducing system costs, board area, power, and design complexity.

A comprehensive evaluation system is available upon request from your local Zarlink representative or distributor. This system includes the CESoP processor, various TDM interfaces and a fully featured evaluation software GUI that will run on a Windows PC.

3.0 Physical Specification

The ZL5011x will be packaged in a PBGA device.

Features:

- Body Size: 23 mm x 23 mm (typ)
- Ball Count: 324
- Ball Pitch: 1.00 mm (typ)
- Ball Matrix: 22 x 22
- Ball Diameter: 0.60 mm (typ)
- Total Package Thickness: 2.03 mm (typ)

ZL50115 Package view from TOP side. Note that ball A1 is non-chamfered corner.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
A	VDD_IO	NC	M0_TXCLK	M0_RXD[7]	M0_RXD[6]	M0_RXD[4]	M0_COL	M0_GTX_CLK	M0_TXEN	DEVICE_ID[4]	CPU_DATA[28]	CPU_DATA[24]	GND	CPU_DATA[23]	GND	CPU_DATA[19]	CPU_DATA[12]	CPU_DATA[9]	CPU_DATA[8]	CPU_DATA[7]	CPU_SDACK1	VDD_IO
B	NC	VDD_IO	GND	NC	NC	M0_CRS	M0_RXD[0]	M0_RBC1	M0_RBC0	M0_TXER	GND	M0_TXD[5]	M0_TXD[3]	M0_TXD[2]	NC	CPU_DATA[27]	CPU_DATA[22]	CPU_DATA[20]	CPU_DATA[13]	GND	VDD_IO	CPU_TA
C	NC	GND	VDD_IO	NC	NC	NC	M0_RXDV	M0_RXD[3]	M0_RXD[1]	M0_RXCLK	M0_TXD[7]	M0_TXD[4]	M0_TXD[0]	VDD_IO	VDD_IO	CPU_DATA[31]	NC	CPU_DATA[29]	CPU_DATA[26]	VDD_IO	GND	CPU_DREQ1
D	NC	NC	NC	VDD_IO	NC	M0_RXER	VDD_IO	M0_RXD[5]	VDD_CORE	M0_RXD[2]	M0_REFCLK	M0_TXD[6]	M0_TXD[1]	VDD_CORE	VDD_CORE	VDD_IO	M0_ACTIVE_LED	VDD_CORE	VDD_IO	CPU_DATA[25]	CPU_ADDR[23]	CPU_DATA[6]
E	NC	M0_GIGABIT_LED	NC	NC															CPU_DATA[30]	CPU_DATA[21]	CPU_DATA[15]	CPU_DATA[14]
F	NC	NC	DEVICE_ID[1]	VDD_CORE															VDD_CORE	CPU_DATA[18]	CPU_DATA[17]	CPU_DATA[16]
G	M_MDIO	DEVICE_ID[0]	M0_LINKUP_LED	VDD_IO															VDD_IO	CPU_IREQ1	CPU_DATA[11]	CPU_DATA[0]
H	M_MDC	GND	NC	VDD_CORE															CPU_DATA[10]	CPU_DATA[1]	CPU_DATA[4]	NC
J	NC	NC	NC	VDD_CORE					GND	GND	GND	GND	GND	GND					VDD_CORE	CPU_DATA[5]	CPU_DATA[3]	CPU_IREQ0
K	NC	NC	NC	VDD_IO					GND	GND	GND	GND	GND	GND					GND	CPU_DATA[2]	NC	CPU_DREQ0
L	GND	AUX_CLKO	AUX_CLKI	VDD_CORE					GND	GND	GND	GND	GND	GND					CPU_CLK	GND	CPU_SDACK2	NC_VDD_IO
M	NC	NC	NC	VDD_IO					GND	GND	GND	GND	GND	GND					GND	CPU_TS_ALE	CPU_WE	CPU_OE
N	NC	NC	NC	VDD_CORE					GND	GND	GND	GND	GND	GND					VDD_IO	CPU_ADDR[22]	CPU_CS	CPU_ADDR[19]
P	NC	GND	VDD_IO	VDD_CORE					GND	GND	GND	GND	GND	GND					VDD_CORE	CPU_ADDR[17]	CPU_ADDR[18]	CPU_ADDR[21]
R	NC	NC	TDM_CLKI[0]	NC															GND	CPU_ADDR[11]	CPU_ADDR[13]	CPU_ADDR[20]
T	NC	NC	TDM_FRMI_REF	VDD_IO															VDD_IO	VDD_IO	CPU_ADDR[14]	CPU_ADDR[16]
U	TDM_STI[0]	VDD_IO	GND	TDM_CLKiS															VDD_CORE	JTAG_TMS	CPU_ADDR[15]	CPU_ADDR[12]
V	TDM_STO[0]	TDM_CLKO[0]	TDM_CLKO_REF	TDM_CLKiP															DEVICE_ID[3]	JTAG_TCK	CPU_ADDR[10]	CPU_ADDR[9]
W	NC	TDM_CLKI_REF	TDM_FRMO_REF	VDD_IO	VDD_IO	VDD_CORE	VDD_IO	VDD_IO	VDD_CORE	PLL_SEC	NC_GND	GND	SYSTEM_CLK	VDD_CORE	GPIO[9]	VDD_IO	GPIO[15]	DEVICE_ID[2]	VDD_IO	JTAG_TDO	CPU_ADDR[4]	CPU_ADDR[8]
Y	NC	GND	VDD_IO	NC	NC	VDD_CORE	NC	NC	PLL_PRI	NC	NC_GND	NC	GND	GND	GPIO[8]	GPIO[14]	TEST_MODE[1]	JTAG_TRST	NC_GND	VDD_IO	GND	CPU_ADDR[7]
AA	NC	VDD_IO	GND	VDD_IO	VDD_IO	NC	GND	A1VDD_PLL	NC	NC	SYSTEM_DEBUG	SYSTEM_RST	GPIO[1]	GPIO[2]	GPIO[7]	GPIO[12]	TEST_MODE[0]	JTAG_TDI	NC_GND	GND	VDD_IO	CPU_ADDR[6]
AB	VDD_IO	NC	NC	NC	GND	NC	NC	NC	GPIO[0]	GPIO[3]	GPIO[4]	GPIO[5]	GPIO[6]	GPIO[10]	GPIO[11]	GPIO[13]	TEST_MODE[2]	NC_GND	CPU_ADDR[2]	CPU_ADDR[3]	CPU_ADDR[5]	VDD_IO

Figure 2 - ZL50115 Package View and Ball Positions

ZL50116 Package view from TOP side. Note that ball A1 is non-chamfered corner.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
A	VDD_IO	NC	M0_TXCLK	M0_RXD[7]	M0_RXD[6]	M0_RXD[4]	M0_COL	M0_GTX_CLK	M0_TXEN	DEVICE_ID[4]	CPU_DATA[28]	CPU_DATA[24]	GND	CPU_DATA[23]	GND	CPU_DATA[19]	CPU_DATA[12]	CPU_DATA[9]	CPU_DATA[8]	CPU_DATA[7]	CPU_SDACK1	VDD_IO
B	NC	VDD_IO	GND	NC	NC	M0_CRS	M0_RXD[0]	M0_RBC1	M0_RBC0	M0_TXER	GND	M0_TXD[5]	M0_TXD[3]	M0_TXD[2]	NC	CPU_DATA[27]	CPU_DATA[22]	CPU_DATA[20]	CPU_DATA[13]	GND	VDD_IO	CPU_TA
C	NC	GND	VDD_IO	NC	NC	NC	M0_RXDV	M0_RXD[3]	M0_RXD[1]	M0_RXCLK	M0_TXD[7]	M0_TXD[4]	M0_TXD[0]	VDD_IO	VDD_IO	CPU_DATA[31]	NC	CPU_DATA[29]	CPU_DATA[26]	VDD_IO	GND	CPU_DREQ1
D	NC	NC	NC	VDD_IO	NC	M0_RXER	VDD_IO	M0_RXD[5]	VDD_CORE	M0_RXD[2]	M0_REFCLK	M0_TXD[6]	M0_TXD[1]	VDD_CORE	VDD_CORE	VDD_IO	M0_ACTIVE_LED	VDD_CORE	VDD_IO	CPU_DATA[25]	CPU_ADDR[23]	CPU_DATA[6]
E	NC	M0_GIGABIT_LED	NC	NC															CPU_DATA[30]	CPU_DATA[21]	CPU_DATA[15]	CPU_DATA[14]
F	NC	NC	DEVICE_ID[1]	VDD_CORE															VDD_CORE	CPU_DATA[18]	CPU_DATA[17]	CPU_DATA[16]
G	M_MDIO	DEVICE_ID[0]	M0_LINKUP_LED	VDD_IO															VDD_IO	CPU_IREQ1	CPU_DATA[11]	CPU_DATA[0]
H	M_MDC	GND	NC	VDD_CORE															CPU_DATA[10]	CPU_DATA[1]	CPU_DATA[4]	NC
J	NC	NC	NC	VDD_CORE					GND	GND	GND	GND	GND	GND					VDD_CORE	CPU_DATA[5]	CPU_DATA[3]	CPU_IREQ0
K	NC	NC	NC	VDD_IO					GND	GND	GND	GND	GND	GND					GND	CPU_DATA[2]	NC	CPU_DREQ0
L	GND	AUX_CLKO	AUX_CLKI	VDD_CORE					GND	GND	GND	GND	GND	GND					CPU_CLK	GND	CPU_SDACK2	NC_VDD_IO
M	NC	NC	NC	VDD_IO					GND	GND	GND	GND	GND	GND					GND	CPU_TS_ALE	CPU_WE	CPU_OE
N	NC	NC	NC	VDD_CORE					GND	GND	GND	GND	GND	GND					VDD_IO	CPU_ADDR[22]	CPU_CS	CPU_ADDR[19]
P	NC	GND	VDD_IO	VDD_CORE					GND	GND	GND	GND	GND	GND					VDD_CORE	CPU_ADDR[17]	CPU_ADDR[18]	CPU_ADDR[21]
R	NC	TDM_STI[1]	TDM_CLKI[1]	TDM_STO[1]															GND	CPU_ADDR[11]	CPU_ADDR[13]	CPU_ADDR[20]
T	TDM_CLKI[1]	TDM_CLKO[1]	TDM_FRMI_REF	VDD_IO															VDD_IO	VDD_IO	CPU_ADDR[14]	CPU_ADDR[16]
U	TDM_STI[0]	VDD_IO	GND	TDM_CLKIS															VDD_CORE	JTAG_TMS	CPU_ADDR[15]	CPU_ADDR[12]
V	TDM_STO[0]	TDM_CLKO[0]	TDM_CLKO_REF	TDM_CLKIP															DEVICE_ID[3]	JTAG_TCK	CPU_ADDR[10]	CPU_ADDR[9]
W	NC	TDM_CLKI_REF	TDM_FRMIO_REF	VDD_IO	VDD_IO	VDD_CORE	VDD_IO	VDD_IO	VDD_CORE	PLL_SEC	NC_GND	GND	SYSTEM_CLK	VDD_CORE	GPIO[9]	VDD_IO	GPIO[15]	DEVICE_ID[2]	VDD_IO	JTAG_TDO	CPU_ADDR[4]	CPU_ADDR[8]
Y	NC	GND	VDD_IO	NC	NC	VDD_CORE	NC	NC	PLL_PRI	NC	NC_GND	NC	GND	GND	GPIO[8]	GPIO[14]	TEST_MODE[1]	JTAG_TRST	NC_GND	VDD_IO	GND	CPU_ADDR[7]
AA	NC	VDD_IO	GND	VDD_IO	VDD_IO	NC	GND	A1VDD_PLL1	NC	NC	SYSTEM_DEBUG	SYSTEM_RST	GPIO[1]	GPIO[2]	GPIO[7]	GPIO[12]	TEST_MODE[0]	JTAG_TDI	NC_GND	GND	VDD_IO	CPU_ADDR[6]
AB	VDD_IO	NC	NC	NC	GND	NC	NC	NC	GPIO[0]	GPIO[3]	GPIO[4]	GPIO[5]	GPIO[6]	GPIO[10]	GPIO[11]	GPIO[13]	TEST_MODE[2]	NC_GND	CPU_ADDR[2]	CPU_ADDR[3]	CPU_ADDR[5]	VDD_IO

Figure 3 - ZL50116 Package View and Ball Positions

ZL50117 Package view from TOP side. Note that ball A1 is non-chamfered corner.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
A	VDD_IO	NC	M0_TXCLK	M0_RXD[7]	M0_RXD[6]	M0_RXD[4]	M0_COL	M0_GTX_CLK	M0_TXEN	DEVICE_ID[4]	CPU_DATA[28]	CPU_DATA[24]	GND	CPU_DATA[23]	GND	CPU_DATA[19]	CPU_DATA[12]	CPU_DATA[9]	CPU_DATA[8]	CPU_DATA[7]	CPU_SDACK1	VDD_IO
B	NC	VDD_IO	GND	NC	NC	M0_CRS	M0_RXD[0]	M0_RBC1	M0_RBC0	M0_TXER	GND	M0_TXD[5]	M0_TXD[3]	M0_TXD[2]	NC	CPU_DATA[27]	CPU_DATA[22]	CPU_DATA[20]	CPU_DATA[13]	GND	VDD_IO	CPU_TA
C	NC	GND	VDD_IO	NC	NC	NC	M0_RXDV	M0_RXD[3]	M0_RXD[1]	M0_RXCLK	M0_TXD[7]	M0_TXD[4]	M0_TXD[0]	VDD_IO	VDD_IO	CPU_DATA[31]	NC	CPU_DATA[29]	CPU_DATA[26]	VDD_IO	GND	CPU_DREQ1
D	NC	NC	NC	VDD_IO	NC	M0_RXER	VDD_IO	M0_RXD[5]	VDD_CORE	M0_RXD[2]	M0_REFCLK	M0_TXD[6]	M0_TXD[1]	VDD_CORE	VDD_CORE	VDD_IO	M0_ACTIVE_LED	VDD_CORE	VDD_IO	CPU_DATA[25]	CPU_ADDR[23]	CPU_DATA[6]
E	NC	M0_GIGABIT_LED	NC	NC															CPU_DATA[30]	CPU_DATA[21]	CPU_DATA[15]	CPU_DATA[14]
F	NC	NC	DEVICE_ID[1]	VDD_CORE															VDD_CORE	CPU_DATA[18]	CPU_DATA[17]	CPU_DATA[16]
G	M_MDIO	DEVICE_ID[0]	M0_LINKUP_LED	VDD_IO															VDD_IO	CPU_IREQ1	CPU_DATA[11]	CPU_DATA[0]
H	M_MDC	GND	NC	VDD_CORE															CPU_DATA[10]	CPU_DATA[1]	CPU_DATA[4]	NC
J	NC	NC	NC	VDD_CORE					GND	GND	GND	GND	GND	GND					VDD_CORE	CPU_DATA[5]	CPU_DATA[3]	CPU_IREQ0
K	NC	NC	NC	VDD_IO					GND	GND	GND	GND	GND	GND					GND	CPU_DATA[2]	NC	CPU_DREQ0
L	GND	AUX_CLKO	AUX_CLKI	VDD_CORE					GND	GND	GND	GND	GND	GND					CPU_CLK	GND	CPU_SDACK2	NC_VDD_IO
M	TDM_CLKI[3]	TDM_STO[3]	TDM_STI[3]	VDD_IO					GND	GND	GND	GND	GND	GND					GND	CPU_TS_ALE	CPU_WE	CPU_OE
N	TDM_STO[2]	TDM_CLKO[3]	TDM_STI[2]	VDD_CORE					GND	GND	GND	GND	GND	GND					VDD_IO	CPU_ADDR[22]	CPU_CS	CPU_ADDR[19]
P	TDM_CLKI[2]	GND	VDD_IO	VDD_CORE					GND	GND	GND	GND	GND	GND					VDD_CORE	CPU_ADDR[17]	CPU_ADDR[18]	CPU_ADDR[21]
R	TDM_CLKO[2]	TDM_STI[1]	TDM_CLKI[0]	TDM_STO[1]															GND	CPU_ADDR[11]	CPU_ADDR[13]	CPU_ADDR[20]
T	TDM_CLKI[1]	TDM_CLKO[1]	TDM_FRMI_REF	VDD_IO															VDD_IO	VDD_IO	CPU_ADDR[14]	CPU_ADDR[16]
U	TDM_STI[0]	VDD_IO	GND	TDM_CLKIS															VDD_CORE	JTAG_TMS	CPU_ADDR[15]	CPU_ADDR[12]
V	TDM_STO[0]	TDM_CLKO[0]	TDM_CLKO_REF	TDM_CLKIP															DEVICE_ID[3]	JTAG_TCK	CPU_ADDR[10]	CPU_ADDR[9]
W	NC	TDM_CLKI_REF	TDM_FRMIO_REF	VDD_IO	VDD_IO	VDD_CORE	VDD_IO	VDD_IO	VDD_CORE	PLL_SEC	NC_GND	GND	SYSTEM_CLK	VDD_CORE	GPIO[9]	VDD_IO	GPIO[15]	DEVICE_ID[2]	VDD_IO	JTAG_TDO	CPU_ADDR[4]	CPU_ADDR[8]
Y	NC	GND	VDD_IO	NC	NC	VDD_CORE	NC	NC	PLL_PRI	NC	NC_GND	NC	GND	GND	GPIO[8]	GPIO[14]	TEST_MODE[1]	JTAG_TRST	NC_GND	VDD_IO	GND	CPU_ADDR[7]
AA	NC	VDD_IO	GND	VDD_IO	VDD_IO	NC	GND	A1VDD_PLL1	NC	NC	SYSTEM_DEBUG	SYSTEM_RST	GPIO[1]	GPIO[2]	GPIO[7]	GPIO[12]	TEST_MODE[0]	JTAG_TDI	NC_GND	GND	VDD_IO	CPU_ADDR[6]
AB	VDD_IO	NC	NC	NC	GND	NC	NC	NC	GPIO[0]	GPIO[3]	GPIO[4]	GPIO[5]	GPIO[6]	GPIO[10]	GPIO[11]	GPIO[13]	TEST_MODE[2]	NC_GND	CPU_ADDR[2]	CPU_ADDR[3]	CPU_ADDR[5]	VDD_IO

Figure 4 - ZL50117 Package View and Ball Positions

ZL50118 Package view from TOP side. Note that ball A1 is non-chamfered corner.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
A	VDD_IO	M1_TXEN	M0_TXCLK	M0_RXD[7]	M0_RXD[6]	M0_RXD[4]	M0_COL	M0_GTX_CLK	M0_TXEN	DEVICE_ID[4]	CPU_DATA[28]	CPU_DATA[24]	GND	CPU_DATA[23]	GND	CPU_DATA[19]	CPU_DATA[12]	CPU_DATA[9]	CPU_DATA[8]	CPU_DATA[7]	CPU_SDACK1	VDD_IO
B	M1_TXD[2]	VDD_IO	GND	M1_TXD[0]	M1_TXD[1]	M0_CRS	M0_RXD[0]	M0_RBC1	M0_RBC0	M0_TXER	GND	M0_TXD[5]	M0_TXD[3]	M0_TXD[2]	M1_ACTIVE_LED	CPU_DATA[27]	CPU_DATA[22]	CPU_DATA[20]	CPU_DATA[13]	GND	VDD_IO	CPU_TA
C	M1_TXD[3]	GND	VDD_IO	M1_RXCLK	M1_COL	M1_TXER	M0_RXDV	M0_RXD[3]	M0_RXD[1]	M0_RXCLK	M0_TXD[7]	M0_TXD[4]	M0_TXD[0]	VDD_IO	VDD_IO	CPU_DATA[31]	M1_LINKUP_LED	CPU_DATA[29]	CPU_DATA[26]	VDD_IO	GND	CPU_DREQ1
D	M1_RXD[1]	M1_RXD[0]	M1_RXD[2]	VDD_IO	M1_RXDV	M0_RXER	VDD_IO	M0_RXD[5]	VDD_CORE	M0_RXD[2]	M0_REFCLK	M0_TXD[6]	M0_TXD[1]	VDD_CORE	VDD_CORE	VDD_IO	M0_ACTIVE_LED	VDD_CORE	VDD_IO	CPU_DATA[25]	CPU_ADDR[23]	CPU_DATA[6]
E	M1_RXD[3]	M0_GIGABIT_LED	M1_TXCLK	M1_RXER															CPU_DATA[30]	CPU_DATA[21]	CPU_DATA[15]	CPU_DATA[14]
F	NC	M1_CRS	DEVICE_ID[1]	VDD_CORE															VDD_CORE	CPU_DATA[18]	CPU_DATA[17]	CPU_DATA[16]
G	M_MDIO	DEVICE_ID[0]	M0_LINKUP_LED	VDD_IO															VDD_IO	CPU_IREQ1	CPU_DATA[11]	CPU_DATA[0]
H	M_MDC	GND	NC	VDD_CORE															CPU_DATA[10]	CPU_DATA[1]	CPU_DATA[4]	IC
J	NC	NC	NC	VDD_CORE					GND	GND	GND	GND	GND	GND					VDD_CORE	CPU_DATA[5]	CPU_DATA[3]	CPU_IREQ0
K	NC	NC	NC	VDD_IO					GND	GND	GND	GND	GND	GND					GND	CPU_DATA[2]	IC	CPU_DREQ0
L	GND	AUX_CLKO	AUX_CLKI	VDD_CORE					GND	GND	GND	GND	GND	GND					CPU_CLK	GND	CPU_SDACK2	IC_VDD_IO
M	NC	NC	NC	VDD_IO					GND	GND	GND	GND	GND	GND					GND	CPU_TS_ALE	CPU_WE	CPU_OE
N	NC	NC	NC	VDD_CORE					GND	GND	GND	GND	GND	GND					VDD_IO	CPU_ADDR[22]	CPU_CS	CPU_ADDR[19]
P	NC	GND	VDD_IO	VDD_CORE					GND	GND	GND	GND	GND	GND					VDD_CORE	CPU_ADDR[17]	CPU_ADDR[18]	CPU_ADDR[21]
R	NC	NC	TDM_CLKI[0]	NC															GND	CPU_ADDR[11]	CPU_ADDR[13]	CPU_ADDR[20]
T	NC	NC	TDM_FRMI_REF	VDD_IO															VDD_IO	VDD_IO	CPU_ADDR[14]	CPU_ADDR[16]
U	TDM_STI[0]	VDD_IO	GND	TDM_CLKIS															VDD_CORE	JTAG_TMS	CPU_ADDR[15]	CPU_ADDR[12]
V	TDM_STO[0]	TDM_CLKO[0]	TDM_CLKO_REF	TDM_CLKOP															DEVICE_ID[3]	JTAG_TCK	CPU_ADDR[10]	CPU_ADDR[9]
W	IC	TDM_CLKI_REF	TDM_FRMO_REF	VDD_IO	VDD_IO	VDD_CORE	VDD_IO	VDD_IO	VDD_CORE	PLL_SEC	IC_GND	GND	SYSTEM_CLK	VDD_CORE	GPIO[9]	VDD_IO	GPIO[15]	DEVICE_ID[2]	VDD_IO	JTAG_TDO	CPU_ADDR[4]	CPU_ADDR[8]
Y	IC	GND	VDD_IO	IC	IC	VDD_CORE	IC	IC	PLL_PRI	IC	IC_GND	IC	GND	GND	GPIO[8]	GPIO[14]	TEST_MODE[1]	JTAG_TRST	IC_GND	VDD_IO	GND	CPU_ADDR[7]
AA	IC	VDD_IO	GND	VDD_IO	VDD_IO	IC	GND	A1VDD_PLL1	IC	IC	SYSTEM_DEBUG	SYSTEM_RST	GPIO[1]	GPIO[2]	GPIO[7]	GPIO[12]	TEST_MODE[0]	JTAG_TDI	IC_GND	GND	VDD_IO	CPU_ADDR[6]
AB	VDD_IO	IC	IC	IC	GND	IC	IC	IC	GPIO[0]	GPIO[3]	GPIO[4]	GPIO[5]	GPIO[6]	GPIO[10]	GPIO[11]	GPIO[13]	TEST_MODE[2]	IC_GND	CPU_ADDR[2]	CPU_ADDR[3]	CPU_ADDR[5]	VDD_IO

Figure 5 - ZL50118 Package View and Ball Positions

ZL50119 Package view from TOP side. Note that ball A1 is non-chamfered corner.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
A	VDD_IO	M1_TXEN	M0_TXCLK	M0_RXD[7]	M0_RXD[6]	M0_RXD[4]	M0_COL	M0_GTX_CLK	M0_TXEN	DEVICE_ID[4]	CPU_DATA[28]	CPU_DATA[24]	GND	CPU_DATA[23]	GND	CPU_DATA[19]	CPU_DATA[12]	CPU_DATA[9]	CPU_DATA[8]	CPU_DATA[7]	CPU_SDACK1	VDD_IO
B	M1_TXD[2]	VDD_IO	GND	M1_TXD[0]	M1_TXD[1]	M0_CRS	M0_RXD[0]	M0_RBC1	M0_RBC0	M0_TXER	GND	M0_TXD[5]	M0_TXD[3]	M0_TXD[2]	M1_ACTIVE_LED	CPU_DATA[27]	CPU_DATA[22]	CPU_DATA[20]	CPU_DATA[13]	GND	VDD_IO	CPU_TA
C	M1_TXD[3]	GND	VDD_IO	M1_RXCLK	M1_COL	M1_TXER	M0_RXDV	M0_RXD[3]	M0_RXD[1]	M0_RXCLK	M0_TXD[7]	M0_TXD[4]	M0_TXD[0]	VDD_IO	VDD_IO	CPU_DATA[31]	M1_LINKUP_LED	CPU_DATA[29]	CPU_DATA[26]	VDD_IO	GND	CPU_DREQ1
D	M1_RXD[1]	M1_RXD[0]	M1_RXD[2]	VDD_IO	M1_RXDV	M0_RXER	VDD_IO	M0_RXD[5]	VDD_CORE	M0_RXD[2]	M0_REFCLK	M0_TXD[6]	M0_TXD[1]	VDD_CORE	VDD_CORE	VDD_IO	M0_ACTIVE_LED	VDD_CORE	VDD_IO	CPU_DATA[25]	CPU_ADDR[23]	CPU_DATA[6]
E	M1_RXD[3]	M0_GIGABIT_LED	M1_TXCLK	M1_RXER															CPU_DATA[30]	CPU_DATA[21]	CPU_DATA[15]	CPU_DATA[14]
F	NC	M1_CRS	DEVICE_ID[1]	VDD_CORE															VDD_CORE	CPU_DATA[18]	CPU_DATA[17]	CPU_DATA[16]
G	M_MDIO	DEVICE_ID[0]	M0_LINKUP_LED	VDD_IO															VDD_IO	CPU_IREQ1	CPU_DATA[11]	CPU_DATA[0]
H	M_MDC	GND	NC	VDD_CORE															CPU_DATA[10]	CPU_DATA[1]	CPU_DATA[4]	IC
J	NC	NC	NC	VDD_CORE					GND	GND	GND	GND	GND	GND					VDD_CORE	CPU_DATA[5]	CPU_DATA[3]	CPU_IREQ0
K	NC	NC	NC	VDD_IO					GND	GND	GND	GND	GND	GND					GND	CPU_DATA[2]	IC	CPU_DREQ0
L	GND	AUX_CLKO	AUX_CLKI	VDD_CORE					GND	GND	GND	GND	GND	GND					CPU_CLK	GND	CPU_SDACK2	IC_VDD_IO
M	NC	NC	NC	VDD_IO					GND	GND	GND	GND	GND	GND					GND	CPU_TS_ALE	CPU_WE	CPU_OE
N	NC	NC	NC	VDD_CORE					GND	GND	GND	GND	GND	GND					VDD_IO	CPU_ADDR[22]	CPU_CS	CPU_ADDR[19]
P	NC	GND	VDD_IO	VDD_CORE					GND	GND	GND	GND	GND	GND					VDD_CORE	CPU_ADDR[17]	CPU_ADDR[18]	CPU_ADDR[21]
R	NC	TDM_STI[1]	TDM_CLKI[0]	TDM_STO[1]															GND	CPU_ADDR[11]	CPU_ADDR[13]	CPU_ADDR[20]
T	TDM_CLKI[1]	TDM_CLKO[1]	TDM_FRMI_REF	VDD_IO															VDD_IO	VDD_IO	CPU_ADDR[14]	CPU_ADDR[16]
U	TDM_STI[0]	VDD_IO	GND	TDM_CLKIS															VDD_CORE	JTAG_TMS	CPU_ADDR[15]	CPU_ADDR[12]
V	TDM_STO[0]	TDM_CLKO[0]	TDM_CLKO_REF	TDM_CLKP															DEVICE_ID[3]	JTAG_TCK	CPU_ADDR[10]	CPU_ADDR[9]
W	IC	TDM_CLKI_REF	TDM_FRMO_REF	VDD_IO	VDD_IO	VDD_CORE	VDD_IO	VDD_IO	VDD_CORE	PLL_SEC	IC_GND	GND	SYSTEM_CLK	VDD_CORE	GPIO[9]	VDD_IO	GPIO[15]	DEVICE_ID[2]	VDD_IO	JTAG_TDO	CPU_ADDR[4]	CPU_ADDR[8]
Y	IC	GND	VDD_IO	IC	IC	VDD_CORE	IC	IC	PLL_PRI	IC	IC_GND	IC	GND	GND	GPIO[8]	GPIO[14]	TEST_MODE[1]	JTAG_TRST	IC_GND	VDD_IO	GND	CPU_ADDR[7]
AA	IC	VDD_IO	GND	VDD_IO	VDD_IO	IC	GND	A1VDD_PLL1	IC	IC	SYSTEM_DEBUG	SYSTEM_RST	GPIO[1]	GPIO[2]	GPIO[7]	GPIO[12]	TEST_MODE[0]	JTAG_TDI	IC_GND	GND	VDD_IO	CPU_ADDR[6]
AB	VDD_IO	IC	IC	IC	GND	IC	IC	IC	GPIO[0]	GPIO[3]	GPIO[4]	GPIO[5]	GPIO[6]	GPIO[10]	GPIO[11]	GPIO[13]	TEST_MODE[2]	IC_GND	CPU_ADDR[2]	CPU_ADDR[3]	CPU_ADDR[5]	VDD_IO

Figure 6 - ZL50119 Package View and Ball Positions

ZL50120 Package view from TOP side. Note that ball A1 is non-chamfered corner.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
A	VDD_IO	M1_TXEN	M0_TXCLK	M0_RXD[7]	M0_RXD[6]	M0_RXD[4]	M0_COL	M0_GTX_CLK	M0_TXEN	DEVICE_ID[4]	CPU_DATA[28]	CPU_DATA[24]	GND	CPU_DATA[23]	GND	CPU_DATA[19]	CPU_DATA[12]	CPU_DATA[9]	CPU_DATA[8]	CPU_DATA[7]	CPU_SDACK1	VDD_IO
B	M1_TXD[2]	VDD_IO	GND	M1_TXD[0]	M1_TXD[1]	M0_CRS	M0_RXD[0]	M0_RBC1	M0_RBC0	M0_TXER	GND	M0_TXD[5]	M0_TXD[3]	M0_TXD[2]	M1_ACTIVE_LED	CPU_DATA[27]	CPU_DATA[22]	CPU_DATA[20]	CPU_DATA[13]	GND	VDD_IO	CPU_TA
C	M1_TXD[3]	GND	VDD_IO	M1_RXCLK	M1_COL	M1_TXER	M0_RXDV	M0_RXD[3]	M0_RXD[1]	M0_RXCLK	M0_TXD[7]	M0_TXD[4]	M0_TXD[0]	VDD_IO	VDD_IO	CPU_DATA[31]	M1_LINKUP_LED	CPU_DATA[29]	CPU_DATA[26]	VDD_IO	GND	CPU_DREQ1
D	M1_RXD[1]	M1_RXD[0]	M1_RXD[2]	VDD_IO	M1_RXDV	M0_RXER	VDD_IO	M0_RXD[5]	VDD_CORE	M0_RXD[2]	M0_REFCLK	M0_TXD[6]	M0_TXD[1]	VDD_CORE	VDD_CORE	VDD_IO	M0_ACTIVE_LED	VDD_CORE	VDD_IO	CPU_DATA[25]	CPU_ADDR[23]	CPU_DATA[6]
E	M1_RXD[3]	M0_GIGABIT_LED	M1_TXCLK	M1_RXER															CPU_DATA[30]	CPU_DATA[21]	CPU_DATA[15]	CPU_DATA[14]
F	NC	M1_CRS	DEVICE_ID[1]	VDD_CORE															VDD_CORE	CPU_DATA[18]	CPU_DATA[17]	CPU_DATA[16]
G	M_MDIO	DEVICE_ID[0]	M0_LINKUP_LED	VDD_IO															VDD_IO	CPU_IREQ1	CPU_DATA[11]	CPU_DATA[0]
H	M_MDC	GND	NC	VDD_CORE															CPU_DATA[10]	CPU_DATA[1]	CPU_DATA[4]	IC
J	NC	NC	NC	VDD_CORE					GND	GND	GND	GND	GND	GND					VDD_CORE	CPU_DATA[5]	CPU_DATA[3]	CPU_IREQ0
K	NC	NC	NC	VDD_IO					GND	GND	GND	GND	GND	GND					GND	CPU_DATA[2]	IC	CPU_DREQ0
L	GND	AUX_CLKO	AUX_CLKI	VDD_CORE					GND	GND	GND	GND	GND	GND					CPU_CLK	GND	CPU_SDACK2	IC_VDD_IO
M	TDM_CLKI[3]	TDM_STO[3]	TDM_STI[3]	VDD_IO					GND	GND	GND	GND	GND	GND					GND	CPU_TS_ALE	CPU_WE	CPU_OE
N	TDM_STO[2]	TDM_CLKO[3]	TDM_STI[2]	VDD_CORE					GND	GND	GND	GND	GND	GND					VDD_IO	CPU_ADDR[22]	CPU_CS	CPU_ADDR[19]
P	TDM_CLKI[2]	GND	VDD_IO	VDD_CORE					GND	GND	GND	GND	GND	GND					VDD_CORE	CPU_ADDR[17]	CPU_ADDR[18]	CPU_ADDR[21]
R	TDM_CLKO[2]	TDM_STI[1]	TDM_CLKI[0]	TDM_STO[1]															GND	CPU_ADDR[11]	CPU_ADDR[13]	CPU_ADDR[20]
T	TDM_CLKI[1]	TDM_CLKO[1]	TDM_FRMI_REF	VDD_IO															VDD_IO	VDD_IO	CPU_ADDR[14]	CPU_ADDR[16]
U	TDM_STI[0]	VDD_IO	GND	TDM_CLKS															VDD_CORE	JTAG_TMS	CPU_ADDR[15]	CPU_ADDR[12]
V	TDM_STO[0]	TDM_CLKO[0]	TDM_CLKO_REF	TDM_CLKP															DEVICE_ID[3]	JTAG_TCK	CPU_ADDR[10]	CPU_ADDR[9]
W	IC	TDM_CLKI_REF	TDM_FRMO_REF	VDD_IO	VDD_IO	VDD_CORE	VDD_IO	VDD_IO	VDD_CORE	PLL_SEC	IC_GND	GND	SYSTEM_CLK	VDD_CORE	GPIO[9]	VDD_IO	GPIO[15]	DEVICE_ID[2]	VDD_IO	JTAG_TDO	CPU_ADDR[4]	CPU_ADDR[8]
Y	IC	GND	VDD_IO	IC	IC	VDD_CORE	IC	IC	PLL_PRI	IC	IC_GND	IC	GND	GND	GPIO[8]	GPIO[14]	TEST_MODE[1]	JTAG_TRST	IC_GND	VDD_IO	GND	CPU_ADDR[7]
AA	IC	VDD_IO	GND	VDD_IO	VDD_IO	IC	GND	A1VDD_PLL1	IC	IC	SYSTEM_DEBUG	SYSTEM_RST	GPIO[1]	GPIO[2]	GPIO[7]	GPIO[12]	TEST_MODE[0]	JTAG_TDI	IC_GND	GND	VDD_IO	CPU_ADDR[6]
AB	VDD_IO	IC	IC	IC	GND	IC	IC	IC	GPIO[0]	GPIO[3]	GPIO[4]	GPIO[5]	GPIO[6]	GPIO[10]	GPIO[11]	GPIO[13]	TEST_MODE[2]	IC_GND	CPU_ADDR[2]	CPU_ADDR[3]	CPU_ADDR[5]	VDD_IO

Figure 7 - ZL50120 Package View and Ball Positions

Ball #	ZL50115 Signal Name	ZL50116 Signal Name	ZL50117 Signal Name	ZL50118 Signal Name	ZL50119 Signal Name	ZL50120 Signal Name	Variant
A1	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	All
A10	DEVICE_ID[4]	DEVICE_ID[4]	DEVICE_ID[4]	DEVICE_ID[4]	DEVICE_ID[4]	DEVICE_ID[4]	All
A11	CPU_DATA[28]	CPU_DATA[28]	CPU_DATA[28]	CPU_DATA[28]	CPU_DATA[28]	CPU_DATA[28]	All
A12	CPU_DATA[24]	CPU_DATA[24]	CPU_DATA[24]	CPU_DATA[24]	CPU_DATA[24]	CPU_DATA[24]	All
A13	GND	GND	GND	GND	GND	GND	All
A14	CPU_DATA[23]	CPU_DATA[23]	CPU_DATA[23]	CPU_DATA[23]	CPU_DATA[23]	CPU_DATA[23]	All
A15	GND	GND	GND	GND	GND	GND	All
A16	CPU_DATA[19]	CPU_DATA[19]	CPU_DATA[19]	CPU_DATA[19]	CPU_DATA[19]	CPU_DATA[19]	All
A17	CPU_DATA[12]	CPU_DATA[12]	CPU_DATA[12]	CPU_DATA[12]	CPU_DATA[12]	CPU_DATA[12]	All
A18	CPU_DATA[9]	CPU_DATA[9]	CPU_DATA[9]	CPU_DATA[9]	CPU_DATA[9]	CPU_DATA[9]	All
A19	CPU_DATA[8]	CPU_DATA[8]	CPU_DATA[8]	CPU_DATA[8]	CPU_DATA[8]	CPU_DATA[8]	All
A20	CPU_DATA[7]	CPU_DATA[7]	CPU_DATA[7]	CPU_DATA[7]	CPU_DATA[7]	CPU_DATA[7]	All
A21	CPU_SDACK1	CPU_SDACK1	CPU_SDACK1	CPU_SDACK1	CPU_SDACK1	CPU_SDACK1	All
A22	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	All
A2	NC	NC	NC	M1_TXEN	M1_TXEN	M1_TXEN	ZL50118/19/20
A3	M0_TXCLK	M0_TXCLK	M0_TXCLK	M0_TXCLK	M0_TXCLK	M0_TXCLK	All
A4	M0_RXD[7]	M0_RXD[7]	M0_RXD[7]	M0_RXD[7]	M0_RXD[7]	M0_RXD[7]	All
A5	M0_RXD[6]	M0_RXD[6]	M0_RXD[6]	M0_RXD[6]	M0_RXD[6]	M0_RXD[6]	All
A6	M0_RXD[4]	M0_RXD[4]	M0_RXD[4]	M0_RXD[4]	M0_RXD[4]	M0_RXD[4]	All
A7	M0_COL	M0_COL	M0_COL	M0_COL	M0_COL	M0_COL	All
A8	M0_GTX_CLK	M0_GTX_CLK	M0_GTX_CLK	M0_GTX_CLK	M0_GTX_CLK	M0_GTX_CLK	All
A9	M0_TXEN	M0_TXEN	M0_TXEN	M0_TXEN	M0_TXEN	M0_TXEN	All
B1	NC	NC	NC	M1_TXD[2]	M1_TXD[2]	M1_TXD[2]	ZL50118/19/20
B10	M0_TXER	M0_TXER	M0_TXER	M0_TXER	M0_TXER	M0_TXER	All
B11	GND	GND	GND	GND	GND	GND	All
B12	M0_TXD[5]	M0_TXD[5]	M0_TXD[5]	M0_TXD[5]	M0_TXD[5]	M0_TXD[5]	All
B13	M0_TXD[3]	M0_TXD[3]	M0_TXD[3]	M0_TXD[3]	M0_TXD[3]	M0_TXD[3]	All
B14	M0_TXD[2]	M0_TXD[2]	M0_TXD[2]	M0_TXD[2]	M0_TXD[2]	M0_TXD[2]	All
B15	NC	NC	NC	M1_ACTIVE_LED	M1_ACTIVE_LED	M1_ACTIVE_LED	ZL50118/19/20
B16	CPU_DATA[27]	CPU_DATA[27]	CPU_DATA[27]	CPU_DATA[27]	CPU_DATA[27]	CPU_DATA[27]	All
B17	CPU_DATA[22]	CPU_DATA[22]	CPU_DATA[22]	CPU_DATA[22]	CPU_DATA[22]	CPU_DATA[22]	All
B18	CPU_DATA[20]	CPU_DATA[20]	CPU_DATA[20]	CPU_DATA[20]	CPU_DATA[20]	CPU_DATA[20]	All
B19	CPU_DATA[13]	CPU_DATA[13]	CPU_DATA[13]	CPU_DATA[13]	CPU_DATA[13]	CPU_DATA[13]	All
B20	GND	GND	GND	GND	GND	GND	All
B21	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	All
B22	CPU_TA	CPU_TA	CPU_TA	CPU_TA	CPU_TA	CPU_TA	All
B2	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	All
B3	GND	GND	GND	GND	GND	GND	All
B4	NC	NC	NC	M1_TXD[0]	M1_TXD[0]	M1_TXD[0]	ZL50118/19/20
B5	NC	NC	NC	M1_TXD[1]	M1_TXD[1]	M1_TXD[1]	ZL50118/19/20
B6	M0_CRS	M0_CRS	M0_CRS	M0_CRS	M0_CRS	M0_CRS	All
B7	M0_RXD[0]	M0_RXD[0]	M0_RXD[0]	M0_RXD[0]	M0_RXD[0]	M0_RXD[0]	All
B8	M0_RBC1	M0_RBC1	M0_RBC1	M0_RBC1	M0_RBC1	M0_RBC1	All

Table 2 - ZL50115/16/17/18/19/20 Ball Signal Assignment

Ball #	ZL50115 Signal Name	ZL50116 Signal Name	ZL50117 Signal Name	ZL50118 Signal Name	ZL50119 Signal Name	ZL50120 Signal Name	Variant
B9	M0_RBC0	M0_RBC0	M0_RBC0	M0_RBC0	M0_RBC0	M0_RBC0	All
C1	NC	NC	NC	M1_TXD[3]	M1_TXD[3]	M1_TXD[3]	ZL50118/19/20
C10	M0_RXCLK	M0_RXCLK	M0_RXCLK	M0_RXCLK	M0_RXCLK	M0_RXCLK	All
C11	M0_TXD[7]	M0_TXD[7]	M0_TXD[7]	M0_TXD[7]	M0_TXD[7]	M0_TXD[7]	All
C12	M0_TXD[4]	M0_TXD[4]	M0_TXD[4]	M0_TXD[4]	M0_TXD[4]	M0_TXD[4]	All
C13	M0_TXD[0]	M0_TXD[0]	M0_TXD[0]	M0_TXD[0]	M0_TXD[0]	M0_TXD[0]	All
C14	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	All
C15	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	All
C16	CPU_DATA[31]	CPU_DATA[31]	CPU_DATA[31]	CPU_DATA[31]	CPU_DATA[31]	CPU_DATA[31]	All
C17	NC	NC	NC	M1_LINKUP_LED	M1_LINKUP_LED	M1_LINKUP_LED	ZL50118/19/20
C18	CPU_DATA[29]	CPU_DATA[29]	CPU_DATA[29]	CPU_DATA[29]	CPU_DATA[29]	CPU_DATA[29]	All
C19	CPU_DATA[26]	CPU_DATA[26]	CPU_DATA[26]	CPU_DATA[26]	CPU_DATA[26]	CPU_DATA[26]	All
C20	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	All
C21	GND	GND	GND	GND	GND	GND	All
C22	CPU_DREQ1	CPU_DREQ1	CPU_DREQ1	CPU_DREQ1	CPU_DREQ1	CPU_DREQ1	All
C2	GND	GND	GND	GND	GND	GND	All
C3	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	All
C4	NC	NC	NC	M1_RXCLK	M1_RXCLK	M1_RXCLK	ZL50118/19/20
C5	NC	NC	NC	M1_COL	M1_COL	M1_COL	ZL50118/19/20
C6	NC	NC	NC	M1_TXER	M1_TXER	M1_TXER	ZL50118/19/20
C7	M0_RXDV	M0_RXDV	M0_RXDV	M0_RXDV	M0_RXDV	M0_RXDV	All
C8	M0_RXD[3]	M0_RXD[3]	M0_RXD[3]	M0_RXD[3]	M0_RXD[3]	M0_RXD[3]	All
C9	M0_RXD[1]	M0_RXD[1]	M0_RXD[1]	M0_RXD[1]	M0_RXD[1]	M0_RXD[1]	All
D1	NC	NC	NC	M1_RXD[1]	M1_RXD[1]	M1_RXD[1]	ZL50118/19/20
D10	M0_RXD[2]	M0_RXD[2]	M0_RXD[2]	M0_RXD[2]	M0_RXD[2]	M0_RXD[2]	All
D11	M0_REFCLK	M0_REFCLK	M0_REFCLK	M0_REFCLK	M0_REFCLK	M0_REFCLK	All
D12	M0_TXD[6]	M0_TXD[6]	M0_TXD[6]	M0_TXD[6]	M0_TXD[6]	M0_TXD[6]	All
D13	M0_TXD[1]	M0_TXD[1]	M0_TXD[1]	M0_TXD[1]	M0_TXD[1]	M0_TXD[1]	All
D14	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	All
D15	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	All
D16	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	All
D17	M0_ACTIVE_LED	M0_ACTIVE_LED	M0_ACTIVE_LED	M0_ACTIVE_LED	M0_ACTIVE_LED	M0_ACTIVE_LED	All
D18	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	All
D19	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	All
D20	CPU_DATA[25]	CPU_DATA[25]	CPU_DATA[25]	CPU_DATA[25]	CPU_DATA[25]	CPU_DATA[25]	All
D21	CPU_ADDR[23]	CPU_ADDR[23]	CPU_ADDR[23]	CPU_ADDR[23]	CPU_ADDR[23]	CPU_ADDR[23]	All
D22	CPU_DATA[6]	CPU_DATA[6]	CPU_DATA[6]	CPU_DATA[6]	CPU_DATA[6]	CPU_DATA[6]	All
D2	NC	NC	NC	M1_RXD[0]	M1_RXD[0]	M1_RXD[0]	ZL50118/19/20
D3	NC	NC	NC	M1_RXD[2]	M1_RXD[2]	M1_RXD[2]	ZL50118/19/20
D4	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	All
D5	NC	NC	NC	M1_RXDV	M1_RXDV	M1_RXDV	ZL50118/19/20
D6	M0_RXER	M0_RXER	M0_RXER	M0_RXER	M0_RXER	M0_RXER	All
D7	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	All

Table 2 - ZL50115/16/17/18/19/20 Ball Signal Assignment (continued)

Ball #	ZL50115 Signal Name	ZL50116 Signal Name	ZL50117 Signal Name	ZL50118 Signal Name	ZL50119 Signal Name	ZL50120 Signal Name	Variant
D8	M0_RXD[5]	M0_RXD[5]	M0_RXD[5]	M0_RXD[5]	M0_RXD[5]	M0_RXD[5]	All
D9	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	All
E1	NC	NC	NC	M1_RXD[3]	M1_RXD[3]	M1_RXD[3]	ZL50118/19/20
E19	CPU_DATA[30]	CPU_DATA[30]	CPU_DATA[30]	CPU_DATA[30]	CPU_DATA[30]	CPU_DATA[30]	All
E20	CPU_DATA[21]	CPU_DATA[21]	CPU_DATA[21]	CPU_DATA[21]	CPU_DATA[21]	CPU_DATA[21]	All
E21	CPU_DATA[15]	CPU_DATA[15]	CPU_DATA[15]	CPU_DATA[15]	CPU_DATA[15]	CPU_DATA[15]	All
E22	CPU_DATA[14]	CPU_DATA[14]	CPU_DATA[14]	CPU_DATA[14]	CPU_DATA[14]	CPU_DATA[14]	All
E2	M0_GIGABIT_LED	M0_GIGABIT_LED	M0_GIGABIT_LED	M0_GIGABIT_LED	M0_GIGABIT_LED	M0_GIGABIT_LED	All
E3	NC	NC	NC	M1_TXCLK	M1_TXCLK	M1_TXCLK	ZL50118/19/20
E4	NC	NC	NC	M1_RXER	M1_RXER	M1_RXER	ZL50118/19/20
F1	NC	NC	NC	NC	NC	NC	All
F19	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	All
F20	CPU_DATA[18]	CPU_DATA[18]	CPU_DATA[18]	CPU_DATA[18]	CPU_DATA[18]	CPU_DATA[18]	All
F21	CPU_DATA[17]	CPU_DATA[17]	CPU_DATA[17]	CPU_DATA[17]	CPU_DATA[17]	CPU_DATA[17]	All
F22	CPU_DATA[16]	CPU_DATA[16]	CPU_DATA[16]	CPU_DATA[16]	CPU_DATA[16]	CPU_DATA[16]	All
F2	NC	NC	NC	M1_CRS	M1_CRS	M1_CRS	ZL50118/19/20
F3	DEVICE_ID[1]	DEVICE_ID[1]	DEVICE_ID[1]	DEVICE_ID[1]	DEVICE_ID[1]	DEVICE_ID[1]	All
F4	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	All
G1	M_MDIO	M_MDIO	M_MDIO	M_MDIO	M_MDIO	M_MDIO	All
G19	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	All
G20	CPU_IREQ1	CPU_IREQ1	CPU_IREQ1	CPU_IREQ1	CPU_IREQ1	CPU_IREQ1	All
G21	CPU_DATA[11]	CPU_DATA[11]	CPU_DATA[11]	CPU_DATA[11]	CPU_DATA[11]	CPU_DATA[11]	All
G22	CPU_DATA[0]	CPU_DATA[0]	CPU_DATA[0]	CPU_DATA[0]	CPU_DATA[0]	CPU_DATA[0]	All
G2	DEVICE_ID[0]	DEVICE_ID[0]	DEVICE_ID[0]	DEVICE_ID[0]	DEVICE_ID[0]	DEVICE_ID[0]	All
G3	M0_LINKUP_LED	M0_LINKUP_LED	M0_LINKUP_LED	M0_LINKUP_LED	M0_LINKUP_LED	M0_LINKUP_LED	All
G4	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	All
H1	M_MDC	M_MDC	M_MDC	M_MDC	M_MDC	M_MDC	All
H19	CPU_DATA[10]	CPU_DATA[10]	CPU_DATA[10]	CPU_DATA[10]	CPU_DATA[10]	CPU_DATA[10]	All
H20	CPU_DATA[1]	CPU_DATA[1]	CPU_DATA[1]	CPU_DATA[1]	CPU_DATA[1]	CPU_DATA[1]	All
H21	CPU_DATA[4]	CPU_DATA[4]	CPU_DATA[4]	CPU_DATA[4]	CPU_DATA[4]	CPU_DATA[4]	All
H22	IC	IC	IC	IC	IC	IC	All
H2	GND	GND	GND	GND	GND	GND	All
H3	NC	NC	NC	NC	NC	NC	All
H4	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	All
J1	NC	NC	NC	NC	NC	NC	All
J10	GND	GND	GND	GND	GND	GND	All
J11	GND	GND	GND	GND	GND	GND	All
J12	GND	GND	GND	GND	GND	GND	All
J13	GND	GND	GND	GND	GND	GND	All
J14	GND	GND	GND	GND	GND	GND	All
J19	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	All
J20	CPU_DATA[5]	CPU_DATA[5]	CPU_DATA[5]	CPU_DATA[5]	CPU_DATA[5]	CPU_DATA[5]	All
J21	CPU_DATA[3]	CPU_DATA[3]	CPU_DATA[3]	CPU_DATA[3]	CPU_DATA[3]	CPU_DATA[3]	All

Table 2 - ZL50115/16/17/18/19/20 Ball Signal Assignment (continued)

Ball #	ZL50115 Signal Name	ZL50116 Signal Name	ZL50117 Signal Name	ZL50118 Signal Name	ZL50119 Signal Name	ZL50120 Signal Name	Variant
J22	CPU_IREQ0	CPU_IREQ0	CPU_IREQ0	CPU_IREQ0	CPU_IREQ0	CPU_IREQ0	All
J2	NC	NC	NC	NC	NC	NC	All
J3	NC	NC	NC	NC	NC	NC	All
J4	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	All
J9	GND	GND	GND	GND	GND	GND	All
K1	NC	NC	NC	NC	NC	NC	All
K10	GND	GND	GND	GND	GND	GND	All
K11	GND	GND	GND	GND	GND	GND	All
K12	GND	GND	GND	GND	GND	GND	All
K13	GND	GND	GND	GND	GND	GND	All
K14	GND	GND	GND	GND	GND	GND	All
K19	GND	GND	GND	GND	GND	GND	All
K20	CPU_DATA[2]	CPU_DATA[2]	CPU_DATA[2]	CPU_DATA[2]	CPU_DATA[2]	CPU_DATA[2]	All
K21	IC	IC	IC	IC	IC	IC	All
K22	CPU_DREQ0	CPU_DREQ0	CPU_DREQ0	CPU_DREQ0	CPU_DREQ0	CPU_DREQ0	All
K2	NC	NC	NC	NC	NC	NC	All
K3	NC	NC	NC	NC	NC	NC	All
K4	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	All
K9	GND	GND	GND	GND	GND	GND	All
L1	GND	GND	GND	GND	GND	GND	All
L10	GND	GND	GND	GND	GND	GND	All
L11	GND	GND	GND	GND	GND	GND	All
L12	GND	GND	GND	GND	GND	GND	All
L13	GND	GND	GND	GND	GND	GND	All
L14	GND	GND	GND	GND	GND	GND	All
L19	CPU_CLK	CPU_CLK	CPU_CLK	CPU_CLK	CPU_CLK	CPU_CLK	All
L20	GND	GND	GND	GND	GND	GND	All
L21	CPU_SDACK2	CPU_SDACK2	CPU_SDACK2	CPU_SDACK2	CPU_SDACK2	CPU_SDACK2	All
L22	IC_VDD_IO	IC_VDD_IO	IC_VDD_IO	IC_VDD_IO	IC_VDD_IO	IC_VDD_IO	All
L2	AUX_CLKO	AUX_CLKO	AUX_CLKO	AUX_CLKO	AUX_CLKO	AUX_CLKO	All
L3	AUX_CLKI	AUX_CLKI	AUX_CLKI	AUX_CLKI	AUX_CLKI	AUX_CLKI	All
L4	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	All
L9	GND	GND	GND	GND	GND	GND	All
M1	NC	NC	TDM_CLKI[3]	NC	NC	TDM_CLKI[3]	ZL50117/20
M10	GND	GND	GND	GND	GND	GND	All
M11	GND	GND	GND	GND	GND	GND	All
M12	GND	GND	GND	GND	GND	GND	All
M13	GND	GND	GND	GND	GND	GND	All
M14	GND	GND	GND	GND	GND	GND	All
M19	GND	GND	GND	GND	GND	GND	All
M20	CPU_TS_ALE	CPU_TS_ALE	CPU_TS_ALE	CPU_TS_ALE	CPU_TS_ALE	CPU_TS_ALE	All
M21	CPU_WE	CPU_WE	CPU_WE	CPU_WE	CPU_WE	CPU_WE	All
M22	CPU_OE	CPU_OE	CPU_OE	CPU_OE	CPU_OE	CPU_OE	All

Table 2 - ZL50115/16/17/18/19/20 Ball Signal Assignment (continued)

Ball #	ZL50115 Signal Name	ZL50116 Signal Name	ZL50117 Signal Name	ZL50118 Signal Name	ZL50119 Signal Name	ZL50120 Signal Name	Variant
M2	NC	NC	TDM_STO[3]	NC	NC	TDM_STO[3]	ZL50117/20
M3	NC	NC	TDM_STI[3]	NC	NC	TDM_STI[3]	ZL50117/20
M4	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	All
M9	GND	GND	GND	GND	GND	GND	All
N1	NC	NC	TDM_STO[2]	NC	NC	TDM_STO[2]	ZL50117/20
N10	GND	GND	GND	GND	GND	GND	All
N11	GND	GND	GND	GND	GND	GND	All
N12	GND	GND	GND	GND	GND	GND	All
N13	GND	GND	GND	GND	GND	GND	All
N14	GND	GND	GND	GND	GND	GND	All
N19	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	All
N20	CPU_ADDR[22]	CPU_ADDR[22]	CPU_ADDR[22]	CPU_ADDR[22]	CPU_ADDR[22]	CPU_ADDR[22]	All
N21	CPU_CS	CPU_CS	CPU_CS	CPU_CS	CPU_CS	CPU_CS	All
N22	CPU_ADDR[19]	CPU_ADDR[19]	CPU_ADDR[19]	CPU_ADDR[19]	CPU_ADDR[19]	CPU_ADDR[19]	All
N2	NC	NC	TDM_CLKO[3]	NC	NC	TDM_CLKO[3]	ZL50117/20
N3	NC	NC	TDM_STI[2]	NC	NC	TDM_STI[2]	ZL50117/20
N4	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	All
N9	GND	GND	GND	GND	GND	GND	All
P1	NC	NC	TDM_CLKI[2]	NC	NC	TDM_CLKI[2]	ZL50117/20
P10	GND	GND	GND	GND	GND	GND	All
P11	GND	GND	GND	GND	GND	GND	All
P12	GND	GND	GND	GND	GND	GND	All
P13	GND	GND	GND	GND	GND	GND	All
P14	GND	GND	GND	GND	GND	GND	All
P19	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	All
P20	CPU_ADDR[17]	CPU_ADDR[17]	CPU_ADDR[17]	CPU_ADDR[17]	CPU_ADDR[17]	CPU_ADDR[17]	All
P21	CPU_ADDR[18]	CPU_ADDR[18]	CPU_ADDR[18]	CPU_ADDR[18]	CPU_ADDR[18]	CPU_ADDR[18]	All
P22	CPU_ADDR[21]	CPU_ADDR[21]	CPU_ADDR[21]	CPU_ADDR[21]	CPU_ADDR[21]	CPU_ADDR[21]	All
P2	GND	GND	GND	GND	GND	GND	All
P3	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	All
P4	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	All
P9	GND	GND	GND	GND	GND	GND	All
R1	NC	NC	TDM_CLKO[2]	NC	NC	TDM_CLKO[2]	ZL50117/20
R19	GND	GND	GND	GND	GND	GND	All
R20	CPU_ADDR[11]	CPU_ADDR[11]	CPU_ADDR[11]	CPU_ADDR[11]	CPU_ADDR[11]	CPU_ADDR[11]	All
R21	CPU_ADDR[13]	CPU_ADDR[13]	CPU_ADDR[13]	CPU_ADDR[13]	CPU_ADDR[13]	CPU_ADDR[13]	All
R22	CPU_ADDR[20]	CPU_ADDR[20]	CPU_ADDR[20]	CPU_ADDR[20]	CPU_ADDR[20]	CPU_ADDR[20]	All
R2	NC	TDM_STI[1]	TDM_STI[1]	NC	TDM_STI[1]	TDM_STI[1]	ZL50116/17/19/20
R3	TDM_CLKI[0]	TDM_CLKI[0]	TDM_CLKI[0]	TDM_CLKI[0]	TDM_CLKI[0]	TDM_CLKI[0]	All
R4	NC	TDM_STO[1]	TDM_STO[1]	NC	TDM_STO[1]	TDM_STO[1]	ZL50116/17/19/20
T1	NC	TDM_CLKI[1]	TDM_CLKI[1]	NC	TDM_CLKI[1]	TDM_CLKI[1]	ZL50116/17/19/20
T19	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	All
T20	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	All

Table 2 - ZL50115/16/17/18/19/20 Ball Signal Assignment (continued)

Ball #	ZL50115 Signal Name	ZL50116 Signal Name	ZL50117 Signal Name	ZL50118 Signal Name	ZL50119 Signal Name	ZL50120 Signal Name	Variant
T21	CPU_ADDR[14]	CPU_ADDR[14]	CPU_ADDR[14]	CPU_ADDR[14]	CPU_ADDR[14]	CPU_ADDR[14]	All
T22	CPU_ADDR[16]	CPU_ADDR[16]	CPU_ADDR[16]	CPU_ADDR[16]	CPU_ADDR[16]	CPU_ADDR[16]	All
T2	NC	TDM_CLKO[1]	TDM_CLKO[1]	NC	TDM_CLKO[1]	TDM_CLKO[1]	ZL50116/17/19/20
T3	TDM_FRMI_REF	TDM_FRMI_REF	TDM_FRMI_REF	TDM_FRMI_REF	TDM_FRMI_REF	TDM_FRMI_REF	All
T4	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	All
U1	TDM_STI[0]	TDM_STI[0]	TDM_STI[0]	TDM_STI[0]	TDM_STI[0]	TDM_STI[0]	All
U19	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	All
U20	JTAG_TMS	JTAG_TMS	JTAG_TMS	JTAG_TMS	JTAG_TMS	JTAG_TMS	All
U21	CPU_ADDR[15]	CPU_ADDR[15]	CPU_ADDR[15]	CPU_ADDR[15]	CPU_ADDR[15]	CPU_ADDR[15]	All
U22	CPU_ADDR[12]	CPU_ADDR[12]	CPU_ADDR[12]	CPU_ADDR[12]	CPU_ADDR[12]	CPU_ADDR[12]	All
U2	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	All
U3	GND	GND	GND	GND	GND	GND	All
U4	TDM_CLKiS	TDM_CLKiS	TDM_CLKiS	TDM_CLKiS	TDM_CLKiS	TDM_CLKiS	All
V1	TDM_STO[0]	TDM_STO[0]	TDM_STO[0]	TDM_STO[0]	TDM_STO[0]	TDM_STO[0]	All
V19	DEVICE_ID[3]	DEVICE_ID[3]	DEVICE_ID[3]	DEVICE_ID[3]	DEVICE_ID[3]	DEVICE_ID[3]	All
V20	JTAG_TCK	JTAG_TCK	JTAG_TCK	JTAG_TCK	JTAG_TCK	JTAG_TCK	All
V21	CPU_ADDR[10]	CPU_ADDR[10]	CPU_ADDR[10]	CPU_ADDR[10]	CPU_ADDR[10]	CPU_ADDR[10]	All
V22	CPU_ADDR[9]	CPU_ADDR[9]	CPU_ADDR[9]	CPU_ADDR[9]	CPU_ADDR[9]	CPU_ADDR[9]	All
V2	TDM_CLKO[0]	TDM_CLKO[0]	TDM_CLKO[0]	TDM_CLKO[0]	TDM_CLKO[0]	TDM_CLKO[0]	All
V3	TDM_CLKO_REF	TDM_CLKO_REF	TDM_CLKO_REF	TDM_CLKO_REF	TDM_CLKO_REF	TDM_CLKO_REF	All
V4	TDM_CLKiP	TDM_CLKiP	TDM_CLKiP	TDM_CLKiP	TDM_CLKiP	TDM_CLKiP	All
W1	IC	IC	IC	IC	IC	IC	All
W10	PLL_SEC	PLL_SEC	PLL_SEC	PLL_SEC	PLL_SEC	PLL_SEC	All
W11	IC_GND	IC_GND	IC_GND	IC_GND	IC_GND	IC_GND	All
W12	GND	GND	GND	GND	GND	GND	All
W13	SYSTEM_CLK	SYSTEM_CLK	SYSTEM_CLK	SYSTEM_CLK	SYSTEM_CLK	SYSTEM_CLK	All
W14	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	All
W15	GPIO[9]	GPIO[9]	GPIO[9]	GPIO[9]	GPIO[9]	GPIO[9]	All
W16	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	All
W17	GPIO[15]	GPIO[15]	GPIO[15]	GPIO[15]	GPIO[15]	GPIO[15]	All
W18	DEVICE_ID[2]	DEVICE_ID[2]	DEVICE_ID[2]	DEVICE_ID[2]	DEVICE_ID[2]	DEVICE_ID[2]	All
W19	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	All
W20	JTAG_TDO	JTAG_TDO	JTAG_TDO	JTAG_TDO	JTAG_TDO	JTAG_TDO	All
W21	CPU_ADDR[4]	CPU_ADDR[4]	CPU_ADDR[4]	CPU_ADDR[4]	CPU_ADDR[4]	CPU_ADDR[4]	All
W22	CPU_ADDR[8]	CPU_ADDR[8]	CPU_ADDR[8]	CPU_ADDR[8]	CPU_ADDR[8]	CPU_ADDR[8]	All
W2	TDM_CLKI_REF	TDM_CLKI_REF	TDM_CLKI_REF	TDM_CLKI_REF	TDM_CLKI_REF	TDM_CLKI_REF	All
W3	TDM_FRMO_REF	TDM_FRMO_REF	TDM_FRMO_REF	TDM_FRMO_REF	TDM_FRMO_REF	TDM_FRMO_REF	All
W4	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	All
W5	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	All
W6	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	All
W7	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	All
W8	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	All
W9	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	All

Table 2 - ZL50115/16/17/18/19/20 Ball Signal Assignment (continued)

Ball #	ZL50115 Signal Name	ZL50116 Signal Name	ZL50117 Signal Name	ZL50118 Signal Name	ZL50119 Signal Name	ZL50120 Signal Name	Variant
Y1	IC	IC	IC	IC	IC	IC	All
Y10	IC	IC	IC	IC	IC	IC	All
Y11	IC_GND	IC_GND	IC_GND	IC_GND	IC_GND	IC_GND	All
Y12	IC	IC	IC	IC	IC	IC	All
Y13	GND	GND	GND	GND	GND	GND	All
Y14	GND	GND	GND	GND	GND	GND	All
Y15	GPIO[8]	GPIO[8]	GPIO[8]	GPIO[8]	GPIO[8]	GPIO[8]	All
Y16	GPIO[14]	GPIO[14]	GPIO[14]	GPIO[14]	GPIO[14]	GPIO[14]	All
Y17	TEST_MODE[1]	TEST_MODE[1]	TEST_MODE[1]	TEST_MODE[1]	TEST_MODE[1]	TEST_MODE[1]	All
Y18	JTAG_TRST	JTAG_TRST	JTAG_TRST	JTAG_TRST	JTAG_TRST	JTAG_TRST	All
Y19	IC_GND	IC_GND	IC_GND	IC_GND	IC_GND	IC_GND	All
Y20	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	All
Y21	GND	GND	GND	GND	GND	GND	All
Y22	CPU_ADDR[7]	CPU_ADDR[7]	CPU_ADDR[7]	CPU_ADDR[7]	CPU_ADDR[7]	CPU_ADDR[7]	All
Y2	GND	GND	GND	GND	GND	GND	All
Y3	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	All
Y4	IC	IC	IC	IC	IC	IC	All
Y5	IC	IC	IC	IC	IC	IC	All
Y6	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	All
Y7	IC	IC	IC	IC	IC	IC	All
Y8	IC	IC	IC	IC	IC	IC	All
Y9	PLL_PRI	PLL_PRI	PLL_PRI	PLL_PRI	PLL_PRI	PLL_PRI	All
AA1	IC	IC	IC	IC	IC	IC	All
AA10	IC	IC	IC	IC	IC	IC	All
AA11	SYSTEM_DEBUG	SYSTEM_DEBUG	SYSTEM_DEBUG	SYSTEM_DEBUG	SYSTEM_DEBUG	SYSTEM_DEBUG	All
AA12	SYSTEM_RST	SYSTEM_RST	SYSTEM_RST	SYSTEM_RST	SYSTEM_RST	SYSTEM_RST	All
AA13	GPIO[1]	GPIO[1]	GPIO[1]	GPIO[1]	GPIO[1]	GPIO[1]	All
AA14	GPIO[2]	GPIO[2]	GPIO[2]	GPIO[2]	GPIO[2]	GPIO[2]	All
AA15	GPIO[7]	GPIO[7]	GPIO[7]	GPIO[7]	GPIO[7]	GPIO[7]	All
AA16	GPIO[12]	GPIO[12]	GPIO[12]	GPIO[12]	GPIO[12]	GPIO[12]	All
AA17	TEST_MODE[0]	TEST_MODE[0]	TEST_MODE[0]	TEST_MODE[0]	TEST_MODE[0]	TEST_MODE[0]	All
AA18	JTAG_TDI	JTAG_TDI	JTAG_TDI	JTAG_TDI	JTAG_TDI	JTAG_TDI	All
AA19	IC_GND	IC_GND	IC_GND	IC_GND	IC_GND	IC_GND	All
AA20	GND	GND	GND	GND	GND	GND	All
AA21	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	All
AA22	CPU_ADDR[6]	CPU_ADDR[6]	CPU_ADDR[6]	CPU_ADDR[6]	CPU_ADDR[6]	CPU_ADDR[6]	All
AA2	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	All
AA3	GND	GND	GND	GND	GND	GND	All
AA4	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	All
AA5	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO	All
AA6	IC	IC	IC	IC	IC	IC	All
AA7	GND	GND	GND	GND	GND	GND	All
AA8	A1VDD_PLL1	A1VDD_PLL1	A1VDD_PLL1	A1VDD_PLL1	A1VDD_PLL1	A1VDD_PLL1	All

Table 2 - ZL50115/16/17/18/19/20 Ball Signal Assignment (continued)