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Features

- Independent multiple channels of echo cancellation; from 32 channels of 64 ms to 16 channels of 128 ms with the ability to mix channels at 128 ms or 64 ms in any combination
- Independent Power Down mode for each group of 2 channels for power management
- Fully compliant to ITU-T G.165, G.168 (2000) and (2002) specifications
- Passed all AT&T voice quality tests for carrier grade echo canceller.
- Compatible to ST-BUS and GCI interface at 2 Mbps serial PCM
- PCM coding, μ /A-Law ITU-T G.711 or sign magnitude
- Per channel Fax/Modem G.164 2100 Hz or G.165 2100 Hz phase reversal Tone Disable
- Per channel echo canceller parameters control
- Transparent data transfer and mute
- Fast reconvergence on echo path changes
- Fully programmable convergence speeds
- Patented Advanced Non-Linear Processor with high quality subjective performance
- Protection against narrow band signal divergence and instability in high echo environments

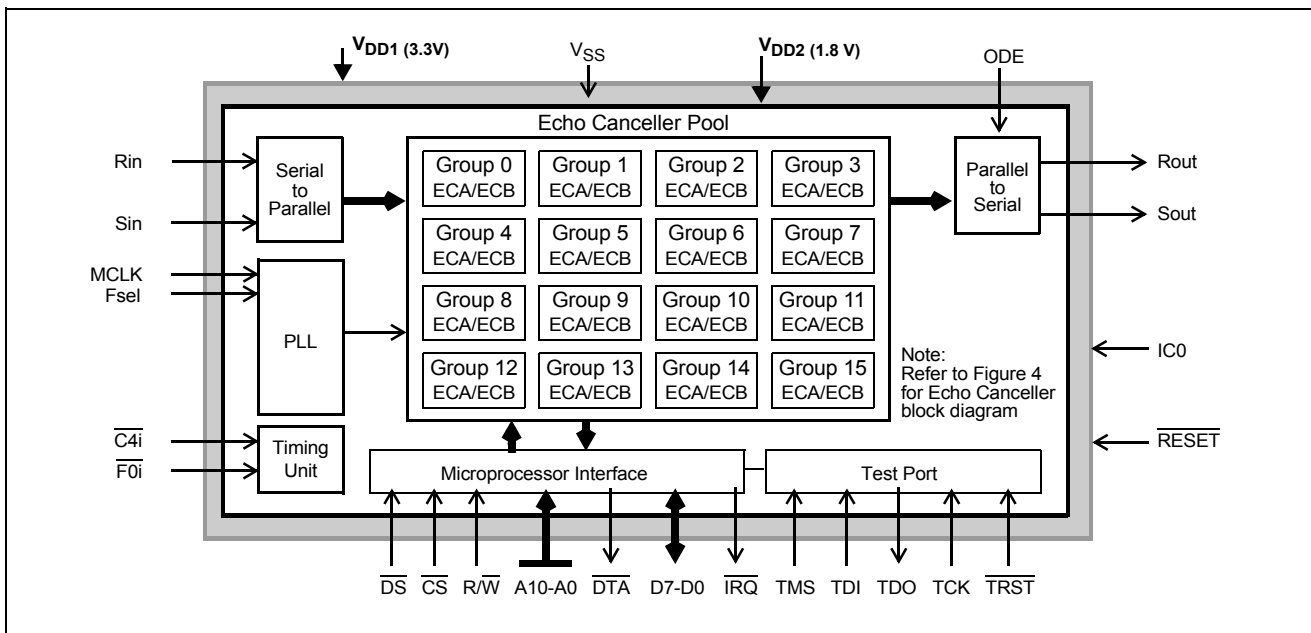
Ordering Information

ZL50232/QCC	100 Pin LQFP	Trays
ZL50232/GDC	208 Ball PBGA	Trays
ZL50232/QCG1	100 Pin LQFP*	Trays, Bake & Drypack
ZL50232/GDG2	208 Ball PBGA**	Trays
*Pb Free Matte Tin		
**Pb Free Tin/Silver/Copper		
-40°C to +85°C		

- +9 dB to -12 dB level adjusters (3 dB steps) at all signal ports
- Offset nulling of all PCM channels
- 10 MHz or 20 MHz master clock operation
- 3.3 V pads and 1.8 V Logic core operation with 5 V tolerant inputs
- IEEE-1149.1 (JTAG) Test Access Port

Applications

- Voice over IP network gateways
- Voice over ATM, Frame Relay
- T1/E1/J1 multichannel echo cancellation
- Wireless base stations
- Echo Canceller pools
- DCME, satellite and multiplexer system


Figure 1 - ZL50232 Device Overview

Description

The ZL50232 Voice Echo Canceller implements a cost effective solution for telephony voice-band echo cancellation conforming to ITU-T G.168 requirements. The ZL50232 architecture contains 16 groups of two echo cancellers (ECA and ECB) which can be configured to provide two channels of 64 milliseconds or one channel of 128 milliseconds echo cancellation. This provides 32 channels of 64 milliseconds to 16 channels of 128 milliseconds echo cancellation or any combination of the two configurations. The ZL50232 supports ITU-T G.165 and G.164 tone disable requirements

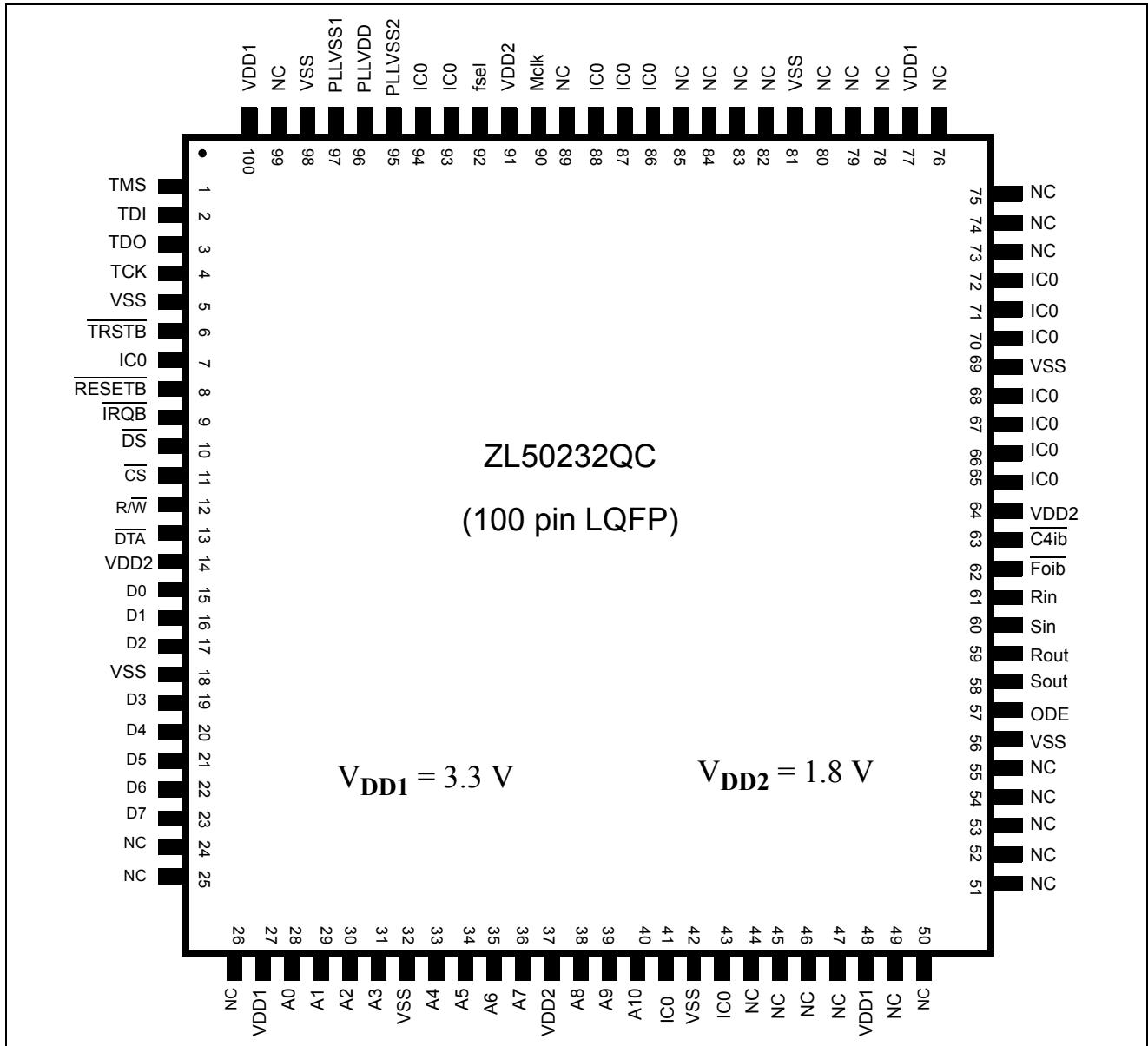


Figure 2 - 100 Pin LQFP

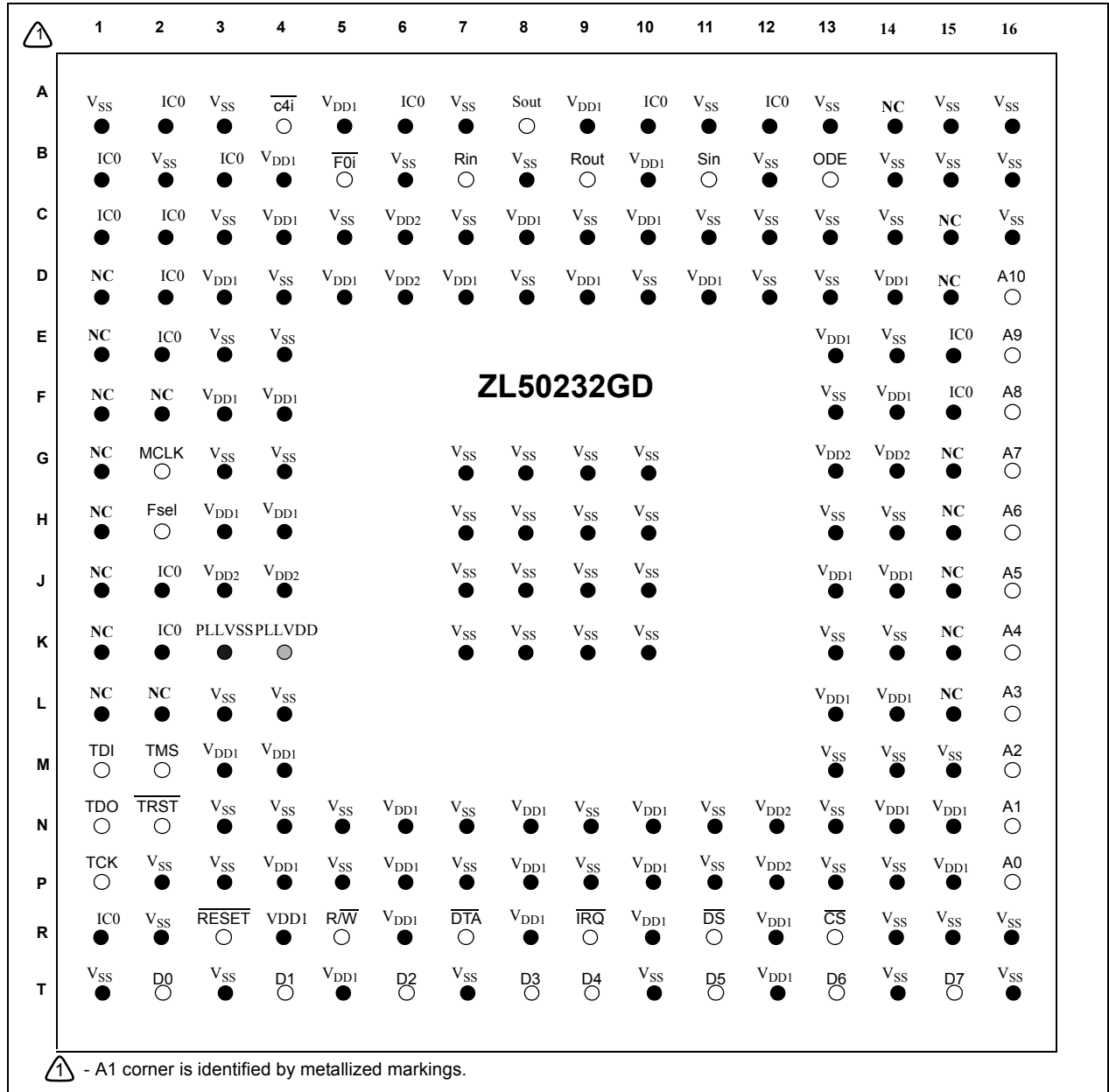


Figure 3 - 208 Ball LPGA

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1.0 Change Summary

Changes from September 2005 Issue to March 2006 Issue. Page, section, figure and table numbers refer to this current issue.

Page	Item	Change
1		Updated Ordering Information

Pin Description

Pin Name	Pin #		Description
	208-Ball LBGA	100 Pin LQFP	
V_{SS}	A1, A3,A7,A11, A13, A15, A16, B2, B6, B8, B12, B14, B15, B16, C3, C5, C7, C9, C11, C12, C13, C14, C16, D4, D8, D10, D12, D13, E3, E4, E14, F13, G3, G4, G7, G8, G9, G10, H7, H8, H9, H10, H13, H14, J7, J8, J9, J10, K7, K8, K9, K10, K13, K14, L3, L4, M13, M14, M15, N3, N4, N5, N7, N9, N11, N13, P2, P3, P5, P7, P9.P11, P13, P14, R2, R14, R15, R16, T1, T3, T7, T10, T14, T16	5, 18, 32, 42, 56, 69, 81, 98	Ground.
V_{DD1}	A5, A9, B10, C4, C8, B4, C10, D3, D5, D7, D9, D11, D14, E13, F3, F4, F14, H3, H4, J13, J14, L13, L14, M3, M4, N6, N8, N10, N14, N15, P4, P6, P8, P10, P15, R4, R6, R8, R10, R12, T5, T12	27, 48, 77, 100	Positive Power Supply. Nominally 3.3 V (I/O Voltage).
V_{DD2}	C6, D6, J3, J4, N12, P12, G13, G14	14, 37, 64, 91	Positive Power Supply. Nominally 1.8 V (Core Voltage).
IC0	E15, F15, A12, A10, A6, A2, B1, B3, C1, C2, D2, E2, J2, K2, R1	7, 41, 43, 65, 66, 67, 68, 70, 71, 72, 86, 87, 88, 93, 94	Internal Connection. These pins must be connected to V _{SS} for normal operation.

Pin Description (continued)

Pin Name	Pin #		Description
	208-Ball LBGA	100 Pin LQFP	
NC	A14, C15, D1, D15, E1, F1, G1, G15, H1, H15, J1, J15, K1, K15, L1, L15, F2, L2	24, 25, 26, 44, 45, 46, 47, 49, 51, 52, 53, 54, 55, 73, 74, 75, 76, 78, 79, 80, 82, 83, 84, 85, 89, 99, 50	No connection. These pins must be left open for normal operation.
IRQ	R9	9	Interrupt Request (Open Drain Output). This output goes low when an interrupt occurs in any channel. IRQ returns high when all the interrupts have been read from the Interrupt FIFO Register. A pull-up resistor (1 K typical) is required at this output.
DS	R11	10	Data Strobe (Input). This active low input works in conjunction with CS to enable the read and write operations.
CS	R13	11	Chip Select (Input). This active low input is used by a microprocessor to activate the microprocessor port.
R/W	R5	12	Read/Write (Input). This input controls the direction of the data bus lines (D7-D0) during a microprocessor access.
DTA	R7	13	Data Transfer Acknowledgment (Open Drain Output). This active low output indicates that a data bus transfer is completed. A pull-up resistor (1 K typical) is required at this output.
D0..D7	T2, T4, T6, T8, T9, T11, T13, T15	15, 16, 17, 19, 20, 21, 22, 23	Data Bus D0 - D7 (Bidirectional). These pins form the 8 bit bidirectional data bus of the microprocessor port.
A0..A10	P16, N16, M16, L16, K16, J16, H16, G16, F16, E16, D16	28, 29, 30, 31, 33, 34, 35, 36, 38, 39, 40	Address A0 to A10 (Input). These inputs provide the A10 - A0 address lines to the internal registers.
ODE	B13	57	Output Drive Enable (Input). This input pin is logically AND'd with the ODE bit-6 of the Main Control Register. When both ODE bit and ODE input pin are high, the Rout and Sout ST-BUS outputs are enabled. When the ODE bit is low or the ODE input pin is low, the Rout and Sout ST-BUS outputs are high impedance.
Sout	A8	58	Send PCM Signal Output (Output). Port 1 TDM data output streams. Sout pin outputs serial TDM data streams at 2.048 Mbps with 32 channels per stream.
Rout	B9	59	Receive PCM Signal Output (Output). Port 2 TDM data output streams. Rout pin outputs serial TDM data streams at 2.048 Mbps with 32 channels per stream.
Sin	B11	60	Send PCM Signal Input (Input). Port 2 TDM data input streams. Sin pin receives serial TDM data streams at 2.048 Mbps with 32 channels per stream.

Pin Description (continued)

Pin Name	Pin #		Description
	208-Ball LBGA	100 Pin LQFP	
Rin	B7	61	Receive PCM Signal Input (Input). Port 1 TDM data input streams. Rin pin receives serial TDM data streams at 2.048 Mbps with 32 channels per stream.
$\overline{F0i}$	B5	62	Frame Pulse (Input). This input accepts and automatically identifies frame synchronization signals formatted according to ST-BUS or GCI interface specifications.
$\overline{C4i}$	A4	63	Serial Clock (Input). 4.096 MHz serial clock for shifting data in/out on the serial streams (Rin, Sin, Rout, Sout).
MCLK	G2	90	Master Clock (Input). Nominal 10 MHz or 20 MHz Master Clock input. May be connected to an asynchronous (relative to frame signal) clock source.
Fsel	H2	92	Frequency select (Input). This input selects the Master Clock frequency operation. When Fsel pin is low, nominal 19.2 MHz Master Clock input must be applied. When Fsel pin is high, nominal 9.6 MHz Master Clock input must be applied.
PLLVss1 PLLVss2	K3	97, 95	PLL Ground. Must be connected to V_{SS}
PLLV _{DD}	K4	96	PLL Power Supply. Must be connected to $V_{DD2} = 1.8 V$
TMS	M2	1	Test Mode Select (3.3 V Input). JTAG signal that controls the state transitions of the TAP controller. This pin is pulled high by an internal pull-up when not driven.
TDI	M1	2	Test Serial Data In (3.3 V Input). JTAG serial test instructions and data are shifted in on this pin. This pin is pulled high by an internal pull-up when not driven.
TDO	N1	3	Test Serial Data Out (Output). JTAG serial data is output on this pin on the falling edge of TCK. This pin is held in high impedance state when JTAG scan is not enabled.
TCK	P1	4	Test Clock (3.3 V Input). Provides the clock to the JTAG test logic.
\overline{TRST}	N2	6	Test Reset (3.3 V Input). Asynchronously initializes the JTAG TAP controller by putting it in the Test-Logic-Reset state. This pin should be pulsed low on power-up or held low, to ensure that the ZL50232 is in the normal functional mode. This pin is pulled by an internal pull-down when not driven.
\overline{RESET}	R3	8	Device Reset (Schmitt Trigger Input). An active low resets the device and puts the ZL50232 into a low-power stand-by mode. When the \overline{RESET} pin is returned to logic high and a clock is applied to the MCLK pin, the device will automatically execute initialization routines, which preset all the Main Control and Status Registers to their default power-up values.

2.0 Device Overview

The ZL50232 architecture contains 32 echo cancellers divided into 16 groups. Each group has two echo cancellers, Echo Canceller A and Echo Canceller B. Each group can be configured in Normal, Extended Delay or Back-to-Back configurations. In **Normal configuration**, a group of echo cancellers provides two channels of 64 ms echo cancellation, which run independently on different channels. In **Extended Delay** configuration, a group of echo cancellers achieves 128 ms of echo cancellation by cascading the two echo cancellers (A & B). In **Back-to-Back** configuration, the two echo cancellers from the same group are positioned to cancel echo coming from both directions in a single channel, providing full-duplex 64 ms echo cancellation.

Each echo canceller contains the following main elements (see Figure 4).

- Adaptive Filter for estimating the echo channel
- Subtractor for cancelling the echo
- Double-Talk detector for disabling the filter adaptation during periods of double-talk
- Path Change detector for fast reconvergence on major echo path changes
- Instability Detector to combat instability in very low ERL environments
- Patented Advanced Non-Linear Processor for suppression of residual echo, with comfort noise injection
- Disable Tone Detectors for detecting valid disable tones at send and receive path inputs
- Narrow-Band Detector for preventing Adaptive Filter divergence from narrow-band signals
- Offset Null filters for removing the DC component in PCM channels
- +9 to -12 dB level adjusters at all signal ports
- Parallel controller interface compatible with Motorola microcontrollers
- PCM encoder/decoder compatible with μ /A-Law ITU-T G.711 or Sign-Magnitude coding

Each echo canceller in the ZL50232 has four functional states: *Mute*, *Bypass*, *Disable Adaptation* and *Enable Adaptation*. These are explained in the section entitled Echo Canceller Functional States.

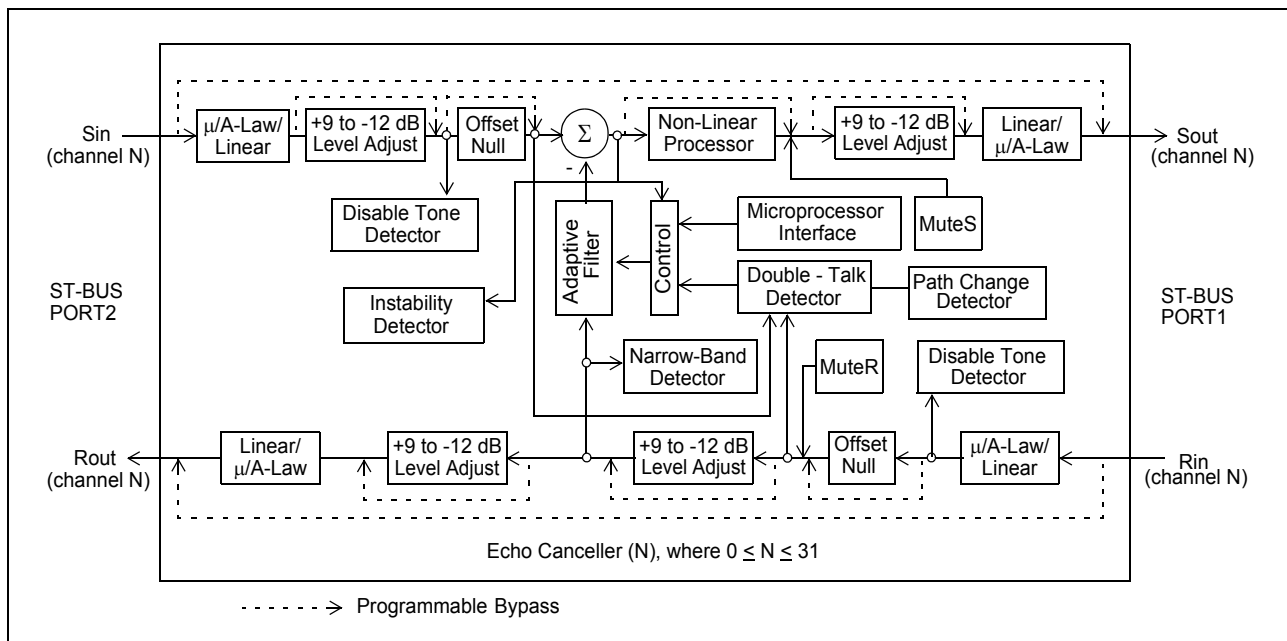


Figure 4 - Functional Block Diagram

2.1 Adaptive Filter

The adaptive filter adapts to the echo path and generates an estimate of the echo signal. This echo estimate is then subtracted from S_{in} . For each group of echo cancellers, the adaptive filter is a 1024 tap FIR adaptive filter which is divided into two sections. Each section contains 512 taps providing 64 ms of echo estimation. In **Normal configuration**, the first section is dedicated to channel A and the second section to channel B. In **Extended Delay configuration**, both sections are cascaded to provide 128 ms of echo estimation in channel A. In **Back-to Back configuration**, the first section is used in the receive direction and the second section is used in the transmit direction for the same channel.

2.2 Double-Talk Detector

Double-Talk is defined as those periods of time when signal energy is present in both directions simultaneously. When this happens, it is necessary to disable the filter adaptation to prevent divergence of the Adaptive Filter coefficients. Note that when double-talk is detected, the adaptation process is halted but the echo canceller continues to cancel echo using the previous converged echo profile. A double-talk condition exists whenever the relative signal levels of R_{in} (L_{rin}) and S_{in} (L_{sin}) meet the following condition:

$$L_{sin} > L_{rin} + 20\log_{10}(DTDT)$$

where DTDT is the Double-Talk Detection Threshold. L_{sin} and L_{rin} are signal levels expressed in dBm0.

A different method is used when it is uncertain whether S_{in} consists of a low level double-talk signal or an echo return. During these periods, the adaptation process is slowed down but it is not halted. The slow convergence speed is set using the Slow sub-register in Control Register 4. During slow convergence, the adaptation speed is reduced by a factor of 2^{Slow} relative to normal convergence for non-zero values of Slow. If Slow equals zero, adaptation is halted completely.

In the G.168 standard, the echo return loss is expected to be at least 6 dB. This implies that the Double-Talk Detector Threshold (DTDT) should be set to 0.5 (-6 dB). However, in order to achieve additional guardband, the DTDT is set internally to 0.5625 (-5 dB).

In some applications the return loss can be higher or lower than 6 dB. The ZL50232 allows the user to change the detection threshold to suit each application's need. This threshold can be set by writing the desired threshold value into the DTDT register.

The DTDT register is 16 bits wide. The register value in hexadecimal can be calculated with the following equation:

$$DTDT_{(hex)} = hex(DTDT_{(dec)} * 32768)$$

where $0 < DTDT_{(dec)} < 1$

Example: For DTDT = 0.5625 (-5 dB), the

hexadecimal value becomes

$$hex(0.5625 * 32768) = 4800_{hex}$$

2.3 Path Change Detector

Integrated into the ZL50232 is a Path Change Detector. This permits fast reconvergence when a major change occurs in the echo channel. Subtle changes in the echo channel are also tracked automatically once convergence is achieved, but at a much slower speed.

The Path Change Detector is activated by setting the PathDet bit in Control Register 3 to "1". An optional path clearing feature can be enabled by setting the PathClr bit in Control Register 3 to "1". With path clearing turned on,

the existing echo channel estimate will also be cleared (i.e. the adaptive filter will be filled with zeroes) upon detection of a major path change.

2.4 Non-Linear Processor (NLP)

After echo cancellation, there is always a small amount of residual echo which may still be audible. The ZL50232 uses **Zarlink's patented Advanced NLP** to remove residual echo signals which have a level lower than the Adaptive Suppression Threshold (TSUP in G.168). This threshold depends upon the level of the Rin (Lrin) reference signal as well as the programmed value of the Non-Linear Processor Threshold register (NLPTHR). TSUP can be calculated by the following equation:

$$TSUP = Lrin + 20\log_{10}(NLPTHR)$$

where NLPTHR is the Non-Linear Processor Threshold register value and Lrin is the relative power level expressed in dBm0. The NLPTHR register is 16 bits wide. The register value in hexadecimal can be calculated with the following equation:

$$NLPTHR_{(hex)} = hex(NLPTHR_{(dec)} * 32768)$$

where $0 < NLPTHR_{(dec)} < 1$

When the level of residual error signal falls below TSUP, the NLP is activated further attenuating the residual signal by an additional 30 dB. To prevent a perceived decrease in background noise due to the activation of the NLP, a spectrally-shaped comfort noise, equivalent in power level to the background noise, is injected. This keeps the perceived noise level constant. Consequently, the user does not hear the activation and de-activation of the NLP.

The NLP processor can be disabled by setting the NLPDis bit to "1" in Control Register 2.

The comfort noise injector can be disabled by setting the INJDis bit to "1" in Control Register 1. It should be noted that the NLPTHR is valid and the comfort noise injection is active only when the NLP is enabled.

The patented Advanced NLP provides a number of new and improved features over the original NLP found in previous generation devices. Differences between the Advanced NLP and the original NLP are summarized in Table 1.

Feature	Register or Bit(s)	Advanced NLP Default Value	Original NLP Default Value
NLP Selection	NLPSEL (Control Register 3)	1	0 (feature not supported)
Reject uncanceled echo as noise	NLRun1 (Control Register 3)	1	0 (feature not supported)
Reject double-talk as noise	NLRun2 (Control Register 3)	1	0 (feature not supported)
Noise level estimate or ramping scheme	InjCtrl (Control Register 3)	1	0 (feature not supported)
Noise level ramping rate	NLInc (Noise Control)	5(hex)	C(hex)
Noise level scaling	Noise Scaling	16(hex)	74(hex)

Table 1 - Comparison of NLP Types

The NLPSEL bit in Control Register 3 selects which NLP is used. A "1" will select the Advanced NLP, "0" selects the original NLP.

The Advanced NLP uses a new noise ramping scheme to quickly and more accurately estimate the background noise level. The noise ramping method of the original NLP can also be used. The InjCtrl bit in Control Register 3 selects the ramping scheme.

The NLInc sub-register in Noise Control is used to set the ramping speed. When InjCtrl = 1 (such as with the Advanced NLP), a lower value will give faster ramping. When InjCtrl = 0 (such as with the original NLP), a higher value will give faster ramping. NLInc is a 4-bit value, so only values from 0 to F(hex) are valid.

The Noise Scaling register can be used to adjust the relative volume of the comfort noise. Lowering this value will scale the injected noise level down, conversely, raising the value will scale the comfort noise up. Due to differences in the noise estimator operation, the Advanced NLP requires a different scaling value than the original NLP.

IMPORTANT NOTE: NLInc and the Noise Scaling register have been pre-programmed with G.168 compliant values. Changing these values may result in undesirable comfort noise performance!

The Advanced NLP also contains safeguards to prevent double-talk and uncanceled echo from being mistaken for background noise. These features were not present in the original NLP. They can be disabled by setting the NLRun1 and NLRun2 bits in Control Register 3 to “0”.

2.5 Disable Tone Detector

The G.165 recommendation defines the disable tone as having the following characteristics: 2100 Hz (± 21 Hz) sine wave, a power level between -6 to -31 dBm0, and a phase reversal of 180 degrees (± 25 degrees) every 450 ms (± 25 ms). If the disable tone is present for a minimum of one second with at least one phase reversal, the Tone Detector will trigger.

The G.164 recommendation defines the disable tone as a 2100 Hz (± 21 Hz) sine wave with a power level between 0 to -31 dBm0. If the disable tone is present for a minimum of 400 ms, with or without phase reversal, the Tone Detector will trigger.

The ZL50232 has two Tone Detectors per channels (for a total of 64) in order to monitor the occurrence of a valid disable tone on both Rin and Sin. Upon detection of a disable tone, TD bit of the Status Register will indicate logic high and an interrupt is generated (i.e., $\overline{\text{IRQ}}$ pin low). Refer to Figure 5 and to the **Interrupts** section.

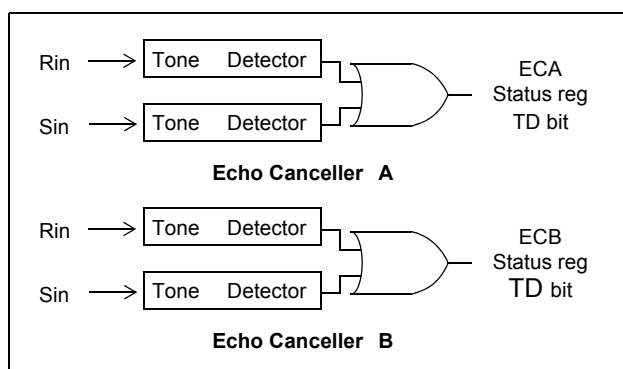


Figure 5 - Disable Tone Detection

Once a Tone Detector has been triggered, there is no longer a need for a valid disable tone (G.164 or G.165) to maintain Tone Detector status (i.e. TD bit high). The Tone Detector status will only release (i.e. TD bit low) if the signals Rin and Sin fall below -30 dBm0, in the frequency range of 390 Hz to 700 Hz, and below -34 dBm0, in the frequency range of 700 Hz to 3400 Hz, for at least 400 ms. Whenever a Tone Detector releases, an interrupt is generated (i.e. $\overline{\text{IRQ}}$ pin low).

The selection between G.165 and G.164 tone disable is controlled by the PHDis bit in Control Register 2 on a per channel basis. When the PHDis bit is set to “1”, G.164 tone disable requirements are selected.

In response to a valid disable tone, the echo canceller must be switched from the Enable Adaptation state to the Bypass state. This can be done in two ways, automatically or externally. In automatic mode, the Tone Detectors internally control the switching between Enable Adaptation and Bypass states. The automatic mode is activated by setting the AutoTD bit in Control Register 2 to high. In external mode, an external controller is needed to service the interrupts and poll the TD bits in the Status Registers. Following the detection of a disable tone (TD bit high) on a given channel, the external controller must switch the echo canceller from Enable Adaptation to Bypass state.

2.6 Instability Detector

In systems with very low echo channel return loss (ERL), there may be enough feedback in the loop to cause stability problems in the adaptive filter. This instability can result in variable pitched ringing or oscillation. Should this ringing occur, the Instability Detector will activate and suppress the oscillations.

The Instability Detector is activated by setting the RingClr bit in Control Register 3 to “1”.

2.7 Narrow Band Signal Detector (NBSD)

Single or dual frequency tones (i.e., DTMF tones) present in the receive input (Rin) of the echo canceller for a prolonged period of time may cause the Adaptive Filter to diverge. The Narrow Band Signal Detector (NBSD) is designed to prevent this by detecting single or dual tones of arbitrary frequency, phase, and amplitude. When narrow band signals are detected, adaptation is halted but the echo canceller continues to cancel echo.

The NBSD will be active regardless of the Echo Canceller functional state. However the NBSD can be disabled by setting the NBDIs bit to “1” in Control Register 2.

2.8 Offset Null Filter

Adaptive filters in general do not operate properly when a DC offset is present at any input. To remove the DC component, the ZL50232 incorporates Offset Null filters in both Rin and Sin inputs.

The offset null filters can be disabled by setting the HPFDis bit to “1” in Control Register 2.

2.9 Adjustable Level Pads

The ZL50232 provides adjustable level pads at Rin, Rout, Sin and Sout. This setup allows signal strength to be adjusted both inside and outside the echo path. Each signal level may be independently scaled with anywhere from +9 dB to -12 dB level, in 3 dB steps. Level values are set using the Gains register.

CAUTION: Gain adjustment can help interface the ZL50232 to a particular system in order to provide optimum echo cancellation, but it can also degrade performance if not done carefully. Excessive loss may cause low signal levels and slow convergence. Exercise great care when adjusting these values. Also, due to internal signal routings in Back to Back mode, it is not recommended that gain adjustments be used on Rin or Sout in this mode.

The -12 dB PAD bit in Control Register 1 is still supported as a legacy feature. Setting this bit will provide 12 dB of attenuation at Rin, and override the values in the Gains register.

2.10 ITU-T G.168 Compliance

The ZL50232 has been certified G.168 (1997), (2000) and (2002) compliant in all 64 ms cancellation modes (i.e. Normal and Back-to-Back configurations) by in-house testing with the DSPG ECT-1 echo canceller tester.

The ZL50232 has also been tested for G.168 compliance and all voice quality tests at AT&T Labs. The ZL50232 was classified as “carrier grade” echo canceller.

3.0 Device Configuration

The ZL50232 architecture contains 32 echo cancellers divided into 16 groups. Each group has two echo cancellers which can be individually controlled (Echo Cancellor A (ECA) and Echo Cancellor B (ECB)). They can be set in three distinct configurations: **Normal**, **Back-to-Back**, and **Extended Delay**. See Figures 6, 7, and 8.

3.1 Normal Configuration

In Normal configuration, the two echo cancellers (Echo Cancellor A and B) are positioned in parallel, as shown in Figure 6, providing 64 milliseconds of echo cancellation in two channels simultaneously.

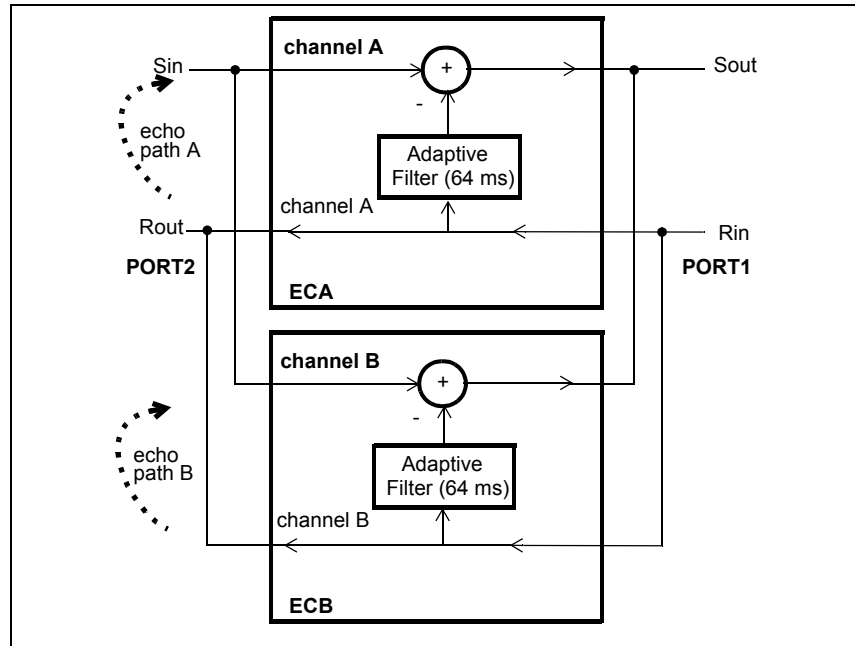


Figure 6 - Normal Device Configuration (64 ms)

3.2 Back-to-Back Configuration

In Back-to-Back configuration, the two echo cancellers from the same group are positioned to cancel echo coming from both directions in a single channel providing full-duplex 64 ms echo cancellation. See Figure 7. This configuration uses only one timeslot on PORT1 and PORT2 and the second timeslot normally associated with ECB contains zero code. Back-to-Back configuration allows a no-glue interface for applications where bidirectional echo cancellation is required.

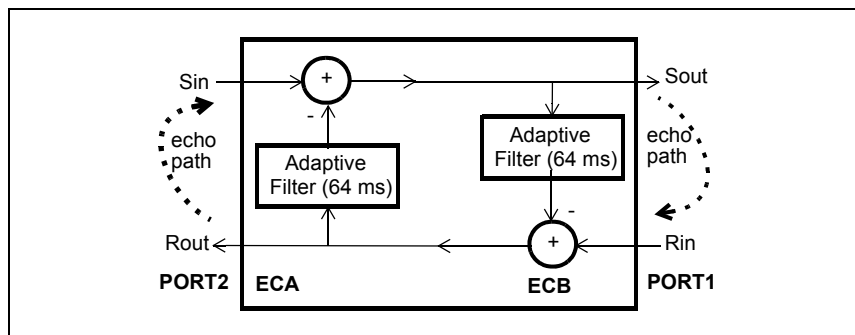


Figure 7 - Back-to-Back Device Configuration (64 ms)

Back-to-Back configuration is selected by writing a “1” into the BBM bit of Control Register 1 for **both** Echo Canceller A and Echo Canceller B for a given group of echo canceller. Table 4 shows the 16 groups of 2 cancellers that can be configured into Back-to-Back.

Examples of Back-to-Back configuration include positioning one group of echo cancellers between a codec and a transmission device or between two codecs for echo control on analog trunks.

3.3 Extended Delay Configuration

In this configuration, the two echo cancellers from the same group are internally cascaded into one 128 milliseconds echo canceller. See Figure 8. This configuration uses only one timeslot on PORT1 and PORT2 and the second timeslot normally associated with ECB contains quiet code.

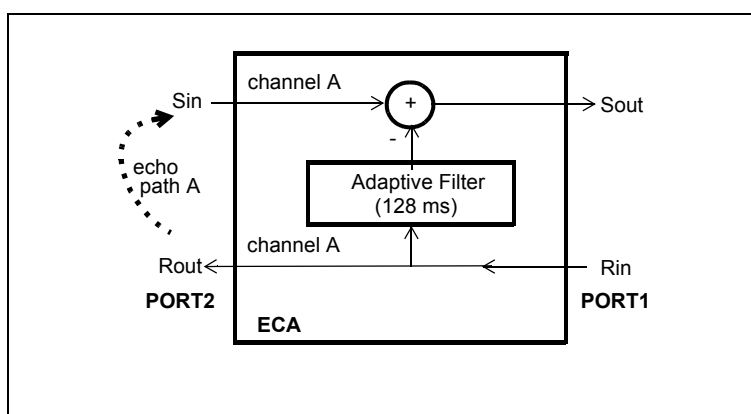


Figure 8 - Extended Delay Configuration (128 ms)

Extended Delay configuration is selected by writing a “1” into the ExtDI bit in Echo Canceller A, Control Register 1. For a given group, only Echo Canceller A, Control Register 1, has the ExtDI bit. For Echo Canceller B Control Register 1, Bit 0 must always be set to zero.

Table 4 shows the 16 groups of 2 cancellers that can each be configured into 64 ms or 128 ms echo tail capacity.

4.0 Echo Canceller Functional States

Each echo canceller has four functional states: **Mute**, **Bypass**, **Disable Adaptation** and **Enable Adaptation**.

4.1 Mute

In Normal and in Extended Delay configurations, writing a “1” into the MuteR bit replaces Rin with quiet code which is applied to both the Adaptive Filter and Rout. Writing a “1” into the MuteS bit replaces the Sout PCM data with quiet code.

	LINEAR 16 bits 2's complement	SIGN/ MAGNITUDE μ -Law A-Law	CCITT (G.711)	
			μ -Law	A-Law
+Zero (quiet code)	0000 _{hex}	80 _{hex}	FF _{hex}	D5 _{hex}

Table 2 - Quiet PCM Code Assignment

In Back-to-Back configuration, writing a “1” into the MuteR bit of Echo Canceller A, Control Register 2, causes quiet code to be transmitted on Rout. Writing a “1” into the MuteS bit of Echo Canceller A, Control Register 2, causes quiet code to be transmitted on Sout.

In Extended Delay and in Back-to-Back configurations, MuteR and MuteS bits of Echo Canceller B must always be “0”. Refer to Figure 4 and to Control Register 2 for bit description.

4.2 Bypass

The Bypass state directly transfers PCM codes from Rin to Rout and from Sin to Sout. **When Bypass state is selected, the Adaptive Filter coefficients are reset to zero.** Bypass state must be selected for at least one frame (125 μ s) in order to properly clear the filter.

4.3 Disable Adaptation

When the Disable Adaptation state is selected, the Adaptive Filter coefficients are frozen at their current value. The adaptation process is halted, however, the echo canceller continues to cancel echo.

4.4 Enable Adaptation

In Enable Adaptation state, the Adaptive Filter coefficients are continually updated. This allows the echo canceller to model the echo return path characteristics in order to cancel echo. This is the normal operating state.

The echo canceller functions are selected in Control Register 1 and Control Register 2 through four control bits: MuteS, MuteR, Bypass and AdaptDis. Refer to the Registers Description for details.

5.0 ZL50232 Throughput Delay

The throughput delay of the ZL50232 varies according to the device configuration. For all device configurations, Rin to Rout has a delay of two frames and Sin to Sout has a delay of three frames. In Bypass state, the Rin to Rout and Sin to Sout paths have a delay of two frames.

6.0 Serial PCM I/O channels

There are two sets of TDM I/O streams, each with channels numbered from 0 to 31. One set of input streams is for Receive (Rin) channels, and the other set of input streams is for Send (Sin) channels. Likewise, one set of output streams is for Rout PCM channels, and the other set is for Sout channels. See Figure 9 for channel allocation.

The arrangement and connection of PCM channels to each echo canceller is a 2 port I/O configuration for each set of PCM Send and Receive channels, as illustrated in Figure 4.

6.1 Serial Data Interface Timing

The ZL50232 provides ST-BUS and GCI interface timing. The Serial Interface clock frequency, $\overline{C4i}$, is 4.096 MHz. The input and output data rate of the ST-BUS and GCI bus is 2.048 Mbps.

The 8 KHz input frame pulse can be in either ST-BUS or GCI format. The ZL50232 automatically detects the presence of an input frame pulse and identifies it as either ST-BUS or GCI. In ST-BUS format, every second falling edge of the $\overline{C4i}$ clock marks a bit boundary, and the data is clocked in on the rising edge of $\overline{C4i}$, three quarters of the way into the bit cell (See Figure 12). In GCI format, every second rising edge of the $\overline{C4i}$ clock marks the bit boundary, and data is clocked in on the second falling edge of $\overline{C4i}$, half the way into the bit cell (see Figure 13).

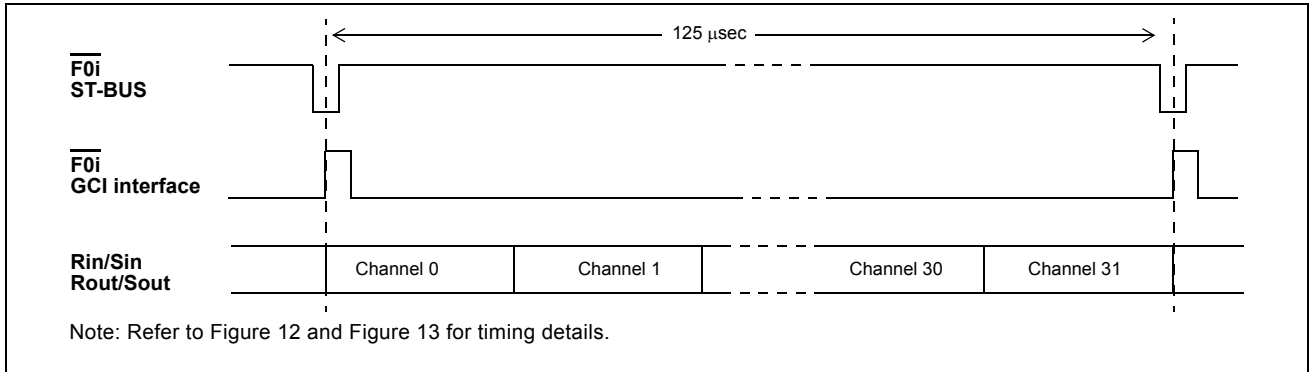


Figure 9 - ST-BUS and GCI Interface Channel Assignment for 2 Mbps Data Streams

Base Address +		Echo Canceller A	Base Address +		Echo Canceller B
MS Byte	LS Byte		MS Byte	LS Byte	
-	00h	Control Reg 1	-	20h	Control Reg 1
-	01h	Control Reg 2	-	21h	Control Reg 2
-	02h	Status Reg	-	22h	Status Reg
-	03h	Reserved	-	23h	Reserved
-	04h	Flat Delay Reg	-	24h	Flat Delay Reg
-	05h	Reserved	-	25h	Reserved
-	06h	Decay Step Size Reg	-	26h	Decay Step Size Reg
-	07h	Decay Step Number	-	27h	Decay Step Number
-	08h	Control Reg 3	-	28h	Control Reg 3
-	09h	Control Reg 4	-	29h	Control Reg 4
-	0Ah	Noise Scaling	-	2Ah	Noise Scaling
-	0Bh	Noise Control	-	2Bh	Noise Control
0Dh	0Ch	Rin Peak Detect Reg	2Dh	2Ch	Rin Peak Detect Reg
0Fh	0Eh	Sin Peak Detect Reg	2Fh	2Eh	Sin Peak Detect Reg
11h	10h	Error Peak Detect Reg	31h	30h	Error Peak Detect Reg
13h	12h	Reserved	33h	32h	Reserved
15h	14h	DTDT Reg	35h	34h	DTDT Reg
17h	16h	Reserved	37h	36h	Reserved
19h	18h	NLPTHR	39h	38h	NLPTHR
1Bh	1Ah	Step Size, MU	3Bh	3Ah	Step Size, MU
1Dh	1Ch	Gains	3Dh	3Ch	Gains
1Fh	1Eh	Reserved	3Fh	3Eh	Reserved

Table 3 - Memory Mapping of Per Channel Control and Status Registers

7.0 Memory Mapped Control and Status Registers

Internal memory and registers are memory mapped into the address space of the HOST interface. The internal dual ported memory is mapped into segments on a “per channel” basis to monitor and control each individual echo canceller and associated PCM channels. For example, in **Normal configuration**, echo canceller #5 makes use of Echo Canceller B from group 2. It occupies the internal address space from 0A0_{hex} to 0BF_{hex} and interfaces to PCM channel #5 on all serial PCM I/O streams.

As illustrated in Table 3, the “per channel” registers provide independent control and status bits for each echo canceller. Figure 10 shows the memory map of the control/status register blocks for all echo cancellers.

When **Extended Delay** or **Back-to-Back** configuration is selected, Control Register 1 of ECA and ECB and Control Register 2 of the selected group of echo cancellers require special care. Refer to the Register description section.

Table 4 is a list of the channels used for the 16 groups of echo cancellers when they are configured as **Extended Delay** or **Back-to-Back**.

7.1 Normal Configuration

For a given group (group 0 to 15), 2 PCM I/O channels are used. For example, group 1 Echo Cancellers A and B, channels 2 and 3 are active.

Group	Channels	Group	Channels
0	0, 1	8	16, 17
1	2, 3	9	18, 19
2	4, 5	10	20, 21
3	6, 7	11	22, 23
4	8, 9	12	24, 25
5	10, 11	13	26, 27
6	12, 13	14	28, 29
7	14, 15	15	30, 31

Table 4 - Group and Channel Allocation

7.2 Extended Delay Configuration

For a given group (group 0 to 15), only one PCM I/O channel is active (Echo Canceller A) and the other channel carries quiet code. For example, group 2, Echo Canceller A (Channel 4) will be active and Echo Canceller B (Channel 5) will carry quiet code.

7.3 Back-to-Back Configuration

For a given group (group 0 to 15), only one PCM I/O channel is active (Echo Canceller A) and the other channel carries quiet code. For example, group 5, Echo Canceller A (Channel 10) will be active and Echo Canceller B (Channel 11) will carry quiet code.

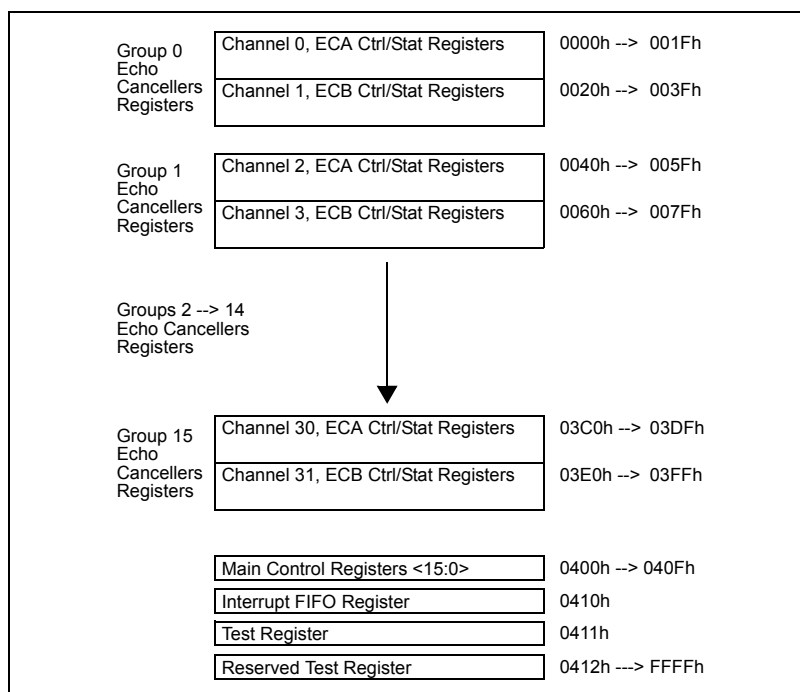


Figure 10 - Memory Mapping

7.4 Power Up Sequence

On power up, the $\overline{\text{RESET}}$ pin must be held low for 100 μs . Forcing the $\overline{\text{RESET}}$ pin low will put the ZL50232 in power down state. In this state, all internal clocks are halted, $\text{D}<7:0>$, Sout , Rout , DTA and IRQ pins are tristated. The 16 Main Control Registers, the Interrupt FIFO Register and the Test Register are reset to zero.

When the $\overline{\text{RESET}}$ pin returns to logic high and a valid MCLK is applied, the user must wait 500 μs for the PLL to lock. C4i and F0i can be active during this period. At this point, the echo canceller must have the internal registers reset to an initial state. This is accomplished by one of two methods. The user can either issue a second hardware reset or perform a software reset. A second hardware reset is performed by driving the $\overline{\text{RESET}}$ pin low for at least 500 ns and no more than 1500 ns before being released. A software reset is accomplished by programming a "1" to each of the PWUP bits in the Main Control Registers, waiting 250 μs (2 frames) and then programming a "0" to each of the PWUP bits.

The user must then wait 500 μs for the PLL to relock. Once the PLL has locked, the user can power up the 16 groups of echo cancellers individually by writing a "1" into the PWUP bit in Main Control Register of each echo canceller group.

For each group of echo cancellers, when the PWUP bit toggles from zero to one, echo cancellers A and B execute their initialization routine. The initialization routine sets their registers, Base Address+00_{hex} to Base Address+3F_{hex}, to the default Reset Value and clears the Adaptive Filter coefficients. Two frames are necessary for the initialization routine to execute properly.

Once the initialization routine is executed, the user can set the per channel Control Registers, Base Address+00_{hex} to Base Address+3F_{hex}, for the specific application.

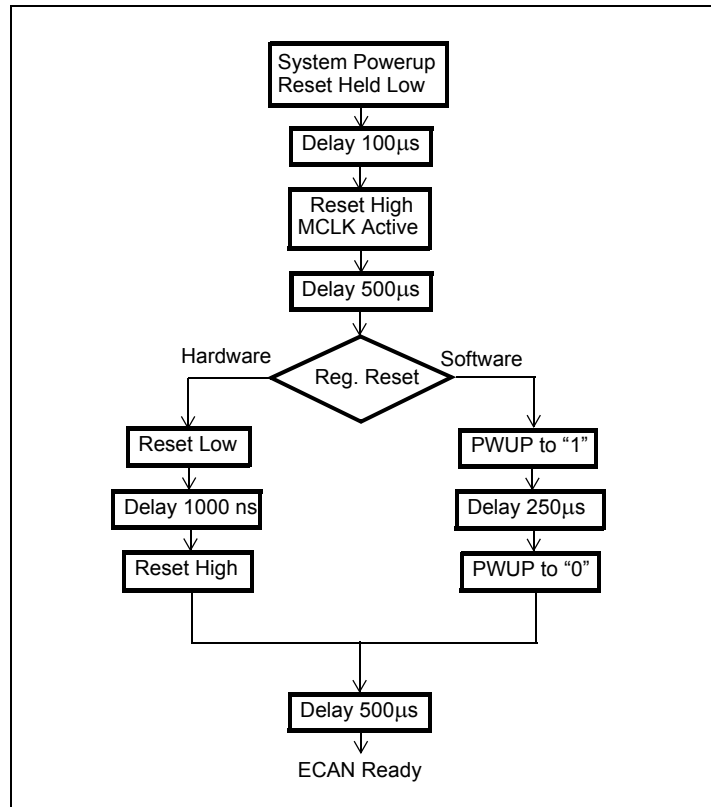


Figure 11 - Power Up Sequence Flow Diagram

7.5 Power Management

Each group of echo cancellers can be placed in Power Down mode by writing a “0” into the PWUP bit in their respective Main Control Register. When a given group is in Power Down mode, the corresponding PCM data are bypassed from Rin to Rout and from Sin to Sout with two frames delay. Refer to the Main Control Register section for description.

The typical power consumption can be calculated with the following equation:

$$P_C = 9 * Nb_of_groups + 3.6, \text{ in } mW$$

where $0 \leq Nb_of_groups \leq 16$.

7.6 Call Initialization

To ensure fast initial convergence on a new call, it is important to clear the Adaptive Filter. This is done by putting the echo canceller in bypass mode for at least one frame (125 µs) and then enabling adaptation.

Since the Narrow Band Detector is “ON” regardless of the functional state of Echo Canceller it is recommended that the Echo cancellers are reset before any call progress tones are applied.

7.7 Interrupts

The ZL50232 provides an interrupt pin ($\overline{\text{IRQ}}$) to indicate to the HOST processor when a G.164 or G.165 Tone Disable is detected and released.

Although the ZL50232 may be configured to react automatically to tone disable status on any input PCM voice channels, the user may want for the external HOST processor to respond to Tone Disable information in an appropriate application-specific manner.

Each echo canceller will generate an interrupt when a Tone Disable occurs and will generate another interrupt when a Tone Disable releases.

Upon receiving an $\overline{\text{IRQ}}$, the HOST CPU should read the Interrupt FIFO Register. This register is a FIFO memory containing the channel number of the echo canceller that has generated the interrupt.

All pending interrupts from any of the echo cancellers and their associated input channel number are stored in this FIFO memory. The $\overline{\text{IRQ}}$ always returns high after a read access to the Interrupt FIFO Register. The $\overline{\text{IRQ}}$ pin will toggle low for each pending interrupt.

After the HOST CPU has received the channel number of the interrupt source, the corresponding per channel Status Register can be read from internal memory to determine the cause of the interrupt (see Table 3 for address mapping of Status register). The TD bit indicates the presence of a Tone Disable.

The MIRQ bit 5 in the Main Control Register 0 masks interrupts from the ZL50232. To provide more flexibility, the MTDBI (bit-4) and MTDAI (bit-3) bits in the Main Control Register<15:0> allow Tone Disable to be masked or unmasked from generating an interrupt on a per channel basis. Refer to the Registers Description section.

8.0 JTAG Support

The ZL50232 JTAG interface conforms to the Boundary-Scan standard IEEE1149.1. This standard specifies a design-for-testability technique called Boundary-Scan test (BST). The operation of the Boundary Scan circuitry is controlled by an Test Access Port (TAP) controller. JTAG inputs are **3.3 V** compliant only.

8.1 Test Access Port (TAP)

The TAP provides access to many test functions of the ZL50232. It consists of four input pins and one output pin. The following pins are found on the TAP.

- Test Clock Input (TCK)
The TCK provides the clock for the test logic. The TCK does not interfere with any on-chip clock and thus remains independent. The TCK permits shifting of test data into or out of the Boundary-Scan register cells concurrent with the operation of the device and without interfering with the on-chip logic.
- Test Mode Select Input (TMS)
The logic signals received at the TMS input are interpreted by the TAP Controller to control the test operations. The TMS signals are sampled at the rising edge of the TCK pulse. This pin is internally pulled to V_{DD1} when it is not driven from an external source.
- Test Data Input (TDI)
Serial input data applied to this port is fed either into the instruction register or into a test data register, depending on the sequence previously applied to the TMS input. Both registers are described in a subsequent section. The received input data is sampled at the rising edge of TCK pulses. This pin is internally pulled to V_{DD1} when it is not driven from an external source.

- **Test Data Output (TDO)**
Depending on the sequence previously applied to the TMS input, the contents of either the instruction register or data register are serially shifted out towards the TDO. The data from the TDO is clocked on the falling edge of the TCK pulses. When no data is shifted through the Boundary Scan cells, the TDO driver is set to a high impedance state.
- **Test Reset (TRST)**
This pin is used to reset the JTAG scan structure. This pin is internally pulled to V_{SS} .

8.2 Instruction Register

In accordance with the IEEE 1149.1 standard, the ZL50232 uses public instructions. The JTAG Interface contains a 3-bit instruction register. Instructions are serially loaded into the instruction register from the TDI when the TAP Controller is in its shifted-IR state. Subsequently, the instructions are decoded to achieve two basic functions: to select the test data register that will operate while the instruction is current, and to define the serial test data register path, which is used to shift data between TDI and TDO during data register scanning.

8.3 Test Data Registers

As specified in IEEE 1149.1, the ZL50232 JTAG Interface contains three test data registers:

- **Boundary-Scan register**
The Boundary-Scan register consists of a series of Boundary-Scan cells arranged to form a scan path around the boundary of the ZL50232 core logic.
- **Bypass Register**
The Bypass register is a single stage shift register that provides a one-bit path from TDI to TDO.
- **Device Identification register**
The Device Identification register provides access to the following encoded information: device version number, part number and manufacturer's name.

Absolute Maximum Ratings*

	Parameter	Symbol	Min.	Max.	Units
1	I/O Supply Voltage (V_{DD1})	V_{DD_IO}	-0.5	5.0	V
2	Core Supply Voltage (V_{DD2})	V_{DD_CORE}	-0.5	2.5	V
3	Input Voltage	V_{I3}	$V_{SS} - 0.5$	$V_{DD1} + 0.5$	V
4	Input Voltage on any 5 V Tolerant I/O pins	V_{I5}	$V_{SS} - 0.3$	7.0	V
5	Continuous Current at digital outputs	I_o		20	mA
6	Package power dissipation	P_D		2	W
7	Storage temperature	T_S	-55	150	°C

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units
1	Operating Temperature	T_{OP}	-40		+85	°C
2	I/O Supply Voltage (V_{DD_IO})	V_{DD1}	3.0	3.3	3.6	V
3	Core Supply Voltage (V_{DD_CORE})	V_{DD2}	1.6	1.8	2.0	V
4	Input High Voltage on 3.3 V tolerant I/O	V_{IH3}	$0.7V_{DD1}$		V_{DD1}	V
5	Input High Voltage on 5 V tolerant I/O pins	V_{IH5}	$0.7V_{DD1}$		5.5	V
6	Input Low Voltage	V_{IL}			$0.3V_{DD1}$	V

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics† - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Static Supply Current	I_{CC}			250	μA	RESET = 0
	IDD_IO ($V_{DD1} = 3.3$ V)	I_{DD_IO}		10		mA	All 32 channels active
	IDD_CORE ($V_{DD2} = 1.8$ V)	I_{DD_CORE}		65		mA	All 32 channels active
2	Power Consumption	P_C		150		mW	All 32 channels active
I N P U T S	Input High Voltage	V_{IH}	$0.7V_{DD1}$			V	
	Input Low Voltage	V_{IL}			$0.3V_{DD1}$	V	
	Input Leakage	I_{IH}/I_{IL}			10	μA	$V_{IN} = V_{SS}$ to V_{DD1} or 5.5 V
	Input Leakage on Pullup	I_{LU}		-30	-55	μA	$V_{IN} = V_{SS}$
	Input Leakage on Pulldown	I_{LD}		30	65	μA	$V_{IN} = V_{DD1}$ See Note 1
6	Input Pin Capacitance	C_I			10	pF	
O U T P U T S	Output High Voltage	V_{OH}	$0.8V_{DD1}$			V	$I_{OH} = 12$ mA
	Output Low Voltage	V_{OL}			0.4	V	$I_{OL} = 12$ mA
	High Impedance Leakage	I_{OZ}			10	μA	$V_{IN} = V_{SS}$ to 5.5 V
	Output Pin Capacitance	C_O			10	pF	

† Characteristics are over recommended operating conditions unless otherwise stated.

‡ Typical figures are at 25°C, $V_{DD1} = 3.3$ V and are for design aid only: not guaranteed and not subject to production testing.

* Note 1: Maximum leakage on pins (output or I/O pins in high impedance state) is over an applied voltage (V_{IN}).

AC Electrical Characteristics[†] - Timing Parameter Measurement Voltage Levels

- Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym.	Level	Units	Conditions
1	CMOS Threshold	V_{TT}	$0.5V_{DD1}$	V	
2	CMOS Rise/Fall Threshold Voltage High	V_{HM}	$0.7V_{DD1}$	V	
3	CMOS Rise/Fall Threshold Voltage Low	V_{LM}	$0.3V_{DD1}$	V	

† Characteristics are over recommended operating conditions unless otherwise stated.

AC Electrical Characteristics[†] - Frame Pulse and $\overline{C4i}$

	Characteristic	Sym.	Min.	Typ. [‡]	Max.	Units	Notes
1	Frame pulse width (ST-BUS, GCI)	t_{FPW}	20		2* $t_{CP}-20$	ns	
2	Frame Pulse Setup time before $\overline{C4i}$ falling (ST-BUS or GCI)	t_{FPS}	10	122	150	ns	
3	Frame Pulse Hold Time from $\overline{C4i}$ falling (ST-BUS or GCI)	t_{FPH}	10	122	150	ns	
4	$\overline{C4i}$ Period	t_{CP}	190	244	300	ns	
5	$\overline{C4i}$ Pulse Width High	t_{CH}	85		150	ns	
6	$\overline{C4i}$ Pulse Width Low	t_{CL}	85		150	ns	
7	$\overline{C4i}$ Rise/Fall Time	t_r, t_f			10	ns	

† Characteristics are over recommended operating conditions unless otherwise stated.

‡ Typical figures are at 25°C, $V_{DD1} = 3.3$ V and for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics[†] - Serial Streams for ST-BUS and GCI Backplanes

	Characteristic	Sym.	Min.	Typ. [‡]	Max.	Units	Test Conditions
1	Rin/Sin Set-up Time	t_{SIS}	10			ns	
2	Rin/Sin Hold Time	t_{SIH}	10			ns	
3	Rout/Sout Delay - Active to Active	t_{SOD}			60	ns	$C_L = 150$ pF
4	Output Data Enable (ODE) Delay	t_{ODE}			30	ns	$C_L = 150$ pF, $R_L = 1$ K See Note 1

† Characteristics are over recommended operating conditions unless otherwise stated.

‡ Typical figures are at 25°C, $V_{DD1} = 3.3$ V and for design aid only: not guaranteed and not subject to production testing.

* Note1: High Impedance is measured by pulling to the appropriate rail with R_L , with timing corrected to cancel time taken to discharge C_L .