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Adaptive Digital DC/DC PWM Controller with Auto Compensation

ZL8101

The ZL8101 is a digital PWM controller with auto compensation that is designed to work with either the ZL1505 MOSFET driver IC, ISL6611 Phase Doubler IC, or DrMOS type devices. Current sharing allows multiple devices to be connected in parallel to source loads with very high current demands. Adaptive performance optimization algorithms improve power conversion efficiency across the entire load range. Zilker Labs Digital-DC™ technology enables a blend of power conversion performance and power management features.

The ZL8101 is designed to be a flexible building block for DC power and can be easily adapted to designs ranging from a single-phase power supply operating from a 4.5V input to a multi-phase supply operating from a 12V input. The ZL8101 eliminates the need for complicated power supply managers as well as numerous external discrete components.

Most operating features can be configured by simple pin-strap/resistor selection or through the SMBus™ serial interface. The ZL8101 uses the PMBus™ protocol for communication with a host controller and the Digital-DC bus for communication between other Zilker Labs devices.

Features

- Efficient Synchronous Buck Controller
- Adaptive Performance Optimization Algorithms
- ±1% Output Voltage Accuracy
- Auto Compensation
- Snapshot™ Parametric Capture
- I²C/SMBus Interface, PMBus Compatible
- Internal Non-Volatile Memory (NVM)
- Tri-State PWM Gate Outputs
- Compatible with Industry Standard DrMOS Devices
- Compatible with Intersil ISL6611 Phase Doubler
- Synchronized External Driver Control

Applications

- Servers/Storage Equipment
- Telecom/Datacom Equipment
- Power Supplies (Memory, DSP, ASIC, FPGA)

Related Literature

- [AN2033](#) “Zilker Labs PMBus Command Set - DDC Products”
- [AN2034](#) “Configuring Current Sharing on the ZL2004 and ZL2006”
- [AN2010](#) “Thermal and Layout Guidelines for Digital-DC™ Products”

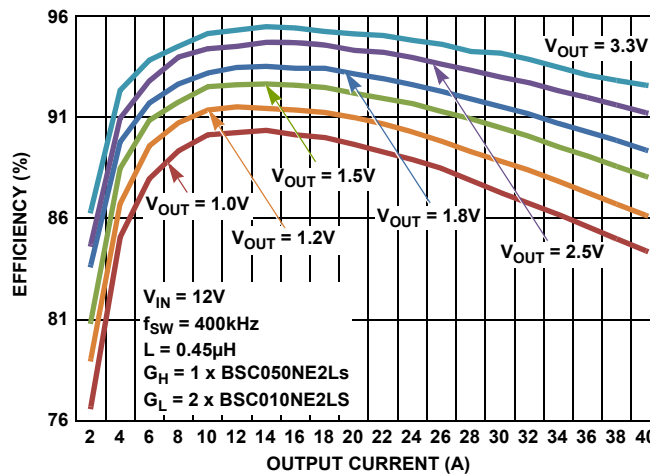
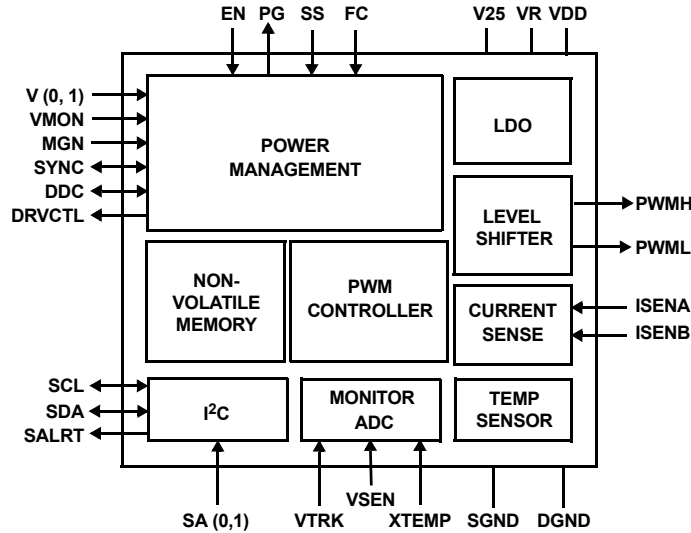


FIGURE 1. EFFICIENCY vs LOAD CURRENT

ZL8101

Block Diagram



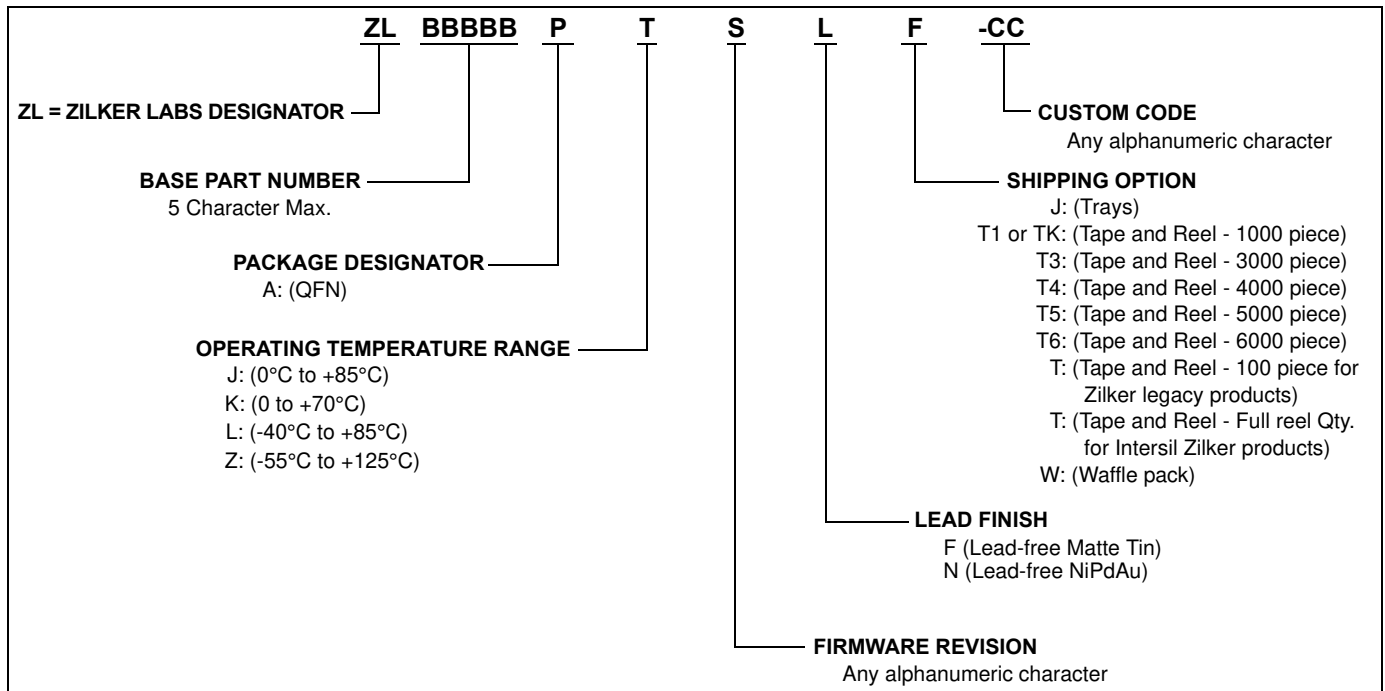
Ordering Information

PART NUMBER (Notes 1, 2)	PART MARKING	TEMP. RANGE (°C)	PACK METHOD	PACKAGE	PKG. DWG. #
ZL8101ALAF	8101	-40 to +85	Tape and Reel 6k	32 Ld QFN	L32.5x5G
ZL8101ALAFK	8101	-40 to +85	Tape and Reel 1k	32 Ld QFN	L32.5x5G
ZL8101ALAF	8101	-40 to +85	Bulk	32 Ld QFN	L32.5x5G

NOTES:

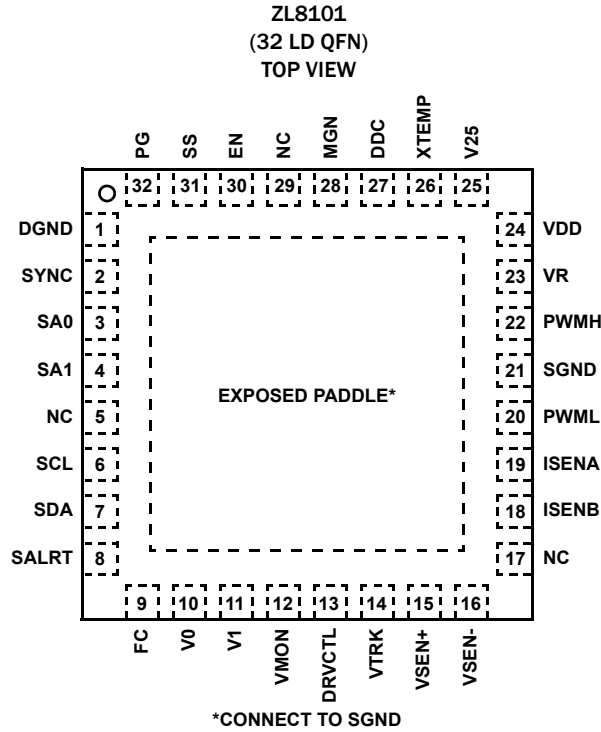
- These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
- For Moisture Sensitivity Level (MSL), please see device information page for [ZL8101](#). For more information on MSL please see techbrief [TB363](#).

ZL Types



ZL8101

Pin Configuration



Pin Descriptions

PIN	LABEL	TYPE (Note 3)	DESCRIPTION
1	DGND	PWR	Digital ground. Connect to low impedance contiguous ground plane.
2	SYNC	I/O, M (Note 4)	Clock synchronization input. Used to set the frequency of the internal switch clock, to sync to an external clock or to output internal clock.
3	SA0	I, M	Serial address select pins. Used to assign a unique address for each individual device or to enable certain management features.
4	SA1		
5	NC		No Connect. Leave pin open.
6	SCL	I/O	Serial clock. Connect to external host and/or to other ZL devices.
7	SDA	I/O	Serial data. Connect to external host and/or to other ZL devices.
8	SALRT	O	Serial alert. Connect to external host if desired.
9	FC	I	Auto compensation configuration pin. Used to set up auto compensation.
10	V0	I, M	Output voltage selection pins. Used to set V_{OUT} set-point and V_{OUT} max.
11	V1		
12	VMON	I, M	External voltage monitoring (can be used for external driver bias monitoring for Power-Good).
13	DRVCTL	O	External driver enable control output.
14	VTRK	I	Tracking sense input. Used to track an external voltage source.
15	VSEN+	I	Differential Output voltage sense feedback. Connect to positive output regulation point.
16	VSEN-	I	Differential Output voltage sense feedback. Connect to negative output regulation point.
17	NC		No Connect. Leave pin open.
18	ISENB	I	Differential voltage input for current sensing.
19	ISENA	I	Differential voltage input for current sensing. High voltage (DCR).

Pin Descriptions (Continued)

PIN	LABEL	TYPE (Note 3)	DESCRIPTION
20	PWML	O	PWM Gate low signal.
21	SGND	PWR	Connect to low impedance ground plane. Internal connection to SGND.
22	PWMH	O	PWM Gate High signal.
23	VR	PWR	Internal 5V Reference.
24	VDD (Note 5)	PWR	Supply voltage.
25	V25	PWR	Internal 2.5V reference used to power internal circuitry.
26	XTEMP	I	External temperature sensor input. Connect to external 2N3904 (Base Emitter junction).
27	DDC	I	Single wire DDC bus (Current sharing, inter device communication).
28	MGN	I	V _{OUT} margin control.
29	NC		No Connect. Leave pin open.
30	EN	I	Enable. Active signal enables PWM switching.
31	SS	I, M	Soft-start delay and ramp select. Sets the delay from when EN is asserted until the output voltage starts to ramp and the ramp time.
32	PG	O	Power-Good output.
PD	SGND	PWR	Exposed thermal pad. Connect to low impedance ground plane. Internal connection to SGND.

NOTES:

3. I = Input, O = Output, PWR = Power or Ground. M = Multi-mode pins (refer to "Multi-mode Pins" on page 12).
4. The SYNC pin can be used as a logic pin, a clock input or a clock output.
5. The V_{DD} pin voltage is used to measure V_{IN} as part of the Pre-Bias calculation and Loop Gain calculation used for current sharing ramps.

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Absolute Maximum Ratings (Note 6)

DC Supply Voltage for VDD Pin	-0.3V to 17V
Logic I/O Voltage for DDC, EN, FC, MGN, PG, SA(0,1), SALRT, SCL, SDA, SS, SYNC, VMON, V(0,1) Pins	-0.3V to 6.5V
Analog Input Voltages for VSEN+, VSEN-, VTRK, XTEMP Pins	-0.3V to 6.5V
Analog Input Voltages for ISENA, ISENB Pins	-1.5V to 6.5V
MOSFET Drive Reference for VR Pin	-0.3V to 6.5V
Logic Reference for V25 Pin	-0.3V to 3V
Ground Voltage Differential ($V_{DGND}-V_{SGND}$) for DGND, SGND Pins	-0.3V to +0.3V
ESD Rating	
Human Body Model (Tested per JESD22-A114F)	2000V
Machine Model (Tested per JESD22-A115C)	200V
Latch Up	Tested per JESD-78

Thermal Information

Thermal Resistance (Typical)	θ_{JA} ($^{\circ}\text{C}/\text{W}$)	θ_{JC} ($^{\circ}\text{C}/\text{W}$)
32 Ld QFN Package (Notes 7, 8)	35	5
Operating Junction Temperature Range	-40 $^{\circ}\text{C}$ to +125 $^{\circ}\text{C}$	
Junction Temperature	-55 $^{\circ}\text{C}$ to +150 $^{\circ}\text{C}$	
Storage Temperature Range	-55 $^{\circ}\text{C}$ to +150 $^{\circ}\text{C}$	
Pb-Free Reflow Profile	see link below http://www.intersil.com/pbfree/Pb-FreeReflow.asp	

Recommended Operating Conditions

Input Supply Voltage Range	4.5V to 14V
Output Voltage Range (Inductor Sensing) (Note 9)	0.54V to 4V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

6. Voltage measured with respect to SGND.
7. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
8. For θ_{JC} , the "case temp" location is the center of the exposed metal pad on the package underside.
9. Includes margin limits.

Electrical Specifications $V_{DD} = 12\text{V}$, $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, unless otherwise specified. Typical values are at $T_A = +25^{\circ}\text{C}$. **Boldface limits apply over the operating temperature range, -40°C to $+85^{\circ}\text{C}$.**

PARAMETER	CONDITIONS	MIN (Note 10)	TYP	MAX (Note 10)	UNIT
INPUT AND SUPPLY CHARACTERISTICS					
I_{DD} Supply Current at $f_{SW} = 200\text{kHz}$	GH no load, GL no load, MISC_CONFIG[7] = 1		16	30	mA
I_{DD} Supply Current at $f_{SW} = 1.4\text{MHz}$			25	50	mA
I_{DDS} Shutdown Current	EN = 0V, No I ² C/SMBus activity		6.5	8	mA
VR Reference Output Voltage	$V_{DD} > 6\text{V}$	4.5	5.2	5.7	V
V25 Reference Output Voltage	$V_R > 3\text{V}$	2.25	2.5	2.75	V
OUTPUT CHARACTERISTICS					
Output Voltage Adjustment Range (Note 11)		0.6		3.6	V
Output Voltage Set-point Resolution	Set using resistors		10		mV
	Set using I ² C/SMBus		± 0.025		% FS (Note 12)
Output Voltage Accuracy (Note 13)	Includes line, load, temp	-1		1	%
VSEN Input Bias Current	VSEN = 4V		80	150	μA
Current Sense Differential Input Voltage (V_{OUT} Referenced)	$V_{ISENA} - V_{ISENB}$	-50		50	mV
Current Sense Input Bias Current (V_{OUT} Referenced, $V_{OUT} \leq 3.6\text{V}$)	ISENA	-50		50	nA
	ISENB	-75		75	μA
Soft-start Delay Duration Range	Set using SS pin or resistor	2		20	ms
	Set using I ² C/SMBus	0.002		500	s
Soft-start Delay Duration Accuracy	Turn-on delay (precise mode) (Notes 14, 15)		± 0.25		ms
	Turn-on delay (normal mode) (Note 16)		-1/+5		ms
	Turn-off delay (Note 16)		-1/+5		ms

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Electrical Specifications $V_{DD} = 1.2V$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$, unless otherwise specified. Typical values are at $T_A = +25^{\circ}C$. **Boldface limits apply over the operating temperature range, $-40^{\circ}C$ to $+85^{\circ}C$. (Continued)**

PARAMETER	CONDITIONS	MIN (Note 10)	TYP	MAX (Note 10)	UNIT
Soft-start Ramp Duration Range	Set using SS pin or resistor	2		20	ms
	Set using I ² C	0		200	ms
Soft-start Ramp Duration Accuracy			100		μs
LOGIC INPUT/OUTPUT CHARACTERISTICS					
Logic Input Bias Current	EN, PG, SCL, SDA, SALRT pins	-250		250	nA
MGN Input Bias Current		-1		1	mA
Logic Input Low, V _{IL}				0.8	V
Logic Input OPEN (N/C)	Multi-mode logic pins		1.4		V
Logic Input High, V _{IH}		2.0			V
Logic Output Low, V _{OL}	I _{OL} ≤ 4mA			0.4	V
Logic Output High, V _{OH}	I _{OH} ≥ -2mA	2.25			V
PWM OUTPUTS (PWMH, PWML)					
PWM Output Voltage Low Threshold	I _{LOAD} = ±500μA (Note 20) Sinking			100	mV
PWN Output Voltage High Threshold		4.7			V
EXTERNAL DRIVER CONTROL (DRVCTL)					
HW_EN to DRVCTL Delay (t _{dED})	Turn-on		100	350	μs
3S_Delay	Turn-off		0.1	2	ms
t _{dOFF}	Turn-off		0.1	0.5	ms
OSCILLATOR AND SWITCHING CHARACTERISTICS					
Switching Frequency Range		200		1400	kHz
Switching Frequency Set-point Accuracy		-5		5	%
Maximum PWM Duty Cycle	Factory default, decreases with frequency	95			%
Minimum SYNC Pulse Width		150			ns
Input Clock Frequency Drift Tolerance	External clock source	-13		13	%
TRACKING					
VTRK Input Bias Current	VTRK = 4.0V		110	200	μA
VTRK Tracking Ramp Accuracy	100% Tracking, V _{OUT} - VTRK (During Ramps)	-100		+100	mV
VTRK Regulation Accuracy	100% Tracking, V _{OUT} - VTRK (Steady State)		1.5%		%
FAULT PROTECTION CHARACTERISTICS					
UVLO Threshold Range	Configurable via I ² C/SMBus	2.85		16	V
UVLO Set-point Accuracy		-150		150	mV
UVLO Hysteresis	Factory default		3		%
	Configurable via I ² C/SMBus	0		100	%
UVLO Delay				2.5	μs
Power-Good V _{OUT} Low Threshold	Factory default		90		% V _{OUT}
Power-Good V _{OUT} High Threshold	Factory default		115		% V _{OUT}
Power-Good V _{OUT} Hysteresis	Factory default		5		%

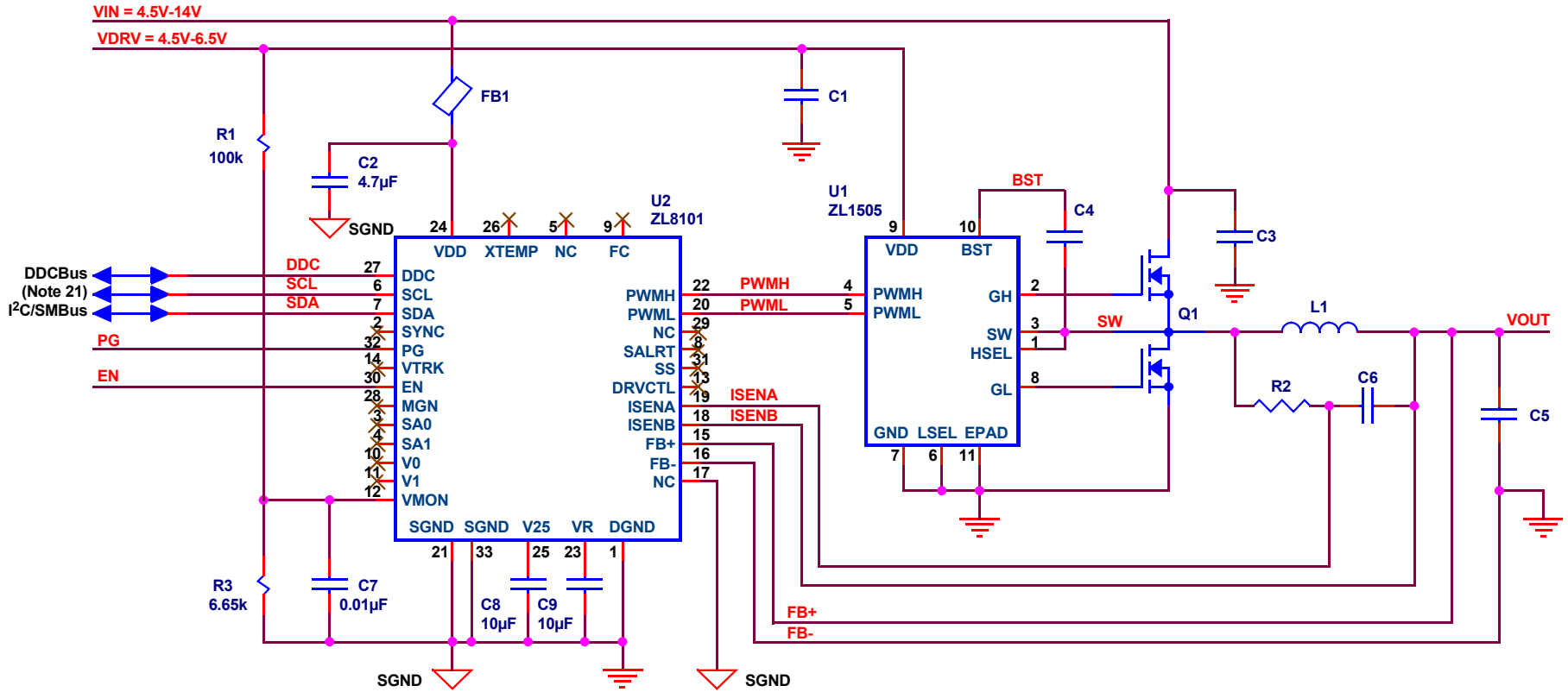
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Electrical Specifications $V_{DD} = 1.2V$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$, unless otherwise specified. Typical values are at $T_A = +25^{\circ}C$. **Boldface limits apply over the operating temperature range, $-40^{\circ}C$ to $+85^{\circ}C$. (Continued)**

PARAMETER	CONDITIONS	MIN (Note 10)	TYP	MAX (Note 10)	UNIT
Power-good Delay	Using pin-strap or resistor (Note 17)	2		20	ms
	Configurable via I ² C/SMBus	0		500	s
VSEN Undervoltage Threshold	Factory default		85		% V _{OUT}
	Configurable via I ² C/SMBus	0		110	% V _{OUT}
VSEN Overvoltage Threshold	Factory default		115		% V _{OUT}
	Configurable via I ² C/SMBus	0		115	% V _{OUT}
VSEN Undervoltage Hysteresis			5		% V _{OUT}
VSEN Undervoltage/Overvoltage Fault Response Time	Factory default		16		μs
	Configurable via I ² C/SMBus	5		60	μs
Current Limit Set-point Accuracy (V _{OUT} Referenced)			±10		% FS (Note 18)
Current Limit Protection Delay	Factory default		5		t _{sw} (Note 19)
	Configurable via I ² C/SMBus	1		32	t _{sw} (Note 19)
Temperature Compensation of Current Limit Protection Threshold	Factory default		4400		ppm/°C
	Configurable via I ² C/SMBus	100		12700	ppm/°C
Thermal Protection Threshold (Junction Temperature)	Factory default		125		°C
	Configurable via I ² C/SMBus	-40		125	°C
Thermal Protection Hysteresis			15		°C

NOTES:

10. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
11. Set point adjustment range does not include margin limits.
12. Percentage of Full Scale (FS) with temperature compensation applied.
13. V_{OUT} set-point measured at the termination of the VSEN+ and VSEN- sense points.
14. The device requires approximately 2ms following an enable signal and prior to ramping its output. The delay accuracy will vary by ±0.25ms around the 2ms minimum delay value.
15. Precise ramp timing mode is only valid when using EN pin to enable the device rather than PMBus enable.
16. The devices may require up to a 4ms delay following an assertion of the enable signal (normal mode) or following the de-assertion of the enable signal.
17. Factory default Power-good delay is set to the same value as the soft-start ramp time.
18. Percentage of Full Scale (FS) with temperature compensation applied.
19. t_{sw} = 1/f_{sw}, where f_{sw} is the switching frequency.
20. Outputs are Tri-State when disabled.



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FIGURE 2. EXAMPLE DESIGN USING ZL8101 AND ZL1505 DRIVER

NOTE:

21. The DDC bus requires a pull-up resistor. The resistance will vary based on the capacitive loading of the bus (and on the number of devices connected). The 10k default value, assuming a maximum of 100pF per device, provides the necessary 1µs pull-up rise time. Please refer to the "Digital-DC Bus" section on page 30 for more information.

Typical Application Circuit

Figure 2 represents a typical application circuit for single phase applications using a ZL1505 driver. Other power stages like DrMOS devices can be substituted for the ZL1505 and output FET's.

Figure 3 represents a typical application circuit for 2-phase designs using a ISL6611 phase doubler IC.

ZL8101 Overview

Digital-DC Architecture

The ZL8101 is an innovative mixed-signal power conversion and power management IC based on Zilker Labs' patented Digital-DC technology that provides an integrated, high performance step-down converter for a wide variety of power supply applications.

Today's embedded power systems are typically designed for optimal efficiency at maximum load, reducing the peak thermal stress by limiting the total thermal dissipation inside the system.

Unfortunately, many of these systems are often operated at load levels far below the peak where the power system has been optimized, resulting in reduced efficiency. While this may not cause thermal stress to occur, it does contribute to higher electricity usage and results in higher overall system operating costs.

Zilker Labs' efficiency-adaptive ZL8101 DC-DC controller helps mitigate this scenario by enabling the power converter to automatically change their operating state to increase efficiency and overall performance.

Its unique digital PWM loop utilizes an innovative mixed signal topology to enable precise control of the power conversion

process with no software required, resulting in a very flexible device that is also easy to use. An extensive set of power management functions is fully integrated and can be configured using simple pin connections or via the I²C/SMBus hardware interface using standard PMBus commands. The user configuration can be saved in an on-chip non-volatile memory (NVM), allowing ultimate flexibility.

Once enabled, the ZL8101 is immediately ready to regulate power and perform power management tasks with no programming required. The ZL8101 can be configured by simply connecting its pins according to the tables provided in this document. Advanced configuration options and real-time configuration changes are available via the I²C/SMBus interface if desired, and continuous monitoring of multiple operating parameters is possible with minimal interaction from a host controller. Integrated sub-regulation circuitry enables single supply operation from any supply between 4.5V and 14V with no secondary bias supplies needed.

Zilker Labs provides a comprehensive set of application notes to assist with power supply design and simulation. An evaluation board is also available to help the user become familiar with the device. This board can be evaluated as a stand-alone platform using pin configuration settings. Additionally, a Windows™-based GUI is provided to enable full configuration and monitoring capability via the I²C/SMBus interface using an available computer and the included USB cable.

Please refer to www.intersil.com for access to the most up-to-date documentation or call your local Intersil sales office to order an evaluation kit.

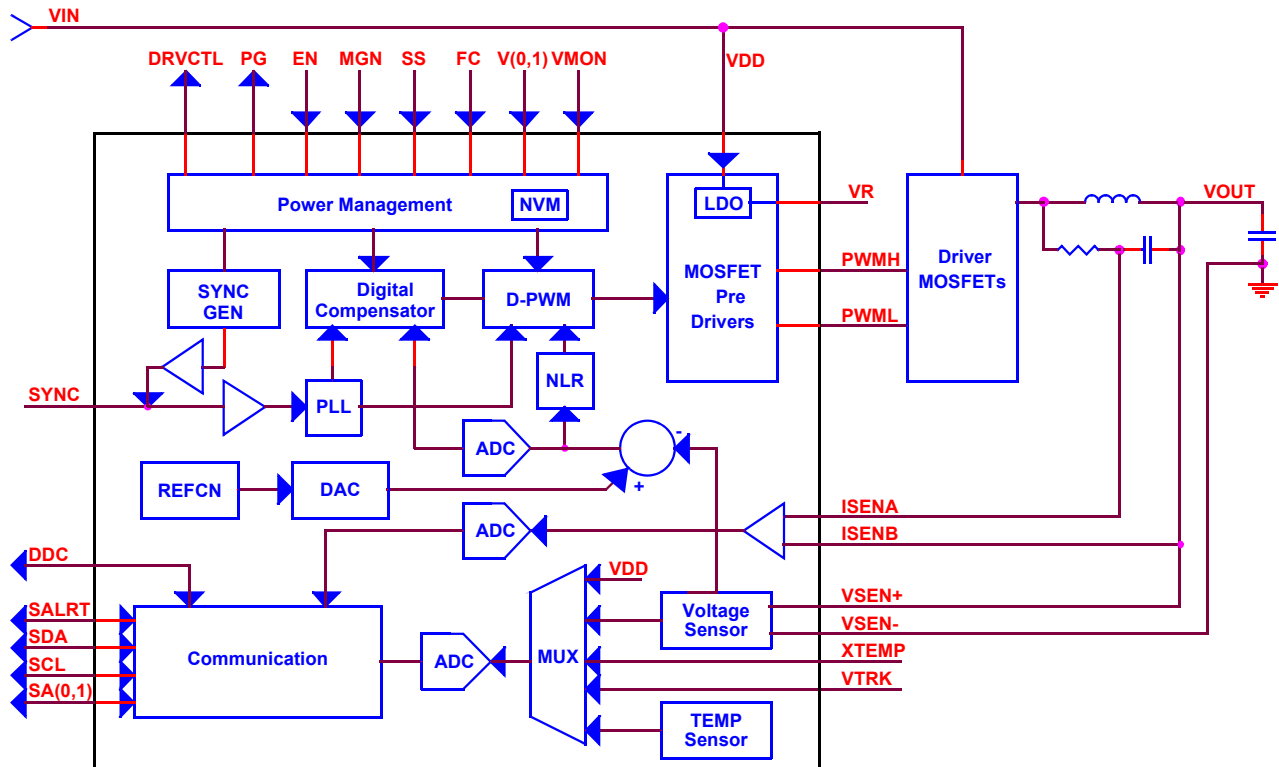


FIGURE 4. ZL8101 BLOCK DIAGRAM

Power Conversion Overview

The ZL8101 operates as a voltage-mode, synchronous buck converter with a selectable constant frequency pulse width modulator (PWM) control scheme that uses an external driver, MOSFETs, capacitors, and an inductor to perform power conversion.

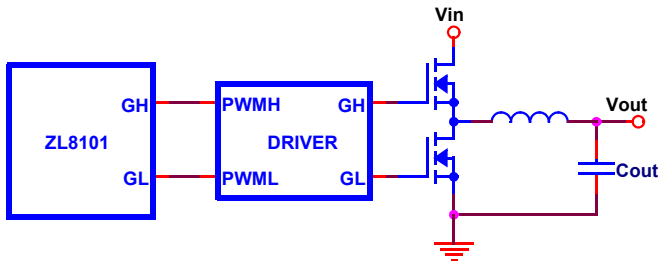


FIGURE 5. SYNCHRONOUS BUCK CONVERTER

Figure 5 illustrates the basic synchronous buck converter topology showing the primary power train components. This converter is also called a step-down converter, as the output voltage must always be lower than the input voltage.

DUAL OUTPUT PWM

The ZL8101 provides a dual PWM signal for use with the ZL1505 driver and tri-state capable outputs for compatibility with single input drivers and DrMOS devices.

When using the ZL8101/ZL1505 driver combination, higher efficiency can be obtained by enabling the Zilker Labs Adaptive Dead Time Algorithm.

The ZL1505 is a driver with two PWM inputs. Using two PWM signals (PWMH and PWML) offers more options during fault event and pre-bias conditions. The ZL8101 has several features to improve the power conversion efficiency. A non-linear response (NLR) loop improves the response time and reduces the output deviation as a result of a load transient. The ZL8101 monitors the power converter's operating conditions and continuously adjusts the turn-on and turn-off timing of the high-side and low-side MOSFETs to optimize the overall efficiency of the power supply. Adaptive performance optimization algorithms such as dead-time control, diode emulation, and adaptive frequency are available to provide greater efficiency improvement. The ZL8101 can also be used with single-ended MOSFET drivers and DrMOS devices that require the PWMH output to Tri-State when Disabled.

The trade-offs for using this mode may include reduced efficiency and degraded pre-bias protection depending on the minimum pulse width requirement of the single input driver.

TRI-STATE PWM OUTPUTS

Anytime the ZL8101 has power applied and PMBus or HW Enable is de-asserted, the PWMH and PWML CMOS outputs are Tri-States. The PWM outputs switch between 0 and the voltage on the VR pin (typically 5V). The ZL8101 PWM outputs are compatible with drivers who's inputs are pulled between 2.5V and 5.5V. The Tri-State function is always active, so no controls are provided. The ZL1505 driver contains integrated pull-down resistors that deactivate the tri-state function.

DRIVER ENABLE CONTROL (DRVCTL)

The ZL8101 includes an output pin that can be used to control the enable pin of single input drivers and DrMOS devices. The DRVCTL pin is asserted High plus a small delay time (t_{dED}) when HW Enable or PMBus Enable is asserted. The DRVCTL pin is de-asserted at the end of the fall time plus a delay (t_{dOFF}). See Figure 6 for timing information.

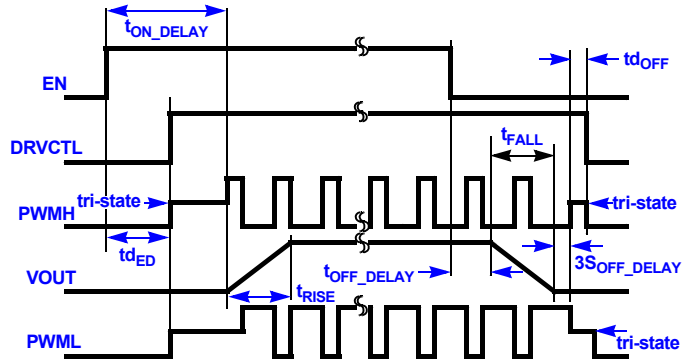


FIGURE 6. DRVCTL AND TRI-STATE BEHAVIOR

Power Management Overview

The ZL8101 incorporates a wide range of configurable power management options that are simple to implement with no external components. The ZL8101 includes circuit protection features that continuously safeguard the device and load from damage due to unexpected system faults. The ZL8101 can continuously monitor input voltage, output voltage/current, internal temperature, and the temperature of an external thermal diode. A Power-good output signal is also included to enable power-on reset functionality for an external processor.

All power management functions can be configured using either pin configuration techniques (see Figure 7) or via the I²C/SMBus interface. Monitoring parameters can also be pre-configured to provide alerts for specific conditions. See Application Note [AN2033](#) for more details on SMBus monitoring.

Multi-mode Pins

In order to simplify circuit design, the ZL8101 incorporates patented multi-mode pins that allow the user to easily configure many aspects of the device with no programming. Most power management features can be configured using these pins. The multi-mode pins can respond to four different connections as shown in Table 1. These pins are sampled when power is applied or by issuing a PMBus Restore command (See Application Note [AN2033](#)).

PIN-STRAP SETTINGS

This is the simplest implementation method, as no external components are required. Using this method, each pin can take on one of three possible states: LOW, OPEN, or HIGH. These pins can be connected to the V25 pin for logic HIGH settings as this pin provides a regulated voltage higher than 2V. Using a single pin, one of three settings can be selected. Using two pins, one of nine settings can be selected.

TABLE 1. MULTI-MODE PIN CONFIGURATION

PIN TIED TO	VALUE
LOW (Logic LOW)	<0.8VDC
OPEN (N/C)	No connection
HIGH (Logic HIGH)	>2.0VDC
Resistor to SGND	Set by resistor value

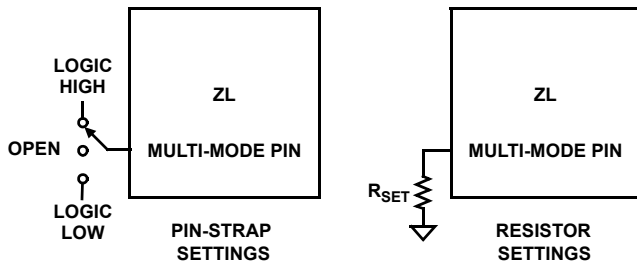


FIGURE 7. PIN-STRAP AND RESISTOR SETTING EXAMPLES

RESISTOR SETTINGS

This method allows a greater range of adjustability when connecting a finite value resistor (in a specified range) between the multi-mode pin and SGND. Standard 1% resistor values are used, and only every fourth E96 resistor value is used so the device can reliably recognize the value of resistance connected to the pin while eliminating the error associated with the resistor accuracy. Up to 31 unique selections are available using a single resistor.

I²C/SMBUS METHOD

Almost all ZL8101 functions can be configured via the I²C/SMBus interface using standard PMBus commands. Any value that has been configured using the pin-strap or resistor setting methods can also be re-configured and/or verified via the I²C/SMBus. See Application Note [AN2033](#) for more details.

The SMBus device address and VOUT_MAX are the only parameters that must be set by external pins. All other device parameters can be set via the I²C/SMBus. The device address is set using the SA0 and SA1 pins. VOUT_MAX is set to 10% greater than the voltage set by the V0 and V1 pins.

Power Conversion Functional Description

Internal Bias Regulators and Input Supply Connections

The ZL8101 employs two internal low dropout (LDO) regulators to supply bias voltages for internal circuitry, allowing it to operate from a single input supply. The internal bias regulators are as follows:

- VR: The VR LDO provides a regulated 5V bias supply for the MOSFET pre-driver circuits. It is powered from the VDD pin. A 4.7 to 10μF filter capacitor is required at the VR pin. To ensure regulator stability, capacitors outside of this range must not be used.

- V25: The V25 LDO provides a regulated 2.5V bias supply for the main controller circuitry. It is powered from an internal 5V node. A 4.7 to 10μF filter capacitor is required at the V25 pin. To ensure regulator stability capacitors outside of this range must not be used.

When the input supply (VDD) is higher than 5.5V, the VR pin should not be connected to any other pins. It should only have a filter capacitor attached as shown in Figure 8. Due to the dropout voltage associated with the VR bias regulator, the VDD pin must be connected to the VR pin for designs operating from a supply below 5.5V. Figure 8 illustrates the required connections for both cases.

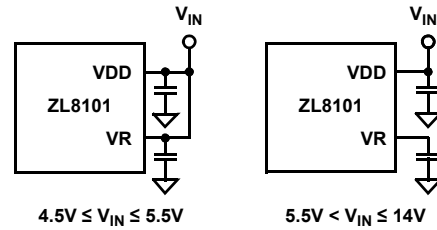


FIGURE 8. INPUT SUPPLY CONNECTIONS

Note: the internal bias regulators are not designed to be outputs for powering other circuitry. Do not attach external loads to any of these pins. The multi-mode pins may be connected to the V25 pin for logic HIGH settings.

Output Voltage Selection

STANDARD MODE

The output voltage may be set to any voltage between 0.6V and 3.6V provided that the input voltage is higher than the desired output voltage by an amount sufficient to prevent the device from exceeding its maximum duty cycle specification. Using the pin-strap method, V_{OUT} can be set to any of nine standard voltages as shown in Table 2.

TABLE 2. PIN-STRAP OUTPUT VOLTAGE SETTINGS

		V0		
		LOW	OPEN	HIGH
V1	LOW	0.6V	0.8V	1.0V
	OPEN	1.2V	1.5V	1.8V
	HIGH	2.5V	3.3V	3.6V

The resistor setting method can be used to set the output voltage to levels not available in Table 2. Resistors R0 and R1 are selected to produce a specific voltage between 0.6V and 3.6V in 10mV steps. Resistor R1 provides a coarse setting and resistor R0 provides a fine adjustment, thus eliminating the additional errors associated with using two 1% resistors (this typically adds 1.4% error).

To set V_{OUT} using resistors, follow the steps below to calculate an index value and then use Table 3 to select the resistor that corresponds to the calculated index value as follows:

1. Calculate Index1: Index1 = 4 x V_{OUT} (V_{OUT} in 10mV steps)
2. Round the result down to the nearest whole number.

3. Select the value of R1 from Table 3 using the Index1 rounded value from Step 2.
4. Calculate Index0: $\text{Index0} = 100 \times V_{\text{OUT}} - (25 \times \text{Index1})$
5. Select the value of R0 from Table 3 using the Index0 value from Step 4.

TABLE 3. RESISTORS FOR SETTING OUTPUT VOLTAGE

INDEX	R0 OR R1 (kΩ)
0	10
1	11
2	12.1
3	13.3
4	14.7
5	16.2
6	17.8
7	19.6
8	21.5
9	23.7
10	26.1
11	28.7
12	31.6
13	34.8
14	38.3
15	42.2
16	46.4
17	51.1
18	56.2
19	61.9
20	68.1
21	75
22	82.5
23	90.9
24	100

Example from Figure 9: For $V_{\text{OUT}} = 1.33\text{V}$,

$\text{Index1} = 4 \times 1.33\text{V} = 5.32$;

From Table 3, $R1 = 16.2\text{k}\Omega$

$\text{Index0} = (100 \times 1.33\text{V}) - (25 \times 5) = 8$;

From Table 3, $R0 = 21.5\text{k}\Omega$

The output voltage can be determined from the R0 (Index0) and R1 (Index1) values using Equation 1:

$$V_{\text{OUT}} = \frac{\text{Index0} + (25 \times \text{Index1})}{100} \quad (\text{EQ. 1})$$

The output voltage may also be set to any value between 0.6V and 3.6V using the I²C interface. See Application Note [AN2033](#) for details.

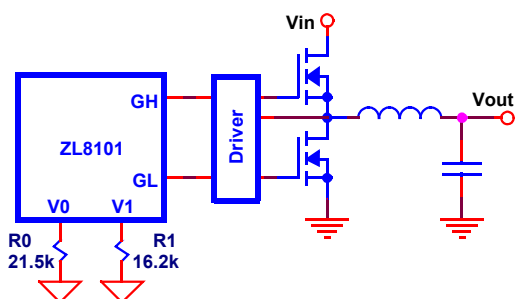


FIGURE 9. OUTPUT VOLTAGE RESISTOR SETTING EXAMPLE

Single Resistor Output Voltage Setting Mode

Some applications desire the output voltage to be set using a single resistor. This can be accomplished using a resistor on the V1 pin while the V0 pin is tied to SGND. Table 4 lists the available output voltage settings with a single resistor. See Application Note [AN2033](#) for more details.

TABLE 4.

$R_{V1}(\text{k}\Omega)$	R_{V0}	V_{OUT}
10	Low	0.60
11	Low	0.65
12.1	Low	0.70
13.3	Low	0.75
14.7	Low	0.80
16.2	Low	0.85
17.8	Low	0.90
19.6	Low	0.95
21.5	Low	1.00
23.7	Low	1.05
26.1	Low	1.10
28.7	Low	1.15
31.6	Low	1.20
34.8	Low	1.25
38.3	Low	1.30
42.2	Low	1.40
46.4	Low	1.50
51.1	Low	1.60
56.2	Low	1.70
61.9	Low	1.80
68.1	Low	1.90
75.0	Low	2.00
82.5	Low	2.10
90.9	Low	2.20
100	Low	2.30

ZL8101

TABLE 4. (Continued)

$R_{V1}(k\Omega)$	R_{VO}	V_{OUT}
110	Low	2.50
121	Low	3.00
133	Low	3.30
147	Low	4.00
162	Low	5.00
178	Low	5.50

Start-up Procedure

The ZL8101 follows a specific internal start-up procedure after power is applied to the VDD pin. Table 5 describes the start-up sequence.

If the device is to be synchronized to an external clock source, the clock frequency must be stable prior to asserting the EN pin. The device requires approximately 5ms to 10ms to check for specific values stored in its internal memory. If the user has stored values in memory, those values will be loaded. The device will then check the status of all multi-mode pins and load the values associated with the pin settings.

Once this process is completed, the device is ready to accept commands via the I²C/SMBus interface and the device is ready to be enabled. Once enabled, the device requires approximately 2ms before its output voltage may be allowed to start its ramp-up process. If a soft-start delay period less than 2ms has

been configured (using PMBus commands), the device will default to a 2ms delay period (with an accuracy of approximately ± 0.25 ms). If a delay period greater than 2ms is configured, the device will wait for the configured delay period prior to starting to ramp its output.

After the delay period has expired, the output will begin to ramp towards its target voltage according to the pre-configured soft-start ramp time that has been set using the SS pin.

Soft-start Delay and Ramp Times

In some applications, it may be necessary to set a delay from when an enable signal is received until the output voltage starts to ramp to its target value. In addition, the designer may wish to precisely set the time required for V_{OUT} to ramp to its target value after the delay period has expired. These features may be used as part of an overall inrush current management strategy or to precisely control how fast a load IC is turned on. The ZL8101 gives the system designer several options for precisely and independently controlling both the delay and ramp time periods.

The soft-start delay period begins when the EN pin is asserted and ends when the delay time expires. The soft-start delay period is set using the SS pin.

The soft-start ramp timer enables a precisely controlled ramp to the nominal V_{OUT} value that begins once the delay period has expired. The ramp-up is guaranteed monotonic and its slope may be precisely set using the SS pin.

The soft-start delay and ramp times can be set to standard values according to Table 6.

TABLE 5. ZL8101 START-UP SEQUENCE

STEP #	STEP NAME	DESCRIPTION	TIME DURATION
1	Power Applied	Input voltage is applied to the ZL8101's VDD pin	Depends on input supply ramp time
2	Internal Memory Check	The device will check for values stored in its internal memory. This step is also performed after a Restore command.	Approx 5ms to 10ms (device will ignore an enable signal or PMBus traffic during this period)
3	Multi-mode Pin Check	The device loads values configured by the multi-mode pins.	
4	Device Ready	The device is ready to accept an enable signal.	-
5	Pre-ramp Delay	The device requires approximately 2ms following an enable signal and prior to ramping its output. Additional pre-ramp delay may be configured using the Delay pins.	Approximately 2ms

TABLE 6. SOFT-START RAMP SETTINGS

R _{SS} (kΩ)	SS DELAY (ms)	SS RAMP (ms)	UVLO (V)
LOW	2	2	4.5
OPEN	5	5	
HIGH	10	10	
10	2	2	4.5
11		5	
12.1		10	
13.3	5	2	
14.7		5	
16.2		10	
17.8		20	
19.6	10	2	
21.5		5	
23.7		10	
26.1		20	
28.7	20	2	
31.6		5	
34.8		10	
38.3		20	
42.2	2	2	10.8
46.4		5	
51.1		10	
56.2		20	
61.9	5	2	
68.1		5	
75		10	
82.5		20	
90.9	10	2	
100		5	
110		10	
121		20	
133	20	2	
147		5	
162		10	
178		20	

Note that when Auto Compensation is enabled, the minimum TON_DELAY is 5ms.

The value of this resistor is measured upon start-up or Restore and will not change if the resistor is varied after power has been applied to the ZL8101. See Figure 10 for typical connections using resistors.

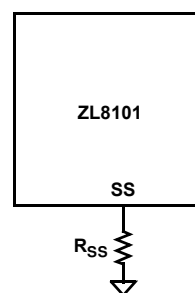


FIGURE 10. SS PIN RESISTOR CONNECTIONS

If the desired soft-start delay and ramp times are not one of the values listed in Table 6, the times can be set to a custom value via the I²C/SMBus interface. When the SS delay time is set to 0ms, the device will begin its ramp after the internal circuitry has initialized (~2ms). The soft-start ramp period may be set to values less than 2ms, however it is generally recommended to set the soft-start ramp to a value greater than 500μs to prevent inadvertent fault conditions due to excessive inrush current.

Power-Good

The ZL8101 provides a Power-Good (PG) signal that indicates the output voltage is within a specified tolerance of its target level and no fault condition exists. By default, the PG pin will assert if the output is within -10%/+15% of the target voltage. These limits and the polarity of the pin may be changed via the I²C/SMBus interface. See Application Note [AN2033](#) for details.

A PG delay period is defined as the time from when all conditions within the ZL8101 for asserting PG are met, to when the PG pin is actually asserted. This feature is commonly used instead of using an external reset controller to control external digital logic. By default, the ZL8101 PG delay is set equal to the soft-start ramp time setting. Therefore, if the soft-start ramp time is set to 10ms, the PG delay will be set to 10ms. The PG delay may be set independently of the soft-start ramp using the I²C/SMBus as described in Application Note AN2033.

Switching Frequency and PLL

The ZL8101 incorporates an internal phase-locked loop (PLL) to clock the internal circuitry. The PLL can be driven by an external clock source connected to the SYNC pin. When using the internal oscillator, the SYNC pin can be configured as a clock source for other Zilker Labs devices.

The SYNC pin is a unique pin that can perform multiple functions depending on how it is configured.

CONFIGURATION A: SYNC OUTPUT

When the SYNC pin is configured as an output, the device will run from its internal oscillator and will drive the resulting internal oscillator signal (preset to 400kHz) onto the SYNC pin so other devices can be synchronized to it. The SYNC pin will not be checked for an incoming clock signal while in this mode. This mode is only available using the I²C/SMBus as described in Application Note AN2033.

CONFIGURATION B: SYNC INPUT

When the SYNC pin is configured as an input, the device will automatically check for a clock signal on the SYNC pin each time EN is asserted. The ZL8101's oscillator will then synchronize with the rising edge of the external clock. The internal clock must be configured to the nearest available frequency to the external clock, to minimize output perturbations if the external clock is lost.

The incoming clock signal must be in the range of 200kHz to 1.4MHz and must be stable when the enable pin is asserted. The clock signal must also exhibit the necessary performance requirements (see the "Electrical Specifications" table beginning on page 6). In the event of a loss of the external clock signal, the output voltage may show transient over/undershoot.

If this happens, the ZL8101 will automatically switch to its internal oscillator and switch at a frequency close to the previous incoming frequency. This mode is only available using the

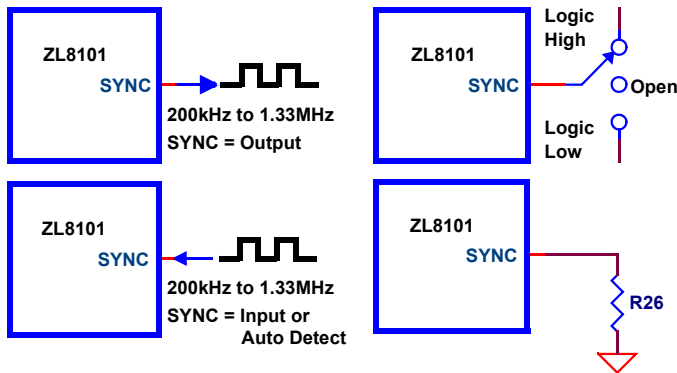


FIGURE 11. SYNC PIN CONFIGURATIONS

I²C/SMBus as described in Application Note [AN2033](#).

SYNC AUTO DETECT

When the SYNC pin is configured in auto detect mode, the device will automatically check for a clock signal on the SYNC pin after enable is asserted.

If a clock signal is present, The ZL8101's oscillator will then synchronize the rising edge of the external clock.

If no incoming clock signal is present, the ZL8101 will configure the switching frequency according to the state of the SYNC pin as listed in Table 7. In this mode, the ZL8101 will only read the SYNC pin connection during the start-up sequence. Changes to

SYNC pin connections will not affect f_{sw} until the power (VDD) is cycled off and on.

TABLE 7. SWITCHING FREQUENCY SELECTION

SYNC PIN	FREQUENCY
LOW	200kHz
OPEN	400kHz
HIGH	1MHz
Resistor	See Table 8

If the user desires to configure other frequencies not listed in Table 7, the switching frequency can also be set to any value between 200kHz and 1.33MHz using the I²C/SMBus interface. The available frequencies below 1.4MHz are defined by $f_{sw} = 8MHz/N$, where $6 \leq N \leq 40$. See Application Note [AN2033](#) for details.

If a value other than $f_{sw} = 8MHz/N$ is entered using a PMBus command, the internal circuitry will select the switching frequency value using N as a whole number to achieve a value close to the entered value. For example, if 810kHz is entered, the device will select 800kHz (N = 10).

TABLE 8. R_{SYNC} RESISTOR VALUES

R _{SYNC} (kΩ)	f _{sw} (kHz)
10	200
11	222
12.1	242
13.3	267
14.7	296
16.2	320
17.8	364
19.6	400
21.5	421
23.7	471
26.1	533
28.7	571
31.6	615
34.8	727
38.3	800
46.4	889
51.1	1000
56.2	1143
68.1	1333

When multiple Zilker Labs devices are used together, connecting the SYNC pins together will force all devices to synchronize with each other. One of the devices must be configured as a Sync source and the remaining devices must be configured as a Sync input. The I²C/SMBus must be used to configure the Sync Pin.

Note: The switching frequency read back using the appropriate PMBus command will differ slightly from the selected values in Table 8. The difference is due to hardware quantization.

Power Train Component Selection

The ZL8101 is a synchronous buck converter that uses external Driver, MOSFETs, inductor and capacitors to perform the power conversion process. The proper selection of the external components is critical for optimized performance.

To select the appropriate external components for the desired performance goals, the power supply requirements listed in Table 9 must be known.

TABLE 9. POWER SUPPLY REQUIREMENTS

PARAMETER	RANGE	EXAMPLE VALUE
Input voltage (V_{IN})	4.5V to 14.0V	12V
Output voltage (V_{OUT})	0.6V to 3.6V	1.2V
Output current (I_{OUT})	0A to ~25A	20A
Output voltage ripple (V_{ORIP})	< 3% of V_{OUT}	1% of V_{OUT}
Output load step (I_{OSTEP})	< I_O	50% of I_O
Output load step rate	-	10A/ μ s
Output deviation due to load step	-	\pm 50mV
Maximum PCB temp.	+120 °C	+85 °C
Desired efficiency	-	85%
Other considerations	Various	Optimize for small size

DESIGN GOAL TRADE-OFFS

The design of the buck power stage requires several compromises among size, efficiency, and cost. The inductor core loss increases with frequency, so there is a trade-off between a small output filter made possible by a higher switching frequency and getting better power supply efficiency. Size can be decreased by increasing the switching frequency at the expense of efficiency. Cost can be minimized by using through-hole inductors and capacitors; however these components are physically large.

To start the design, select a switching frequency based on Table 10. This frequency is a starting point and may be adjusted as the design progresses.

TABLE 10. CIRCUIT DESIGN CONSIDERATIONS

FREQUENCY RANGE	EFFICIENCY	CIRCUIT SIZE
200kHz to 400kHz	Highest	Larger
400kHz to 800kHz	Moderate	Smaller
800kHz to 1.4MHz	Lower	Smallest

DRIVER SELECTION

The ZL8101 requires an external driver, the recommended 2-input companion driver is the ZL1505 with integrated 30V bootstrap Schottky diode. The ZL1505 has independent PWMH

and PWML inputs to take advantage of the dynamic dead-time control on the ZL8101.

The ZL8101 can be used with other driver devices, like the ISL6611 Phase Doubler Driver and several DrMOS type drivers. Please check with Intersil if you are not sure about compatibility.

INDUCTOR SELECTION

The output inductor selection process must include several trade-offs. A high inductance value will result in a low ripple current (I_{opp}), which will reduce output capacitance and produce a low output ripple voltage, but may also compromise output transient load performance. Therefore, a balance must be struck between output ripple and optimal load transient performance. A good starting point is to select the output inductor ripple equal to the expected load transient step magnitude (I_{ostep}):

$$I_{opp} = I_{ostep} \quad (\text{EQ. 2})$$

Now the output inductance can be calculated using Equation 3, where V_{INM} is the maximum input voltage:

$$L_{OUT} = \frac{V_{OUT} \times \left(1 - \frac{V_{OUT}}{V_{INM}}\right)}{f_{sw} \times I_{opp}} \quad (\text{EQ. 3})$$

The average inductor current is equal to the maximum output current. The peak inductor current (I_{Lpk}) is calculated using Equation 4 where I_{OUT} is the maximum output current:

$$I_{Lpk} = I_{OUT} + \frac{I_{opp}}{2} \quad (\text{EQ. 4})$$

Select an inductor rated for the average DC current with a peak current rating above the peak current computed in Equation 4.

In overcurrent or short-circuit conditions, the inductor may have currents greater than 2X the normal maximum rated output current. It is desirable to use an inductor that still provides some inductance to protect the load and the MOSFETs from damaging currents in this situation.

Once an inductor is selected, the DCR and core losses in the inductor are calculated. Use the DCR specified in the inductor manufacturer's datasheet.

$$P_{LDCR} = DCR \times I_{Lrms}^2 \quad (\text{EQ. 5})$$

I_{Lrms} is given by Equation 6:

$$I_{Lrms} = \sqrt{I_{OUT}^2 + \frac{(I_{opp})^2}{12}} \quad (\text{EQ. 6})$$

where I_{OUT} is the maximum output current. Next, calculate the core loss of the selected inductor. Since this calculation is specific to each inductor and manufacturer, refer to the chosen inductor datasheet. Add the core loss and the ESR loss and compare the total loss to the maximum power dissipation recommendation in the inductor datasheet.

OUTPUT CAPACITOR SELECTION

Several trade-offs must also be considered when selecting an output capacitor. Low ESR values are needed to have a small output deviation during transient load steps (V_{osag}) and low output voltage ripple (V_{orip}). However, capacitors with low ESR, such as semi-stable (X5R and X7R) dielectric ceramic capacitors, also have relatively low capacitance values. Many designs can use a combination of high capacitance devices and low ESR devices in parallel.

For high ripple currents, a low capacitance value can cause a significant amount of output voltage ripple. Likewise, in high transient load steps, a relatively large amount of capacitance is needed to minimize the output voltage deviation while the inductor current ramps up or down to the new steady state output current value.

As a starting point, apportion one-half of the output ripple voltage to the capacitor ESR and the other half to capacitance, as shown in Equations 7 and 8:

$$C_{OUT} = \frac{I_{opp}}{8 \times f_{sw} \times \frac{V_{orip}}{2}} \quad (\text{EQ. 7})$$

$$ESR = \frac{V_{orip}}{2 \times I_{opp}} \quad (\text{EQ. 8})$$

Use these values to make an initial capacitor selection, using a single capacitor or several capacitors in parallel.

After a capacitor has been selected, the resulting output voltage ripple can be calculated using Equation 9:

$$V_{orip} = I_{opp} \times ESR + \frac{I_{opp}}{8 \times f_{sw} \times C_{OUT}} \quad (\text{EQ. 9})$$

Because each part of this equation was made to be less than or equal to half of the allowed output ripple voltage, the V_{orip} should be less than the desired maximum output ripple.

INPUT CAPACITOR

It is highly recommended that dedicated input capacitors be used in any point-of-load design, even when the supply is powered from a heavily filtered 5V or 12V “bulk” supply from an off-line power supply. This is because of the high RMS ripple current that is drawn by the buck converter topology. This ripple (I_{CINrms}) can be determined from Equation 10:

$$I_{CINrms} = I_{OUT} \times \sqrt{D \times (1 - D)} \quad (\text{EQ. 10})$$

Without capacitive filtering near the power supply circuit, this current would flow through the supply bus and return planes, coupling noise into other system circuitry. The input capacitors should be rated at 1.2X the ripple current calculated above to avoid overheating of the capacitors due to the high ripple current, which can cause premature failure. Ceramic capacitors with X7R or X5R dielectric with low ESR and 1.1X the maximum expected input voltage are recommended.

QL SELECTION

The bottom MOSFET should be selected primarily based on the device's $r_{DS(ON)}$ and secondarily based on its gate charge. To choose QL, use Equation 11 and allow 2% to 5% of the output power to be dissipated in the $r_{DS(ON)}$ of QL (lower output voltages and higher step-down ratios will be closer to 5%):

$$P_{QL} = 0.05 \times V_{OUT} \times I_{OUT} \quad (\text{EQ. 11})$$

Calculate the RMS current in QL as follows:

$$I_{botrms} = I_{Lrms} \times \sqrt{1 - D} \quad (\text{EQ. 12})$$

Calculate the desired maximum $r_{DS(ON)}$ as follows:

$$R_{DS(ON)} = \frac{P_{QL}}{(I_{botrms})^2} \quad (\text{EQ. 13})$$

Note that the $r_{DS(ON)}$ given in the manufacturer's datasheet is measured at +25°C. The actual $r_{DS(ON)}$ in the end-use application will be much higher. For example, a Vishay Si7114 MOSFET with a junction temperature of +125°C has an $r_{DS(ON)}$ that is 1.4 times higher than the value at +25°C. Select a candidate MOSFET, and calculate the required gate drive current as follows:

$$I_g = f_{sw} \times Q_g \quad (\text{EQ. 14})$$

Keep in mind that the total allowed gate drive current for both QH and QL is 80mA.

MOSFETs with lower $r_{DS(ON)}$ tend to have higher gate charge requirements, which increases the current and resulting power required to turn them on and off. Since the MOSFET gate drive circuits are integrated in the ZL1505, this power is dissipated in the ZL1505 according to Equation 15:

$$P_{QL} = f_{sw} \times Q_g \times V_{INM} \quad (\text{EQ. 15})$$

QH SELECTION

In addition to the $r_{DS(ON)}$ loss and gate charge loss, QH also has switching loss. The procedure to select QH is similar to the procedure for QL. First, assign 2% to 5% of the output power to be dissipated in the $r_{DS(ON)}$ of QH using the Equation 11 for QL. As was done with QL, calculate the RMS current as follows:

$$I_{toprms} = I_{Lrms} \times \sqrt{D} \quad (\text{EQ. 16})$$

Calculate a starting $r_{DS(ON)}$ as follows, in this example using 5%:

$$P_{QH} = 0.05 \times V_{OUT} \times I_{OUT} \quad (\text{EQ. 17})$$

$$R_{DS(ON)} = \frac{P_{QH}}{(I_{toprms})^2} \quad (\text{EQ. 18})$$

Select a MOSFET and calculate the resulting gate drive current. Verify that the combined gate drive current from QL and QH does not exceed 80mA.

Next, calculate the switching time using Equation 19:

$$t_{sw} = \frac{Q_g}{I_{gdr}} \quad (\text{EQ. 19})$$

where Q_g is the gate charge of the selected QH and I_{gdr} is the peak gate drive current available from the ZL1505.

Although the ZL1505 has a typical gate drive current of 3.2A, use the minimum guaranteed current of 2A for a conservative design. Using the calculated switching time, calculate the switching power loss in QH using Equation 20:

$$P_{swtop} = V_{INM} \times t_{sw} \times I_{OUT} \times f_{sw} \quad (\text{EQ. 20})$$

The total power dissipated by QH is given by Equation 21:

$$P_{QHtot} = P_{QH} + P_{swtop} \quad (\text{EQ. 21})$$

MOSFET THERMAL CHECK

Once the power dissipations for QH and QL have been calculated, the MOSFET's junction temperature can be estimated. Using the junction-to-case thermal resistance (R_{th}) given in the MOSFET manufacturer's datasheet and the expected maximum printed circuit board temperature, calculate the junction temperature as shown in Equation 22:

$$T_{jmax} = T_{pcb} + (P_Q \times R_{th}) \quad (\text{EQ. 22})$$

CURRENT SENSING COMPONENTS

Once the current sense method has been selected (refer to "Current Limit Threshold Selection" on page 22), the components are selected as follows.

When using the inductor DCR sensing method, the user must also select an R/C network comprised of R_1 and C_L (see Figure 12).

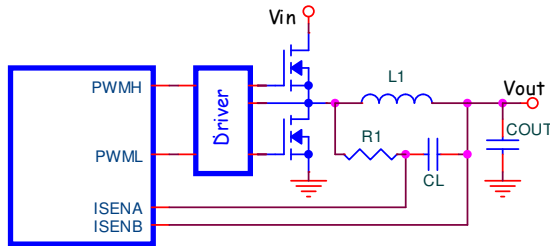


FIGURE 12. DCR CURRENT SENSING

For the voltage across C_L to reflect the voltage across the DCR of the inductor, the time constant of the inductor must match the time constant of the RC network. That is:

$$\tau_{RC} = \tau_{L/DCR} \quad (\text{EQ. 23})$$

$$R_1 \cdot C_L = \frac{L}{DCR}$$

For L , use the average of the nominal value and the minimum value. Include the effects of tolerance, DC Bias and switching frequency on the inductance when determining the minimum value of L . Use the typical value for DCR.

The value of R_1 should be as small as feasible and no greater than $5k\Omega$ for best signal-to-noise ratio. The designer should make sure the resistor package size is appropriate for the power dissipated and include this loss in efficiency calculations. In calculating the minimum value of R_1 , the average voltage across C_L (which is the average I_{OUT} DCR product) is small and can be neglected. Therefore, the minimum value of R_1 may be approximated by Equation 24:

$$R_{1-min} = \frac{D(V_{IN-max} - V_{OUT})^2 + (1-D) \cdot V_{OUT}^2}{P_{R1pkg-max} \cdot \delta_P} \quad (\text{EQ. 24})$$

where $P_{R1pkg-max}$ is the maximum power dissipation specification for the resistor package and δ_P is the derating factor for the same parameter (e.g.: $P_{R1pkg-max} = 0.0625W$ for 0603 package, $\delta_P = 50\%$ @ $+85^\circ C$). Once R_{1-min} has been calculated, solve for the maximum value of C_L from Equation 25:

$$C_{L-max} = \frac{L}{R_{1-min} \cdot DCR} \quad (\text{EQ. 25})$$

and choose the next-lowest readily available value (e.g., for $C_{L-max} = 1.86\mu F$, $C_L = 1.5\mu F$ is a good choice). Then substitute the chosen value into the same equation and re-calculate the value of R_1 . Choose the 1% resistor standard value closest to this re-calculated value of R_1 . The error due to the mismatch of the two time constants is:

$$\varepsilon_\tau = \left(1 - \frac{R_1 \cdot C_L \cdot DCR}{L_{avg}} \right) \cdot 100\% \quad (\text{EQ. 26})$$

Current Limit Threshold Selection

It is recommended that the user include a current limiting mechanism in their design to protect the power supply from damage and prevent excessive current from being drawn from the input supply in the event that the output is shorted to ground or an overload condition is imposed on the output. Current limiting is accomplished by sensing the current through the circuit during a portion of the duty cycle.

Output current sensing can be accomplished by measuring the voltage across a series resistive sensing element according to Equation 27:

$$V_{LIM} = I_{LIM} \times R_{SENSE} \quad (\text{EQ. 27})$$

Where:

I_{LIM} is the desired maximum current that should flow in the circuit

R_{SENSE} is the resistance of the sensing element

V_{LIM} is the voltage across the sensing element at the point the circuit should start limiting the output current.

The ZL8101 supports "lossless" current sensing, by measuring the voltage across a resistive element that is already present in the circuit. This eliminates additional efficiency losses incurred by devices that must use an additional series resistance in the circuit.

To set the current limit threshold, the user must first select a current sensing method. The ZL8101 incorporates inductor DC

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resistance (DCR) sensing; Figure 12 shows a simplified schematic for DCR method. $r_{DS(ON)}$ method is not supported.

Advanced ILIM pinstrapping options are not available for the ZL8101. However, all current limit and fault response options are available when using I²C/SMBus interface and configuration file.

The blanking time represents the time when no current measurement is taken. This is to avoid taking a reading just after a coincident switching edge (less accurate due to potential ringing). Blanking time is a configurable parameter.

ZL8101 provides an adjustable maximum full scale sensing range. The available ranges are 25mV, 35mV and 50mV using the I²C/SMBus interface or a configuration file. Table 11 lists the factory default value for the current limit function.

TABLE 11. FACTORY DEFAULT ILIM CONFIGURATION

CURRENT LIMITING CONFIGURATION	NUMBER OF VIOLATIONS ALLOWED	CURRENT LIMIT THRESHOLD V_{LIM} (mV)	MAXIMUM CURRENT SENSING RANGE (mV)
Output-referenced, down-slope sensing (Inductor DCR sensing) Blanking time: 480ns	7	50	50

The user must select the voltage threshold (V_{LIM}), the desired current limit threshold, and the resistance of the sensing element.

The current limit threshold must be set to a custom value via the I²C/SMBus interface. Please refer to Application Note [AN2033](#) for further details.

Loop Compensation

The ZL8101 has an auto compensation feature that measures the characteristics of the power train and calculates the proper tap coefficients. Auto compensation is configured using the FC pin as shown in Table 12.

TABLE 12. PIN #9 (FC) AUTO COMPENSATION MODE

R_{FC} (k Ω)	STORE VALUES	SINGLE/ REPEAT	PG ASSERT	AUTO COMP GAIN
LOW	Auto Comp Disabled			
OPEN	Not Stored	Single	After Auto Comp	100%
HIGH	Store in Flash	Single	After Auto Comp	

TABLE 12. PIN #9 (FC) AUTO COMPENSATION MODE (Continued)

R_{FC} (k Ω)	STORE VALUES	SINGLE/ REPEAT	PG ASSERT	AUTO COMP GAIN
10	Not Stored	Single	After Auto Comp	100%
11	Store in Flash			
12.1	Not Stored	Repeat 1s	After PG Delay	
13.3	Store in Flash			
14.7	Not Stored	Single	After PG Delay	
16.2	Store in Flash			
17.8	Not Stored	Repeat 1s	After Auto Comp	
19.6	Store in Flash			
OPEN	Not Stored	Single	After Auto Comp	
HIGH/ 21.5	Store in Flash			
23.7	Not Stored	Repeat 1min	After PG Delay	
26.1	Store in Flash			
28.7	Not Stored	Single	After PG Delay	
31.6	Store in Flash			
34.8	Not Stored	Repeat 1min	After Auto Comp	
38.3	Store in Flash			
42.2	Not Stored	Single	After Auto Comp	
46.4	Store in Flash			
51.1	Not Stored	Repeat 1s	After PG Delay	
56.2	Store in Flash			
61.9	Not Stored	Single	After PG Delay	
68.1	Store in Flash			
75	Not Stored	Repeat 1s	After Auto Comp	
82.5	Store in Flash			
90.9	Not Stored	Single	After Auto Comp	
100	Store in Flash			
110	Not Stored	Repeat 1min	After PG Delay	
121	Store in Flash			
133	Not Stored	Single	After PG Delay	
147	Store in Flash			
162	Not Stored	Repeat 1min	After Auto Comp	
178	Store in Flash			

When auto compensation is enabled, the routine can be set to execute one time after ramp or periodically while regulating. Note that the Auto Compensation feature requires a minimum TON_DELAY as described in "Soft-Start Delay and Ramp Times" on page 16.

If the device is configured to store auto comp values, the calculated compensation values will be saved in the Auto Comp Store and may be read back through the PID_TAPS command. If repeat mode is enabled, the first Auto Comp results after the first ramp will be stored; the values calculated periodically are not stored in the Auto Comp Store. When compensation values are saved in the Auto Comp Store, the device will use those compensation values on subsequent ramps. In repeat mode, the latest Auto Comp results will always be used during operation. Stored Auto Comp results can only be cleared by disabling Auto Comp Store, which is not permitted while the output is enabled. However, sending the AUTOCOMP_CONTROL command while enabled in Store mode will cause the next results to be stored, overwriting previously stored values. If auto compensation is disabled, the device will use the compensation parameters that are stored in the DEFAULT_STORE or USER_STORE.

If the PG Assert parameter is set to "Use PG Delay," PG will be asserted according to the POWER_GOOD_DELAY command. When Auto Comp is enabled, the user must not program a Power-Good Delay that will expire before the ramp is finished. If PG Assert is set to "After Auto Comp," PG will be asserted immediately after the first Auto Comp cycle completes (POWER_GOOD_DELAY will be ignored). The Auto Comp Gain control scales the Auto Comp results to allow a trade-off between transient response and steady-state duty cycle jitter. A setting of 100% will provide the fastest transient response while a setting of 10% will produce the lowest jitter. Note that if Auto Comp is enabled, for best results Vin must be stable before Auto Comp begins, as shown in Equation 28. The auto compensation function can also be configured via the AUTO_COMP_CONFIG command and controlled using the AUTO_COMP_CONTROL command over the I²C/SMBus interface. Please refer to Application Note AN2033 for further details.

$$\frac{\Delta V_{in}}{V_{inNom}} (\text{in}\%) \leq \frac{100\%}{1 + \frac{256 \cdot V_{out}}{V_{inNom}}} \quad (\text{EQ. 28})$$

Non-linear Response (NLR) Settings

The ZL8101 incorporates a non-linear response (NLR) loop that decreases the response time and the output voltage deviation in the event of a sudden output load current step. The NLR loop incorporates a secondary error signal processing path that bypasses the primary error loop when the output begins to transition outside of the standard regulation limits. This scheme results in a higher equivalent loop bandwidth than what is possible using a traditional linear loop.

When a load current step function imposed on the output causes the output voltage to drop below the lower regulation limit, the NLR circuitry will force a positive correction signal that will turn on the upper MOSFET and quickly force the output to increase. Conversely, a negative load step (i.e., removing a large load current) will cause the NLR circuitry to force a negative correction signal that will turn on the lower MOSFET and quickly force the

output to decrease. The ZL8101 has been pre-configured with appropriate NLR settings that correspond to the loop compensation settings in Table 13.

Efficiency Optimized Driver Dead-time Control

The ZL8101 utilizes a closed loop algorithm to optimize the dead-time applied between the gate drive signals for the top and bottom FETs. In a synchronous buck converter, the MOSFET drive circuitry must be designed such that the top and bottom MOSFETs are never in the conducting state at the same time. Potentially damaging currents flow in the circuit if both top and bottom MOSFETs are simultaneously on for periods of time exceeding a few nanoseconds. Conversely, long periods of time in which both MOSFETs are off reduce overall circuit efficiency by allowing current to flow in their parasitic body diodes.

It is therefore advantageous to minimize this dead-time to provide optimum circuit efficiency. In the first order model of a buck converter, the duty cycle is determined by Equation 29:

$$D \approx \frac{V_{OUT}}{V_{IN}} \quad (\text{EQ. 29})$$

However, non-idealities exist that cause the real duty cycle to extend beyond the ideal. Dead-time is one of those non-idealities that can be manipulated to improve efficiency. The ZL8101 has an internal algorithm that constantly adjusts dead-time non-overlap to minimize duty cycle, thus maximizing efficiency.

This circuit will null out dead-time differences due to component variation, temperature, and loading effects.

This algorithm is independent of application circuit parameters such as MOSFET type, gate driver delays, rise and fall times and circuit layout.

In addition, it does not require drive or MOSFET voltage or current waveform measurements.

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TABLE 13. PIN-STRAP SETTINGS FOR LOOP COMPENSATION

NLR	f_n RANGE	f_{zesr} RANGE	FC PIN (k Ω)
Off	$f_{sw}/60 < f_n < f_{sw}/30$	$f_{zesr} > f_{sw}/10$	10
		$f_{sw}/10 > f_{zesr} > f_{sw}/30$	11
		$f_{sw}/30 > f_{zesr} > f_{sw}/60$	12.1
	$f_{sw}/120 < f_n < f_{sw}/60$	$f_{zesr} > f_{sw}/10$	13.3
		$f_{sw}/10 > f_{zesr} > f_{sw}/30$	14.7
		$f_{sw}/30 > f_{zesr} > f_{sw}/60$	16.2
	$f_{sw}/240 < f_n < f_{sw}/120$	$f_{zesr} > f_{sw}/10$	17.8
		$f_{sw}/10 > f_{zesr} > f_{sw}/30$	19.6
		$f_{sw}/30 > f_{zesr} > f_{sw}/60$	21.5
On	$f_{sw}/60 < f_n < f_{sw}/30$	$f_{zesr} > f_{sw}/10$	23.7
		$f_{sw}/10 > f_{zesr} > f_{sw}/30$	26.1
		$f_{sw}/30 > f_{zesr} > f_{sw}/60$	28.7
	$f_{sw}/120 < f_n < f_{sw}/60$	$f_{zesr} > f_{sw}/10$	31.6
		$f_{sw}/10 > f_{zesr} > f_{sw}/30$	34.8
		$f_{sw}/30 > f_{zesr} > f_{sw}/60$	38.3
	$f_{sw}/240 < f_n < f_{sw}/120$	$f_{zesr} > f_{sw}/10$	42.2
		$f_{sw}/10 > f_{zesr} > f_{sw}/30$	46.4
		$f_{sw}/30 > f_{zesr} > f_{sw}/60$	51.1

Adaptive Diode Emulation

Most power converters use synchronous rectification to optimize efficiency over a wide range of input and output conditions. However, at light loads the synchronous MOSFET will typically sink current and introduce additional energy losses associated with higher peak inductor currents, resulting in reduced efficiency. Adaptive diode emulation mode turns off the low-side FET gate drive at low load currents to prevent the inductor current from going negative, reducing the energy losses and increasing overall efficiency. Diode emulation is available to single-phase devices only.

Note: the overall bandwidth of the device may be reduced when in diode emulation mode. It is recommended that diode emulation is disabled prior to applying significant load steps.

Power Management Functional Description

Input Undervoltage Lockout

The input undervoltage lockout (UVLO) prevents the ZL8101 from operating when the input falls below a preset threshold, indicating the input supply is out of its specified range. The UVLO threshold (V_{UVLO}) can be set between 4.5V and 10.8V using the SS pin. The simplest implementation is to connect the SS pin as shown in Table 6.

The UVLO voltage can also be set to any value between 2.85V and 16V via the I²C/SMBus interface.

Once an input undervoltage fault condition occurs, the device can respond in a number of ways as follows:

1. Continue operating without interruption.
2. Continue operating for a given delay period, followed by shutdown if the fault still exists. The device will remain in shutdown until instructed to restart.
3. Initiate an immediate shutdown until the fault has been cleared. The user can select a specific number of retry attempts.

The default response from a UVLO fault is an immediate shutdown of the device. The device will continuously check for the presence of the fault condition. If the fault condition is no longer present, the ZL8101 will be re-enabled.

Please refer to Application Note [AN2033](#) for details on how to configure the UVLO threshold or to select specific UVLO fault response options via the I²C/SMBus interface.

Output Overvoltage Protection

The ZL8101 offers an internal output overvoltage protection circuit that can be used to protect sensitive load circuitry from being subjected to a voltage higher than its prescribed limits. A hardware comparator is used to compare the actual output voltage (seen at the VSEN pin) to a threshold set to 15% higher than the target output voltage (the default setting). If the VSEN voltage exceeds this threshold, the PG pin will de-assert and the device can then respond in a number of ways as follows:

1. Initiate an immediate shutdown until the fault has been cleared. The user can select a specific number of retry attempts.
2. Turn off the high-side MOSFET and turn on the low-side MOSFET. The low-side MOSFET remains ON until the device attempts a restart.

The default response from an overvoltage fault is to immediately shut down. The device will continuously check for the presence of the fault condition, and when the fault condition no longer exists the device will be re-enabled.

For continuous overvoltage protection when operating from an external clock, the only allowed response is an immediate shutdown.

Refer to AN2033 for details on how to select specific overvoltage fault response options.

Output Pre-Bias Protection

An output pre-bias condition exists when an externally applied voltage is present on a power supply's output before the power supply's control IC is enabled. After enable is asserted the output voltage is sampled and the initial pulse width is set to match the existing pre-bias voltage and both drivers become active. The output voltage is then ramped to the target output voltage value at a rate equal to the configured T_{RISE} .

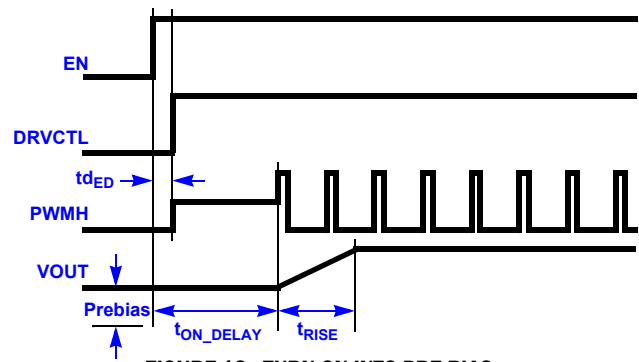


FIGURE 13. TURN-ON INTO PRE-BIAS

When using single input drivers or DrMOS devices the pre-bias is accommodated with the Tri-State PWMH and DRVCTL outputs. When DRVCTL is deasserted the control and Sync FET gates are active low. When DRVCTL is asserted PWMH becomes tri-state and both FET gates remain active low. After the configured t_{ON_DELAY} PWMH is adjusted to match the pre-bias voltage and VOUT will begin ramping from the pre-bias value. See Figure 13.

When powering down into a pre-bias VOUT is driven to 0V at a rate equal to the configured T_{fall} . After the tri-state delay ($3S_delay$) PWMH becomes tri-stated and VOUT will transition towards the pre-bias voltage. After the tri-state delay off period (td_{OFF}) DRVCTL de-asserts coincidentally with PWMH going active low. Both the Control and Sync FET will be active low and VOUT will ramp towards the pre-bias voltage. See Figure 14.

Minimum Duty Cycle

The ZL8101 is capable of producing output pulses as small as 5ns, however external drivers are not capable of pulses smaller than their minimum processing requirement. The minimum

required pulse width is often specified in the product data sheet. If the external driver is presented with pulse(s) below the minimum requirement the control pulse will not be processed and the gate-high output pulse will not be present. The driver will still deliver a complementary Gate-Low pulse. If a pre-bias is present the output will discharge towards zero until the PWM input is wide enough to meet the minimum required by the driver, this affect is shown in Figure 15.

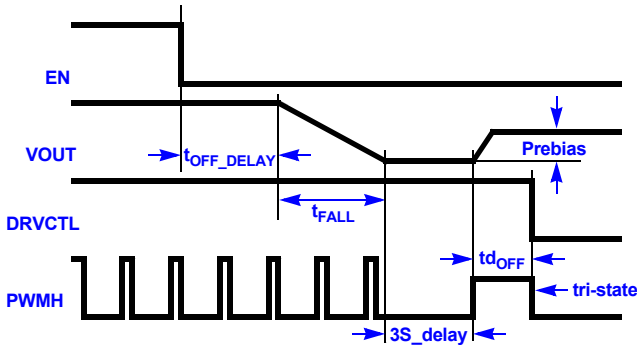


FIGURE 14. TURN_OFF WITH PRE_BIAS

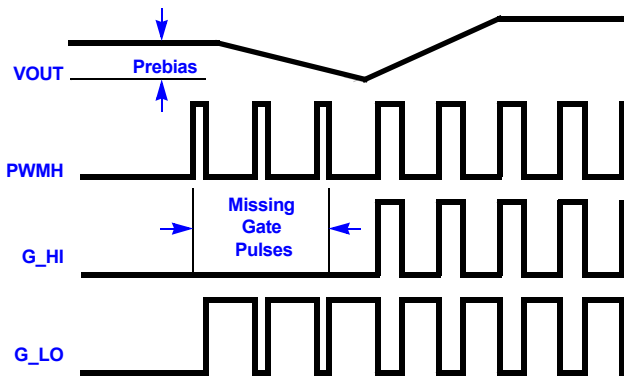


FIGURE 15. INITIAL PWM BELOW MINIMUM REQUIREMENT

To ensure that PWM pulses below the required minimum are not produced enable the Minimum Duty Cycle feature located within the USER_CONFIG field and select the option that is slightly above the minimum value required by the driver. The actual minimum duty cycle time is given by EQ 30.

$$\text{MinDuty} = N \times \frac{T_{sw}}{256} \quad (\text{EQ. 30})$$

N = Minimum Duty Cycle Count
 Tsw = Period of Switching Frequency
 MinDuty = Minimum Duty Cycle Time

The Minimum Duty Cycle parameter is also required to be set when configuring current sharing, enabling minimum a minimum duty cycle ensures that each controller produces a known initial pulse which helps balance inter-phase currents during ramps. Configure the minimum duty cycle to be slightly above the value specified in the driver data sheet.

The Minimum Duty Cycle parameter is part of the USER_CONFIG field and is comprised of the last 3 MSB's. The range of configurable values is shown below in Table 14.

TABLE 14. USER_CONFIG MIN DUTY HEX VALUES

MINIMUM DUTY CYCLE	
MINIMUM DUTY COUNT	USER_CONFIG
Disabled	0x00xx
2	0x40xx
4	0x80xx
6	0xC0xx
8	0x20xx
10	0x60xx
12	0xA0xx
14	0xE0xx

Output Overcurrent Protection

The ZL8101 can protect the power supply from damage if the output is shorted to ground or if an overload condition is imposed on the output. Once the current limit threshold has been selected (see "Current Limit Threshold Selection" on page 20), the user may determine the desired course of action in response to the fault condition. The following overcurrent protection response options are available:

1. Initiate a shutdown and attempt to restart an infinite number of times with a preset delay period between attempts.
2. Initiate a shutdown and attempt to restart a preset number of times with a preset delay period between attempts.
3. Continue operating for a given delay period, followed by shutdown if the fault still exists.
4. Continue operating through the fault (this could result in permanent damage to the power supply).
5. Initiate an immediate shutdown.

The default response from an overcurrent fault is an immediate shutdown of the device. The device will continuously check for the presence of the fault condition, and if the fault condition no longer exists the device will be re-enabled.

Refer to [AN2033](#) for details on how to select specific overcurrent fault response options.

Thermal Overload Protection

The ZL8101 includes an on-chip thermal sensor that continuously measures the internal temperature of the die and shuts down the device when the temperature exceeds the preset limit. The default temperature limit is set to +125 °C in the factory, but the user may set the limit to a different value if desired. See Application Note [AN2033](#) for details. Note that setting a higher thermal limit via the I²C/SMBus interface may result in permanent damage to the device. Once the device has been disabled due to an internal temperature fault, the user may select one of several fault response options as follows: