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Dual Channel/Dual Phase PMBus™ ChargeMode™ Control DC/DC Digital Controller

ZL8802

The ZL8802 is a dual output or dual phase digital DC/DC controller. Each output can operate independently or be used together in a dual phase configuration for high current applications supporting 2-, 4-, 6- and 8-phase operation with up to four ZL8802s.

The ZL8802 supports a wide range of output voltages (0.54V to 5.5V) operating from input voltages as low as 4.5V up to 14V.

With the fully digital ChargeMode control, the ZL8802 will respond to a transient load step within a single switching cycle. This unique compensation-free modulation technique allows designs to meet transient specifications with minimum output capacitance, thus saving cost and board space.

Intersil's proprietary single-wire DDC (Digital-DC™) serial bus enables the ZL8802 to communicate between other Intersil digital power ICs. By using the DDC, the ZL8802 achieves complex functions such as inter-IC phase current balancing, sequencing and fault spreading. This eliminates complicated power supply managers with numerous external discrete components.

The ZL8802 features fast output overcurrent protection. The input voltage, output voltages and DrMOS/MOSFET driver supply voltages are overvoltage and undervoltage protected. Two external and one internal temperature sensors are available for temperature monitoring, one of which can be configured for under- and over-temperature protection. A snapshot parametric capture feature allows users to take a snapshot of operating and fault data during normal or fault conditions.

Integrated Low Dropout (LDO) regulators allow the ZL8802 to operate from a single input supply eliminating the need for additional linear regulators. The VDRV LDO output can be used to power external drivers or DrMOS devices.

With full PMBus™ compliance, the ZL8802 is capable of measuring and reporting input voltage, input current, output voltage, output current as well as the device's internal temperature, 2 external temperatures and an auxiliary voltage or temperature input.

Features

- Unique compensation-free design – always stable
- Output voltage range: 0.54V to 5.5V
- Input voltage range: 4.5V to 14V
- 1% output voltage accuracy over line, load and temperature
- ChargeMode control achieves fast transient response, reduced output capacitance and provides output stability without compensation.
- 2-channel output, 2-, 4-, 6- or 8-phase output with 2, 3 or 4 devices
- Switching frequency range 200kHz to 1.33MHz
- Proprietary single-wire DDC (Digital-DC) serial bus enables voltage sequencing and fault spreading with other Intersil digital power ICs
- Inductor peak and averaged over and undercurrent protection
- Digital fault protection for output voltage UV/OV, input voltage UV/OV, temperature and MOSFET driver voltage
- Accurate average output current measurement with adjustable gain settings for sensing with SPS current monitor outputs or high current, low DCR inductors
- Monitor ADC measures input voltage, input current, output voltage, driver voltage, internal and external temperature
- Nonvolatile memory for storing operating parameters and fault events
- PMBus™ compliant

Applications

- Servers/storage equipment
- Telecom/datacom equipment
- Power supplies (memory, DSP, ASIC, FPGA)

TABLE 1. KEY DIFFERENCES BETWEEN FAMILY OF PARTS

PART NUMBER	DUAL OUTPUT	DUAL PHASE	DDC CURRENT SHARE	SPS SUPPORT
ZL8800	Yes	Yes	No	No
ZL8801	No	Yes	Yes	No
ZL8802	Yes	Yes	Yes	Yes

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Two-Phase Application

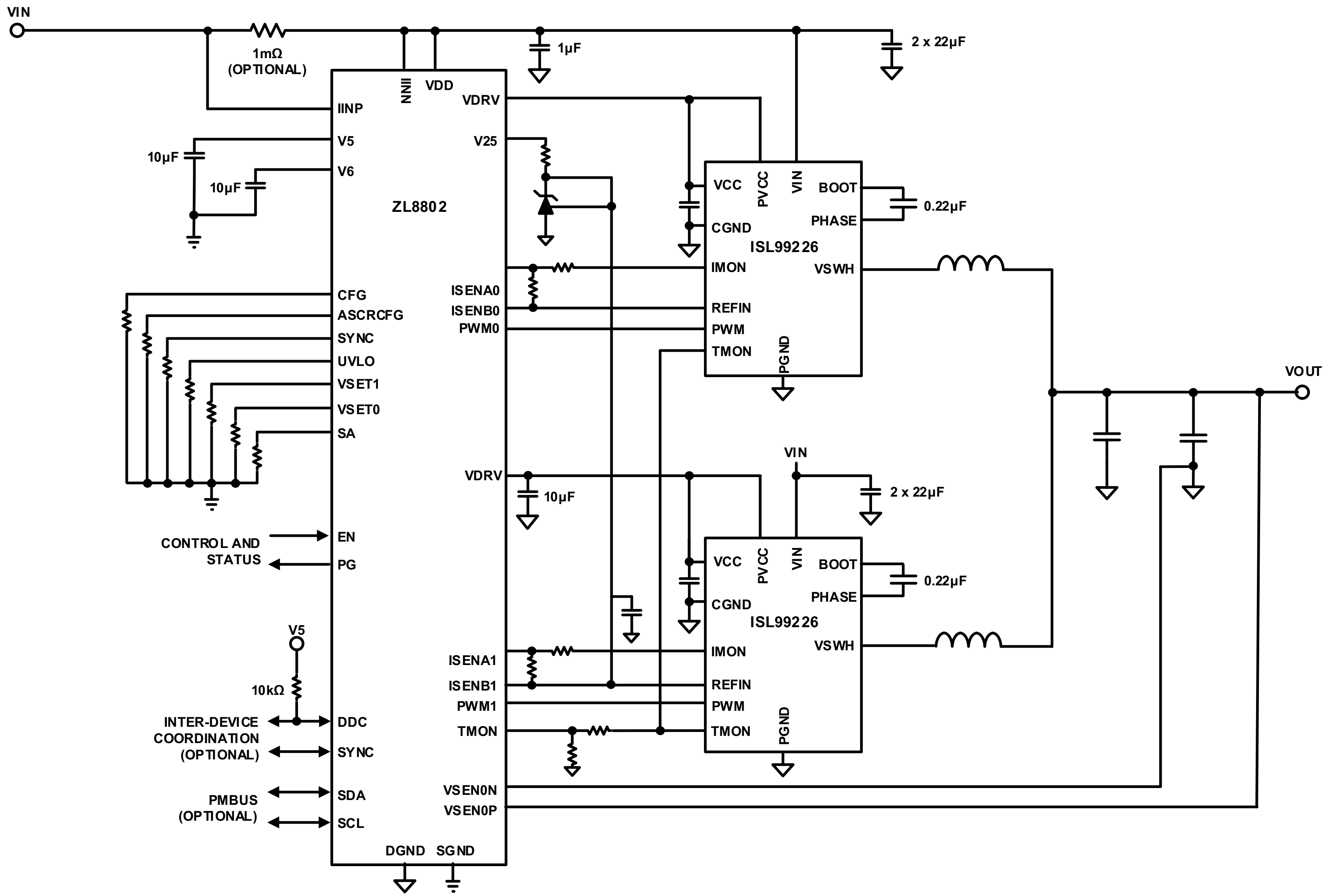


FIGURE 1. TWO-PHASE APPLICATION

Block Diagram

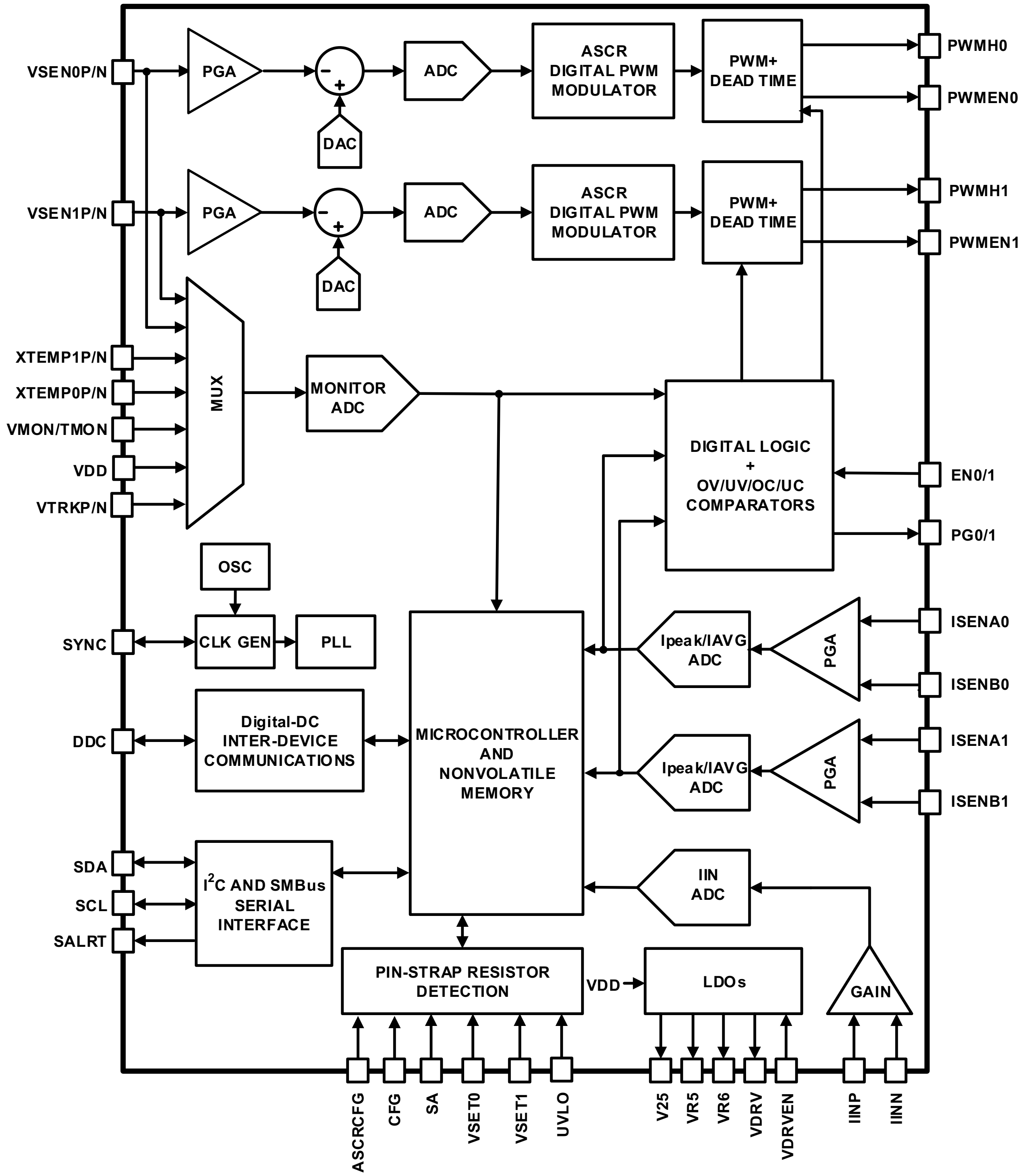
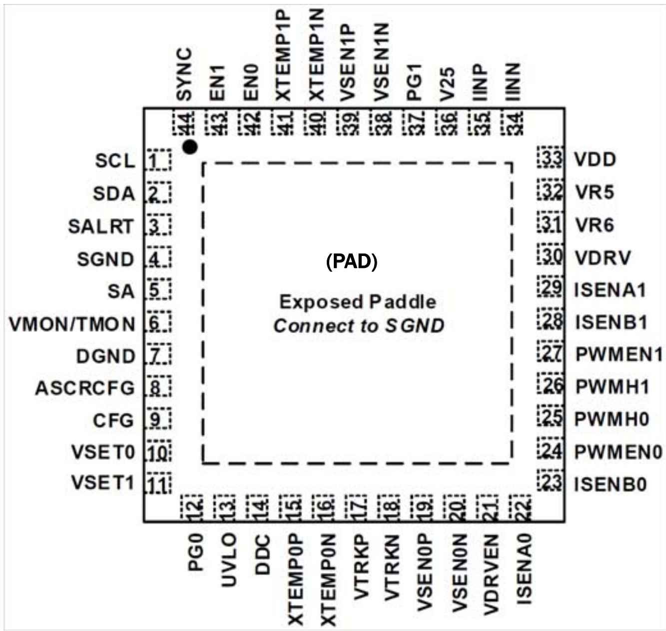


FIGURE 2. BLOCK DIAGRAM

Pin Configuration

ZL8802
(44 LD QFN)
TOP VIEW



Pin Description

PIN #	PIN NAME	TYPE (Note 1)	DESCRIPTION
1	SCL	I/O	Serial clock. Connect to external host and/or to other ZL devices. Requires a pull-up resistor to a 2.5V to 5.5V (recommend VR5, do not use V25) source. Pull-up supply must be from an “always on” source or VR5.
2	SDA	I/O	Serial data. Connect to external host and/or to other ZL devices. Requires a pull-up resistor to a 2.5V to 5.5V (recommend VR5, do not use V25) source. Pull-up supply must be from an “always on” source or VR5.
3	SALRT	O	Serial alert. Connect to external host if desired. Requires a pull-up resistor to a 2.5V to 5.5V (recommend VR5, do not use V25) source. Leave floating if not used.
4	SGND	PWR	Connect to low impedance ground plane. Internal connection to SGND. All pin-strap resistors should be connected to SGND. SGND must be connected to DGND and PGND using a single point connection.
5	SA	M	Serial address select pin. Used to assign unique address for each individual device. See Table 3 for PMBus address options. Connect resistor to SGND.
6	VMON/ TMON	I	Smart power stage temperature monitoring or general purpose voltage monitoring pin. Requires an external 2:1 resistor divider network to correctly read temperature. Requires an external 16:1 resistor divider network to read voltage. Connect bottom of resistor divider network to SGND. Connect VMON/TMON pin to SGND if not used.
7	DGND	PWR	Digital ground. Must connect to SGND and PGND using a single point connection.
8	ASCRCFG	M	Selects ChargeMode control (ASCR) configuration settings. See “Configurable Pins” on page 12 and Table 8 on page 14 for details.
9	CFG	M	Selects current sense, current limit and operating mode. See “Configurable Pins” on page 12 and Table 8 on page 14 for details.
10	VSET0	M	Channel 0 output voltage selection pin. Used to set V_{OUT0} and V_{OUT0} max. See Table 4 on page 12 for V_{OUT} pin-strap options. Default V_{OUT} max is 115% of V_{OUT} setting, but this can be overridden via the PMBus interface with the VOUT_MAX command. Connect resistor to SGND.
11	VSET1	M	Channel 1 output voltage selection pin. Used to set V_{OUT1} and V_{OUT1} max. See Table 4 on page 12 for V_{OUT} pin-strap options. Default V_{OUT} max is 115% of V_{OUT} setting, but this can be overridden via the PMBus interface with the VOUT_MAX command. Connect resistor to SGND. NOT USED IN 2-PHASE MODE. Leave floating in 2-phase mode.
12	PG0	O	Channel 0 power-good output. Can be configured as open drain or push-pull using the PMBus interface. Default setting is open drain.

Pin Description (Continued)

PIN #	PIN NAME	TYPE (Note 1)	DESCRIPTION
13	UVLO	M	Undervoltage lockout selection. Sets the minimum value for V_{DD} voltage to enable V_{OUT}. See Table 6 on page 13 for UVLO setting options. Pin-strapped (configured) values can be overridden by the PMBus interface. Connect resistor to SGND. If enabling the device by tying the EN0 and or EN1 pins high (self-enabling), set the UVLO level to 16V with a 100k resistor so the device will not turn on until after a configuration file has been loaded.
14	DDC	I/O	Single-wire DDC bus (current sharing, interdevice communication). Requires a pull-up resistor to a 2.5V to 5.5V (recommend VR5, no not use V25) source. Pull-up voltage must be present when the device is powered. Pull-up supply must be from an “always on” source or VR5.
15	XTEMP0P	I	External temperature sensor input for Channel 0. Connect to external 2N3904 (base emitter junction) or equivalent embedded thermal diode. If not used connect to SGND.
16	XTEMP0N	I	External temperature sensor input for Channel 0 return. If not used connect to SGND.
17	VTRKP	-	Tracking sense positive input. Used to track an external voltage source. Tracking is only possible in 2-phase operation, or with a single channel in a 2-channel configuration. Tracking is disabled in 4-, 6- and 8-phase operation. If not used connect to SGND.
18	VTRKN	-	Tracking sense negative input (return). If not used connect to SGND.
19	VSEN0P	I	Differential output Channel 0 voltage sense feedback. Connect to positive output regulation point.
20	VSEN0N	I	Differential output Channel 0 voltage sense feedback. Connect to negative output regulation point.
21	VDRVEN	I	VDRV (MOSFET Driver Bias Supply) enable. Leave unconnected (float) or pull up to VR5 to enable, tie to ground to disable.
22	ISENA0	I	Positive differential voltage input for Channel 0 DCR current sensing. Should be routed as a pair with ISENB0. Should connect to resistor located close to output inductor. See “SPS Current Sensing” on page 17.
23	ISENB0	I	Negative differential voltage input for Channel 0 DCR current sensing. Should be routed as a pair with ISENA0. Should be connected to output inductor terminal. See “SPS Current Sensing” on page 17.
24	PWMEN0	O	Used to drive DrMOS enable where applicable. Leave unconnected when not used.
25	PWMH0	O	PWM0 high signal.
26	PWMH1	O	PWM1 high signal.
27	PWMEN1	O	Used to drive DrMOS enable where applicable. Leave unconnected when not used.
28	ISENB1	I	Negative differential voltage input for Channel 1 DCR current sensing. Should be routed as a pair with ISENA1. Should be connected to output inductor terminal. See “SPS Current Sensing” on page 17 for details.
29	ISENA1	I	Positive differential voltage input for Channel 1 DCR current sensing. Should be routed as a pair with ISENB1. Should connect to resistor located close to output inductor. See “SPS Current Sensing” on page 17 for details.
30	VDRV	PWR	MOSFET driver bias supply regulator output. If disabled, this pin can be left floating. Decouple with a high quality 4.7µF X7R or better ceramic capacitor placed close to this pin.
31	VR6	PWR	Bypass for internal 6V reference used to power internal circuitry. Decouple with a high quality 4.7µF X7R or better ceramic capacitor placed close to this pin. Keep this net as small as possible. Do not route near switching signals.
32	VR5	PWR	Bypass for internal 5V reference used to power internal circuitry. Decouple with a high quality 4.7µF X7R or better ceramic capacitor placed close to this pin.
33	VDD	PWR	Supply voltage. Decouple with a high quality 1µF X7R or better ceramic capacitor placed close to this pin.
34	IINN	I	Input current monitor negative input. If not used connect to VDD.
35	IINP	I	Input current monitor positive input. If not used connect to VDD.
36	V25	PWR	Internal 2.5V reference used to power internal circuitry. Decouple with a high quality 4.7µF X7R or better ceramic capacitor placed close to this pin.
37	PG1	O	Channel 1 power-good output. Can be configured as open drain or push-pull using the PMBus interface. Default setting is open drain.
38	VSEN1N	I	Differential output Channel 1 voltage sense feedback. Connect to negative output regulation point. NOT USED IN 2-PHASE MODE. Leave floating in 2-phase mode.
39	VSEN1P	I	Differential output Channel 1 voltage sense feedback. Connect to positive output regulation point. NOT USED IN 2-PHASE MODE. Leave floating in 2-phase mode.
40	XTEMP1N	I	External temperature sensor input for Channel 1 return. If not used connect to SGND.
41	XTEMP1P	I	External temperature sensor input for Channel/Phase 1. Connect to external 2N3904 (base emitter junction) or equivalent embedded thermal diode. If not used connect to SGND.

Pin Description (Continued)

PIN #	PIN NAME	TYPE (Note 1)	DESCRIPTION
42	EN0	I	Enable Channel 0. Active signal enables PWM0 switching. Recommended to be tied low during device configuration. Refer to “Enable Pin Operation and Timing” on page 16 for additional information.
43	EN1	I	Enable Channel 1. Active signal enables PWM1 switching. Recommended to be tied low during device configuration. Refer to “Enable Pin Operation and Timing” on page 16 for additional information. NOT USED IN 2-PHASE MODE. Leave floating in 2-phase mode.
44	SYNC	M/I/O	Clock synchronization input. Used to set the frequency of the internal clock, to sync to an external clock or to output internal clock. When configured as an output this pin is push-pull and does not require a pull-up. See ““Switching Frequency Setting (SYNC)” on page 12 and Table 5 on page 12 for additional information.
PAD	SGND	PWR	Exposed thermal pad. Connect to low impedance ground plane. Internal connection to SGND.

NOTE:

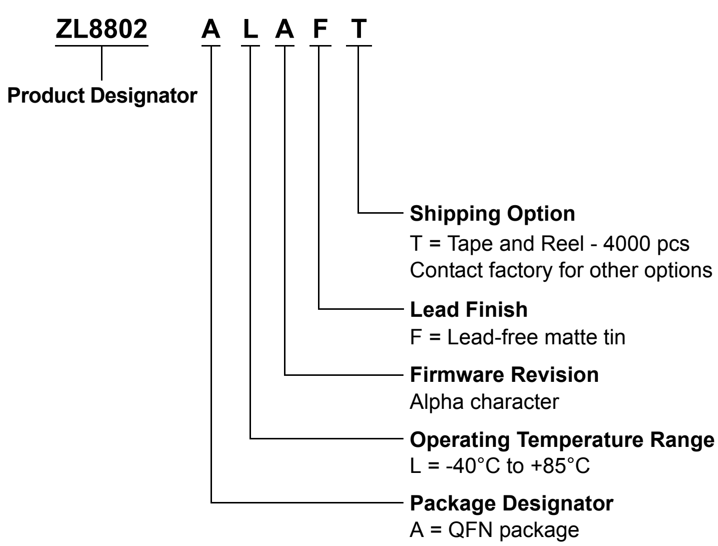
1. I = Input, O = Output, PWR = Power or Ground, M = Multimode pins.

Ordering Information

PART NUMBER (Notes 2, 3, 4)	PART MARKING	TEMP. RANGE (°C)	TAPE AND REEL QUANTITY (Units)	PACKAGE (RoHS Compliant)	PKG. DWG. #
ZL8802ALAFT	8802	-40 to +85	4k	44 Ld QFN	L44.7x7B
ZL8802ALAFT7A	8802	-40 to +85	250	44 Ld QFN	L44.7x7B
ZL8802ALAFTK	8802	-40 to +85	1k	44 Ld QFN	L44.7x7B

NOTES:

2. Please refer to TB347 for details on reel specifications.
3. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pbfree peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
4. For Moisture Sensitivity Level (MSL), please see device information page for ZL8802 For more information on MSL please see techbrief TB363.



Absolute Maximum Ratings

DC Supply Voltage: VDD . . . . -0.3V to 17V
Logic I/O voltage: DDC, EN0, EN1, PG0, PG1, SA, VDRVEN, SALRT, SCL, SDA, SYNC, UVLO, VMON/TMON, VSET0, VSET1, CFG, ASCRCFG . . . . -0.3V to 6.0V
Analog Input Voltages: VSEN0P, VSEN0N, VSEN1P, VSEN1N,
ISENA0, ISENA1, ISENB0, ISENB1 . . . . -0.3V to 6.5V
XTEMP0P, XTEMP1P . . . . -0.3V to 6.0V
XTEMP0N, XTEMP1N . . . . -0.3V to 0.3V
IINN, IINP . . . . -0.3V to 17V
Logic Reference: V25 . . . . -0.3V to 3V
Bias Supplies: VR5, VR6, VDRV . . . . -0.3V to 6.5V
PWM Logic Outputs, PWMH0, PWMH1, PWML0, PWML1 . . . . -0.3V to 6.5V
Ground Voltage Differential (VDGND-VSGND), ... -0.3V to +0.3V
ESD Ratings
Human Body Model (Tested per JESD22-A114E) 3000V
Machine Model (Tested per JESD22-A115-A) 200V
Charged Device Model (Tested per JESD22-C1010-D) 1000V
Latch-Up (Tested per JESD78C; Class 2, Level A) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
44 Ld QFN Package (Notes 6, 7)	25	1.5

Junction Temperature . . . . -55°C to +150°C
Storage Temperature Range . . . . -55°C to +150°C
Pb-Free Reflow Profile . . . . see TB493

Recommended Operating Conditions

Input Supply Voltage Range, VDD . . . . 4.5V to 14V
Output Voltage Range, VOUT . . . . 0.54V to 5.5V
Operating Junction Temperature Range, T_J . . . . -40°C to +125°C
Ambient Temperature Range, T_A . . . . -40°C to +85°C
5V (VR5) Supply Total Supplied Current (Note 8) 5mA
5V LDO Supply (VDRV) (Note 5) . . . . 0 to 80mA

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

5. Output current is limited by device thermal dissipation.
6. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
7. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.
8. Total of current used by pull-ups to SDA, SCL, SALRT, DDC, EN, PG (including push-pull configuration).

Electrical Specifications

V_{DD} = 12V. Typical values are at T_A = +25°C. **Boldface limits apply across the operating ambient temperature range, T_A -40°C to +85°C**

PARAMETER	TEST CONDITIONS	MIN (Note 14)	TYP	MAX (Note 14)	UNIT
IC INPUT AND BIAS SUPPLY CHARACTERISTICS					
IDD Supply Current	f_{SW} = 200kHz	-	26	**50**	mA
	f_{SW} = 1.33MHz	-	50	**80**	mA
IDD Device Disabled Current	EN = 0V, SMBus inactive, VDD = 12V, f_{SW} = 1.33MHz	-	20	**40**	mA
VR5 Reference Output Voltage	VDD > 6V, I < 5mA	**4.5**	5.0	**5.5**	V
V25 Reference Output Voltage	For reference only, VR > 3V	**2.25**	2.5	**2.75**	V
VR6 Reference Output Voltage	For reference only, VDD = 12V	**5.5**	6.1	**6.6**	V
VDRV 5V Output Voltage (Note 9)	V_{DD} > 6.0V; 0 to 80mA	**4.5**	5.25	**5.5**	V
OUTPUT CHARACTERISTICS					
Output Voltage Adjustment Range	$V_{IN} > V_{OUT}$ + 1.1V	**0.54**	-	**5.5**	V
Output Voltage Set-point Accuracy (Note 11)	Across line, load, temperature variation 0.72 < V_{OUT} < 5.50	**-1**	-	**1**	% V_{OUT}
Output Voltage Set-point Resolution (Note 10)	Set using PMBus™ command	-	±0.025	-	% V_{OUT}
Output Voltage Positive Sensing Bias Current	VSEN[0,1] P = 4V (negative = sinking)	**-100**	20	**100**	µA
Output Voltage Negative Sensing Bias Current	VSEN[0,1] N = 0V	-	20	-	µA
LOGIC INPUT/OUTPUT CHARACTERISTICS					
Logic Input Leakage Current	Logic I/O - multimode pins	**-100**	-	**100**	nA
Logic Input Low, V_{IL}		-	-	**0.8**	V
Logic Input High, V_{IH}		**2**	-	-	V
Logic Output Low, V_{OL}	2mA sinking	-	-	**0.5**	V
Logic Output High, V_{OH}	2mA sourcing	**2.25**	-	-	V

Electrical Specifications

V_{DD} = 12V. Typical values are at T_A = +25°C. **Boldface limits apply across the operating ambient temperature range, T_A -40°C to +85°C** **(Continued)**

PARAMETER	TEST CONDITIONS	MIN (Note 14)	TYP	MAX (Note 14)	UNIT
PWM OUTPUT CHARACTERISTICS					
PWM Output Low	2mA sinking	-	-	**0.5**	V
PWM Output High	2mA sourcing	**4.25**	-	-	V
PWM Tri-State Input Bias Current (PWMH0, 1)	V_{PWM} = 2.5V	-	-	**10**	µA
PWM Tri-State transition (always starts from LOW)	10pF maximum load		1		µs
OSCILLATOR AND SWITCHING CHARACTERISTICS					
Switching Frequency Range		**200**	-	**1334**	kHz
Switching Frequency Set-point Accuracy		**-5**	-	**5**	%
Minimum SYNC Pulse Width	50% to 50%	**150**	-	-	ns
Input Clock Frequency Drift Tolerance	Maximum allowed drift of external clock	**-10**	-	**10**	%
PMBus™ Clock Frequency (Note 12)		**100**	-	**400**	kHz
POWER MANAGEMENT					
SOFT START/RAMP CHARACTERISTICS					
Ton-delay/Toff-Delay Range	Set using PMBus™ command	**0**		**5000**	ms
Ton-Delay Accuracy	2-phase Ton-delay > 4ms	-	+/-1	-	ms
Toff-Delay Accuracy	Set to immediate off		-0/+1		ms
Ton-Rise/Toff-Fall Duration Range	Set using PMBus™ command (2-phase or 2-channel only)	**0.0**		**100**	ms
Ton-Rise/Toff-Fall Duration Accuracy	2-phase or 2-channel only	-	±250	-	µs
MONITORING AND FAULT MANAGEMENT					
INPUT VOLTAGE MONITOR AND FAULT DETECTION					
VDD/VIN UVLO Threshold Range		**2.85**	-	**16**	V
VDD/VIN Monitor Accuracy	Full Scale (FS) = 14V	-	±2	-	% FS
VDD/VIN Monitor Resolution	Full Scale (FS) = 14V	-	±0.15	-	% FS
VIN UV Fault Response delay		-	100	-	µs
INPUT CURRENT					
Input Current Sense Differential Input Voltage	V_{IINP}-V_{IINN}	**0**	-	**20**	mV
Input Current Sense Input Offset Voltage	V_{IINP}-V_{IINN}	-	±100	-	µV
Input Current Sense Accuracy	% of full scale (20mV)	-	±5	-	% FS
OUTPUT VOLTAGE MONITOR AND FAULT DETECTION					
VOUT Monitor Accuracy	FS = V_{SET} voltage (VOUT)	**-2**	-	**2**	% FS
VOUT Monitor Resolution	FS = V_{SET} voltage (VOUT)	-	± 0.15	-	% FS
VOUT UV Fault Response Delay		-	10	-	µs
OUTPUT CURRENT					
OUTPUT CURRENT SENSE RESOLUTION					
Low Range	±25mV Full Scale	-	37.5	-	µV
Medium Range	±35mV Full Scale	-	56.25	-	µV
High Range	±50mV Full Scale	-	75.0	-	µV
OUTPUT CURRENT SENSE INPUT BIAS CURRENT					
VOUT Referenced	ISENA0 or ISENA1	**-100**	-	**100**	nA
	ISENB0 or ISENB1	**-25**	-	**25**	µA
OUTPUT CURRENT SENSE MONITOR AND FAULT DETECTION					
Output Current DCR Monitor Temperature Compensation	Configurable via PMBus™	**0**		**12700**	ppm/°C

Electrical Specifications

V_{DD} = 12V. Typical values are at T_A = +25°C. **Boldface limits apply across the operating ambient temperature range, T_A -40°C to +85°C (Continued)**

PARAMETER	TEST CONDITIONS	MIN (Note 14)	TYP	MAX (Note 14)	UNIT
TMON BIAS MONITOR AND FAULT DETECTION					
TMON UVLO Threshold Range	Using TMON pin with 16:1 resistor divider	**2.85**	–	**5**	V
TMON Accuracy (Note 13)	Full Scale (FS) = 1.15V	**-2**	–	**2**	% FS
TMON Resolution	Full Scale (FS) = 1.15V	–	±0.15	–	% FS
TMON UV/OV Fault Response Delay		–	200	–	µs
TEMPERATURE SENSING					
INTERNAL TEMPERATURE SENSOR					
Internal Temperature Accuracy	Tested at +100°C	-5	–	5	°C
Internal Temperature Resolution		–	1	–	°C
Thermal Protection Threshold (Junction temperature)	Factory default	–	125	–	°C
	Configurable via PMBus™	**-40**	–	**125**	°C
EXTERNAL TEMPERATURE SENSOR: XTEMP0 AND XTEMP1					
External Temperature Accuracy	Filter capacitance <100pF	-	±5	-	°C
External Temperature Resolution		–	1	–	°C
Thermal Protection Threshold	Factory default	–	125	–	°C
	Configurable via PMBus™	**-40**	–	**125**	°C

NOTES:

9. Output current is limited by device thermal dissipation.
10. Percentage of Full Scale (FS) with temperature compensation applied.
11. V_{OUT} measured at the termination of the VSENxP and VSENxN sense points.
12. For operation at 400kHz, see PMBus™ Power System Management Protocol Specification Part 1, Section 5.2.6.2 for timing parameter limits.
13. Does not include errors due to resistor divider tolerances.
14. Compliance to data sheet limits is assured by one or more methods: production test, characterization and/or design.

ZL8802 Overview

Digital-DC Architecture Overview

The ZL8802 is an innovative mixed-signal power conversion and power management IC based on Intersil patented Digital-DC technology that provides an integrated, high performance step-down converter for a wide variety of power supply applications.

The ZL8802 DC/DC controller is a dual channel, dual phase controller based on an architecture that does not require loop compensation.

The ZL8802s full digital loop achieves precise control of the entire power conversion process with no software required resulting in a very flexible device that is also very easy to use. The ChargeMode control algorithm is implemented to respond to output current changes within a single PWM switching cycle. This achieves a smaller total output voltage variation with less output capacitance than traditional PWM controllers. An extensive set of power management functions are fully integrated and can be configured using simple pin connections. The user configuration can be saved in an internal Nonvolatile Memory (NVRAM). Additionally, all functions can be configured and monitored via the SMBus hardware interface using standard PMBus™ commands, allowing ultimate flexibility. The ZL8802 is compliant with the PMBus™ Power System Management Protocol Specification Part I and II version 1.2.

Once enabled, the ZL8802 is immediately ready to regulate power and perform power management tasks with no programming required. Advanced configuration options and real-time configuration changes are available via PMBus™ commands if desired and continuous monitoring of multiple operating parameters is possible with minimal interaction from a host controller. Integrated subregulation circuitry enables single supply operation from any supply between 4.5V and 14V with no bias supplies needed.

The ZL8802 can be configured by simply connecting its pins according to the tables provided in the following sections. Additionally, a comprehensive set of online tools and application notes are available to help simplify the design process. An evaluation board is also available to help the user become familiar with the device. This board can be evaluated as a standalone platform using pin configuration settings. PowerNavigator™, a Windows based GUI is also provided to enable full configuration and monitoring capability via the PMBus interface and the included USB cable.

Power Management Overview

The ZL8802 incorporates a wide range of configurable power management features that are simple to implement with no external components. Additionally, the ZL8802 includes circuit protection features that continuously safeguard the device and load from damage due to unexpected system faults. The ZL8802 can continuously monitor input voltage and current, output voltage and current, internal temperature and the temperature of 2 external thermal diodes. A power-good output signal is also included to enable power-on reset functionality for an external processor.

All power management functions can be configured using either pin configuration techniques described in this document or via the SMBus interface using PMBus™ commands. Monitoring parameters can also be preconfigured to provide alerts for specific conditions. The “PMBus™ Command Summary” on page 22 contains a listing of all the PMBus™ commands supported by the ZL8802 and a detailed description of the use of each of these commands.

Pin-Strap Pins

In order to simplify circuit design, the ZL8802 incorporates patented pin-strap pins that allow the user to easily configure many aspects of the device with no programming. Most power management features can be configured using these pins. The pin-strap pins will read the value of the resistor connected to those pins when power is applied to the device and set certain device configuration settings as specified by those resistor values.

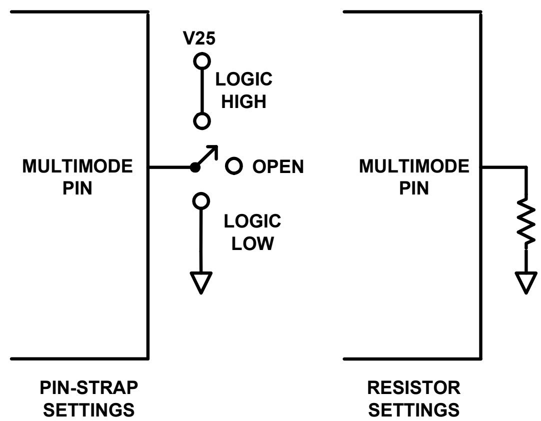


FIGURE 3. PIN-STRAP AND RESISTOR SETTINGS

TABLE 2.

PIN TIED TO	VALUE
LOW (Logic LOW)	<0.8 VDC
OPEN (N/C)	No connection
HIGH (Logic HIGH)	>2.0 VDC
Resistor to SGND	Set by resistor value

Device configuration settings are made when connecting a finite value resistor (in a specified range) between the pin-strap pin and SGND. Standard 1% resistor values are used, and only every fourth E96 resistor value is used so the device can reliably recognize the value of resistance connected to the pin while eliminating the error associated with the resistor accuracy. Up to 31 unique selections are available using a single resistor.

SMBus: Almost any ZL8802 function can be configured via the SMBus interface using standard PMBus™ commands. Additionally, any value that has been configured using the pin-strap setting method can also be reconfigured and/or verified via the SMBus. “PMBus™ Command Detail” on page 27 explains the use of the PMBus™ commands in detail.

Configurable Pins

Numerous operating parameters can be set using the pin-strap resistor setting method: SMBus address (pin 5, SA), output voltage (pins 10 and 11, VSET0, 1), switching frequency (pin 44, SYNC), input voltage undervoltage lockout (pin 13, UVLO). ASCR gain is set by ASCRCFG (pin 8). CFG (pin 9) sets the power stage settings such as over and undercurrent limits.

The SMBus device address is the only parameter that **must** be set by a pin-strap setting pin. All other device parameters can be set via the PMBus™. The device address is set using the SA pin.

SMBus Device Address Selection (SA)

When communicating with multiple SMBus devices using the SMBus interface, each device must have its own unique address so the host can distinguish between the devices. The device address can be set according to the pin-strap options listed in Table 3. When operating in 2-channel mode, care must be taken when using sequential PMBus addresses. Since DDC addresses are automatically set using the PMBus address, it is possible for a device with a PMBus address immediately after a 2-channel ZL8802 to be automatically configured with the same DDC address as one of the ZL8802 channels, which could cause unintended operating modes. For this reason, do not use the next higher PMBus address when using the ZL8802 as a 2-channel device. See PMBus command "DDC_CONFIG (D3h)" on page 65 for details. The SMBus address cannot be changed with a PMBus™ command.

TABLE 3. SMBus DEVICE ADDRESS SELECTION

RSA (kΩ)	SMBus ADDRESS	RSA (kΩ)	SMBus ADDRESS
LOW	40h	42.2	51h
OPEN	42h	46.4	52h
10	41h	51.1	53h
11	43h	56.2	54h
12.1	44h	61.9	55h
13.3	45h	68.1	56h
14.7	46h	75	57h
16.2	47h	82.5	58h
17.8	48h	90.9	59h
19.6	49h	100	5Ah
21.5	4Ah	110	5Bh
23.7	61h	121	5Ch
26.1	4Ch	133	5Dh
28.7	4Dh	147	5Eh
31.6	4Eh	162	5Fh
34.8	4Fh	178	60h
38.3	50h		

Output Voltage and VOUT_MAX Selection (VSET0, 1)

The output voltage may be set to any voltage between 0.54V and 5.5V provided that the input voltage is higher than the desired output voltage by at least 1.1V. Using the pin-strap method, V_{OUT} can be set to any of the voltages shown in Table 4. V_{OUT} can also be set using a PMBus™ command. VOUT_MAX is also determined by this pin-strap setting, and is 15% greater than the VSET0 and VSET1 voltage settings by default, however, VOUT_MAX can be changed via the PMBus.

TABLE 4.

RVSET (kΩ)	VOUT (V)	RVSET (kΩ)	VOUT (V)
LOW	1.00	38.3	1.30
OPEN	1.20	42.2	1.40
HIGH	0.90	46.4	1.50
10	0.60	51.1	1.60
11	0.65	56.2	1.70
12.1	0.70	61.9	1.80
13.3	0.75	68.1	1.90
14.7	0.80	75	2.00
16.2	0.85	82.5	2.10
17.8	0.90	90.9	2.20
19.6	0.95	100	2.30
21.5	1.00	110	2.50
23.7	1.05	121	2.80
26.1	1.10	133	3.00
28.7	1.15	147	3.30
31.6	1.20	162	4.00
34.8	1.25	178	5.00

Switching Frequency Setting (SYNC)

The device's switching frequency is set from 200kHz to 1333kHz using the pin-strap method as shown in Table 5, or by using a PMBus™ command. The ZL8802 generates the device switching frequency by dividing an internal precision 16MHz clock by integers from 11 to 80. 500kHz (n = 32) and 1000kHz (n = 16) are not recommended operating frequencies; use 533kHz and 1067kHz for best performance.

TABLE 5. SWITCHING FREQUENCY SETTINGS

RSYNC (kΩ)	FREQ (kHz)	RSYNC (kΩ)	FREQ (kHz)
LOW	302	23.7	457
OPEN	400	26.1	533
HIGH	485	28.7	571
10	200	31.6	615
11	222	34.8	727
12.1	242	38.3	800

TABLE 5. SWITCHING FREQUENCY SETTINGS (Continued)

RSYNC (kΩ)	FREQ (kHz)	RSYNC (kΩ)	FREQ (kHz)
13.3	267	42.2	842
14.7	286	46.4	889
16.2	320	51.1	1067
17.8	364	56.2	1143
19.6	381	61.9	1231
21.5	432	68.1	1333

The ZL8802 incorporates an internal Phase-Locked Loop (PLL) to clock the internal circuitry. The PLL can be driven by an external clock source connected to the SYNC pin. When using the internal oscillator, the SYNC pin can be configured as a clock source for other Intersil digital power devices.

By default, the SYNC pin is configured as an input. The device will automatically check for a clock signal on the SYNC pin each time EN is asserted. The ZL8802's oscillator will then synchronize with the rising edge of the external clock.

The incoming clock signal must be in the range of 200kHz to 1.33MHz and must be stable when the enable pin (EN0, EN1) is asserted. When using an external clock, the frequencies are not limited to discrete values as when using the internal clock. The external clock signal must not vary more than 10% from its initial value and should have a minimum pulse width of 150ns. In the event of a loss of the external clock signal, the output voltage may show transient overshoot or undershoot.

If loss of synchronization occurs, the ZL8802 will automatically switch to its internal oscillator and switch at its programmed frequency.

When used in a multiphase (4-, 6- and 8-phase) application, the SYNC pin of one of the devices must be configured as an output. The device will run from its internal oscillator and will drive the SYNC pin so other devices can be synchronized to it. The SYNC pin will not be checked for an incoming clock signal while in this mode.

The switching frequency can be set to any value between 200kHz and 1.33MHz using a PMBus™ command. The available frequencies below 1.33MHz are defined by f_{SW} = 16MHz/N, where 12 ≤ N ≤ 80.

If a value other than f_{SW} = 16MHz/N is entered using a PMBus™ command, the internal circuitry will select the switching frequency value using N as a whole number to achieve a value close to the entered value. For example, if 810kHz is entered, the device will select 800kHz (N = 20).

Input Voltage Undervoltage Lockout Setting (UVLO)

The input Undervoltage Lockout (UVLO) prevents the ZL8802 from operating when the input falls below a preset threshold, indicating the input supply is out of its specified range. The input voltage undervoltage lockout threshold can be set between 4.18V and 16V using the pin-strap method as shown in Table 6. UVLO can also be set or changed using the VIN_UV_FAULT_LIMIT command.

TABLE 6. INPUT VOLTAGE UNDERVOLTAGE LOCKOUT SETTING

RUVLO (kΩ)	UVLO (V)	RUVLO (kΩ)	UVLO (V)
LOW	5.50	46.4	7.42
OPEN	4.50	51.1	8.18
HIGH	10.80	56.2	8.99
26.1	4.18	61.9	9.90
28.7	4.59	68.1	10.90
31.6	5.06	75	12.00
34.8	5.57	82.5	13.20
38.3	6.13	90.9	14.54
42.2	6.75	100	16.00

Once an input undervoltage fault condition occurs, the user may determine the desired response to the fault condition. The following input undervoltage protection response options are available:

1. Shut down and stay off until the fault has cleared and the device has been disabled and reenabled.
2. Shut down and restart continuously after a delay.

Refer to "PMBus™ Command Detail" on page 27 for details on how to select specific overvoltage fault response options using the VIN_UV_FAULT_RESPONSE command.

When controlling the ZL8802 exclusively through the PMBus™, a high voltage setting for UVLO can be used to prevent the ZL8802 from being enabled until a lower voltage for UVLO is set using the VIN_UV_FAULT_LIMIT command.

Configuration Setting (CFG)

The Configuration pin (CFG) sets several device configuration settings allowing the device to be used in applications without the need for loading configuration files. The settings are shown in Table 7. **When using the ZL8802 in a 4-phase application, the master device address must be 1 higher than the slave address.** This must be done in order for the 2 devices to be recognized as part of a current sharing group. See PMBus command "DDC_CONFIG (D3h)" on page 65 for details.

TABLE 7. CONFIGURATION SETTINGS

	Page 0		Page 1		
RCFG (kΩ)	AVERAGE OC LIMIT (A)	PEAK OC LIMIT (A)	AVERAGE OC LIMIT (A)	PEAK OC LIMIT (A)	CIRCUIT
10	25	28	25	28	2 Output
11	35	37.5	35	37.5	2 Output
12.1	45	48	45	48	2 Output
13.3	55	60	55	60	2 Output
14.7	60	65	60	65	2 Output
16.2	65	70	65	70	2 Output
17.8	35	37.5	25	28	2 Output
19.6	45	48	25	28	2 Output
21.5	55	60	25	28	2 Output
23.7	45	48	35	37.5	2 Output

TABLE 7. (Continued)CONFIGURATION SETTINGS

RCFG (kΩ)	Page 0		Page 1		CIRCUIT
	AVERAGE OC LIMIT (A)	PEAK OC LIMIT (A)	AVERAGE OC LIMIT (A)	PEAK OC LIMIT (A)	
26.1	55	60	35	37.5	2 Output
28.7	55	60	45	48	2 Output
31.6	25	28	35	37.5	2 Output
34.8	25	28	45	48	2 Output
38.3	25	28	55	60	2 Output
42.2	35	37.5	45	48	2 Output
46.4	35	37.5	55	60	2 Output
51.1	45	48	55	60	2 Output
56.2	25	28	25	28	2-Phase
61.9	35	37.5	35	37.5	2-Phase
68.1	45	48	45	48	2-Phase
75	55	60	55	60	2-Phase
82.5	65	70	65	70	2-Phase
90.9	35	37.5	35	37.5	4-PH Master
100	35	37.5	35	37.5	4-PH Slave
110	45	48	45	48	4-PH Master
121	45	48	45	48	4-PH Slave
133	55	60	55	60	4-PH Master
147	55	60	55	60	4-PH Slave
162	65	70	65	70	4-PH Master
178	65	70	65	70	4-PH Slave
LOW	20	22.5	20	22.5	2-Phase
OPEN	20	22.5	20	22.5	2 Output
HIGH	35	37.5	35	37.5	2 Output

ChargeMode Control (ASCR) Setting (ASCRCFG)

The device's ChargeMode response can be optimized by adjusting the ASCR gain and residual settings, either by using the ASCRCFG pin-strap resistor method as shown in Table 8, or by using the ASCR_CONFIG PMBus™ command. When using Table 8, the ASCR Residual is fixed at 90.

TABLE 8. ChargeMode CONTROL (ASCR) SETTINGS

ASCRCFG kΩ)	GAIN P0	GAIN P1	ASCRCFG (kΩ)	GAIN P0	GAIN P1
10	200	200	51.1	800	600
11	200	400	56.2	800	800
12.1	200	600	61.9	800	1000
13.3	200	800	68.1	1000	200
14.7	200	1000	75	1000	400

TABLE 8. ChargeMode CONTROL (ASCR) SETTINGS (Continued)

ASCRCFG kΩ)	GAIN P0	GAIN P1	ASCRCFG (kΩ)	GAIN P0	GAIN P1
16.2	400	200	82.5	1000	600
17.8	400	400	90.9	1000	800
19.6	400	600	100	1000	1000
21.5	400	800	110	100	100
23.7	400	1000	121	300	300
26.1	600	200	133	500	500
28.7	600	400	147	700	700
31.6	600	600	162	900	900
34.8	600	800	178	1100	1100
38.3	600	1000	LOW	300	300
42.2	800	200	OPEN	500	500
46.4	800	400	HIGH	700	700

Start-Up and Shutdown Settings

The device's start-up and shutdown settings can be set by using the following PMBus Commands:

TON_DELAY: Sets the time from a low to high EN0 or EN1 transition, or the receipt of an OPERATION command via the PMBus, to the start of an output voltage ramp.

TON_RISE: Sets the time from the end of the TON_DELAY to the output voltage reaching regulation.

TOFF_DELAY: Sets the time from a high to low EN0 or EN1 transition, or the receipt of an OPERATION command via the PMBus, to the start of an output voltage ramp down.

TOFF_FALL: Sets the time from the end of the TOFF_DELAY to the output voltage reaching 0V.

Note that in the case of 2-channel operation, these settings will apply to both channels. Each channel can be configured to have different settings by using the TON_DELAY, TON_RISE, TOFF_DELAY and TOFF_FALL PMBus commands.

Internal Bias Regulators and Input Supply Connections

The ZL8802 employs internal Low Dropout (LDO) regulators to supply bias voltages for internal circuitry, allowing it to operate from a single input supply. The internal bias regulators are as follows:

VR6: The VR6 LDO provides a regulated 6.1V bias supply for internal circuitry. It is powered from the VDD pin. A 4.7µF ceramic X7R filter capacitor to SGND is required at the VR6 pin. Keep this net as small as possible and avoid routing this trace near any switching signals.

VR5: The VR5 LDO provides a regulated 5.1V bias supply for internal circuitry. It is powered from the VDD pin. A 4.7µF ceramic X7R filter capacitor to SGND is required at the VR5 pin. This supply may be used for to provide a pull-up supply as long as load current does not exceed 5mA.

V25: The V25 LDO provides a regulated 2.5V bias supply for the main controller circuitry. It is powered from an internal 5V node. A 4.7µF ceramic X7R filter capacitor to SGND is required at the V25 pin. This voltage should only be used to set pin-strap pins to the HIGH state.

VDRV: The VDRV LDO provides a regulated 5.25V bias supply for external MOSFET driver ICs or DrMOS integrated drivers/FETs. A 4.7µF ceramic X7R filter capacitor to PGND is required, however, additional capacitance will be needed as specified by the MOSFET driver or DrMOS device selected. The maximum rated output current is 80mA, but device thermal limits must be considered. The power dissipated by the VDRV supply will be (VIN-5.25V) X IDRV, where IDRV is the current supplied by the VDRV bias supply. VDRV is enabled by leaving the VDRVEN unconnected (floating) or connecting it to VR5, and is disabled by connecting VDRVEN to ground.

NOTE: The internal bias regulators, VR6, VR5 and V25, are not designed to be outputs for powering other circuitry. The multimode pins may be connected to the V25 pin for logic HIGH settings, and the VR5 supply can be used to provide up to 5mA of pull-up current for the SDA, SCL, SALRT, DDC and PG pins.

Operation with 5V VDD: When operating the ZL8802 at voltages below 5.5V, the VR6 and VR5 supplies should be connected directly to VDD for best performance. The VDRV supply should not be used; the 5V VDD supply should be used instead for powering DrMOS and MOSFET driver ICs.

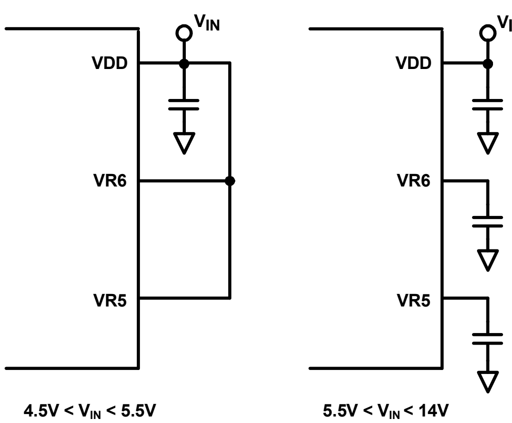


FIGURE 4. VR SUPPLY CONNECTIONS

Start-Up Procedure

The ZL8802 follows a specific internal start-up procedure after power is applied to the VDD pin, as shown in Figure 5.

The device requires approximately 60ms to check for specific values stored in its internal memory. If the user has stored values in memory, those values will be loaded.

Once this process is completed, the device is ready to accept commands via the serial interface and the device is ready to be enabled. If the device is to be synchronized to an external clock source, the clock frequency must be stable prior to asserting the EN pin. Once enabled, the device requires approximately 2ms before its output voltage may be allowed to start its ramp-up process.

After the Ton-delay period has expired, the output will begin to ramp towards its target voltage according to the preconfigured Ton-rise time.

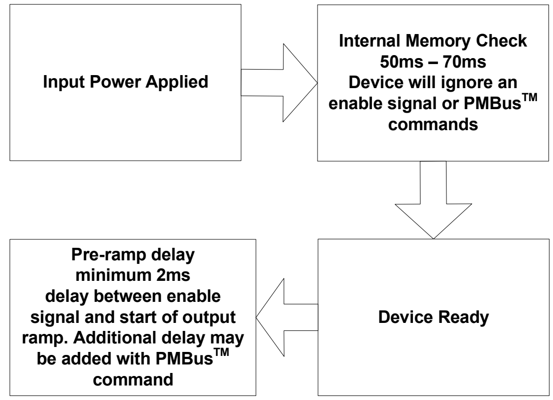


FIGURE 5. ZL8802 INTERNAL START-UP PROCEDURE

V_{IN} should be above the ZL8802's UVLO limit (VIN_UV_FAULT_LIMIT) before the Enable pin is driven high. Following this sequence will result in the most consistent turn-on delays. **If a configuration file is needed to ensure proper circuit operation**, when V_{IN} is first applied to the ZL8802, for example, during initial PCB turn-on and test, the Enable pin must be held low by some means until the ZL8802 configuration file can be loaded. If the Enable pin is not held low, then the ZL8802 may attempt to turn on with incorrect configuration settings, possibly causing circuit failure.

In those cases where a configuration file is needed to ensure proper circuit operation and the Enable pin cannot be held low during the initial application of power, two options are available:

1. Limit V_{IN} to 3.0V during initial testing. The ZL8802 configuration file can be loaded when V_{IN} is as low as 3.0V. Once the configuration file is loaded V_{IN} can be increased to the normal input voltage range.
2. Use a 100kΩ pin-strap resistor to set UVLO to 16V. This will keep the ZL8802 disabled while the configuration file is loaded. Ensure that the VIN_UV_FAULT_LIMIT command is the last command in the configuration file.

Ton-Delay and Rise Times

Ton- and Toff-delay and Ramp times are initially set to 5ms. In some applications, it may be necessary to set a delay from when an enable signal is received until the output voltage starts to ramp to its target value. In addition, the designer may wish to precisely set the time required for V_{OUT} to ramp to its target value after the delay period has expired. These features may be used as part of an overall inrush current management strategy or to precisely control how fast a load IC is turned on. The ZL8802 gives the system designer several options for precisely and independently controlling both the delay and ramp time periods.

The Ton-delay time begins when the EN pin is asserted. The Ton-delay time is set using the PMBus™ command TON_DELAY.

The Ton-rise time enables a precisely controlled ramp to the nominal V_{OUT} value that begins once the Ton-delay time has expired. The ramp-up is monotonic and its slope may be precisely set using the PMBus™ command TON_RISE.

The Ton-delay and Ton-ramp times can be set using PMBus™ commands TON_DELAY and TON_RISE over the serial bus interface. When the Ton-delay time is set to 0ms, the device will begin its ramp after the internal circuitry has initialized

The Ton-delay and Ton-ramp times can be set using PMBus™ commands TON_DELAY and TON_RISE over the serial bus interface. When the Ton-delay time is set to 0ms, the device will begin its ramp after the internal circuitry has initialized which takes approximately 2ms to complete. The Ton-rise time may be set to values less than 2ms, however the Ton-rise time should be set to a value greater than 500µs to prevent inadvertent fault conditions due to excessive inrush current. A lower Ton-rise time limit can be estimated using the formula: Ton-rise = C_{OUT}*V_{OUT}/I_{LIMIT} where C_{OUT} is the total output capacitance, V_{OUT} is the output voltage and I_{LIMIT} is the current limit setting for the ZL8802.

When interdevice current sharing is used (4 phases), the output voltage rise time will vary by application. The rise time in this case can be adjusted using the PMBus command MULTI_PHASE_RAMP_GAIN. Higher gain values produce faster turn-on ramps. Typical MULTI_PHASE_RAMP_GAIN values range between 1 and 10; the default value is 3. The slew rate of the output voltage during ramp-up is directly proportional to this gain, as well as the input voltage (V_{IN}) and the device switching frequency (FREQUENCY_SWITCH). The slew rate of the output voltage during turn-on can be calculated with the following formula:

Slew Rate (mV/ms) = 14*(VIN)*(MULTI_PHASE_RAMP_GAIN) * (FREQUENCY_SWITCH in MHz)

The resulting total rise time can then be calculated:

Rise Time = Output Voltage/Slew Rate

Enable Pin Operation and Timing

The enable pins (EN0 and EN1) are used to enable and disable each channel of the ZL8802. When operated as a 2-phase converter, use EN0 and ground EN1. The enable pins should be held low whenever a configuration file or script is used to configure the ZL8802, or a PMBus™ command is sent that could potentially damage the application circuit. When the ZL8802 is used in a self-enabled mode, for example, when EN0 or EN1 is tied to VR5, or to a resistor divider to VIN, the user must consider the ZL8802's default factory settings. When a configuration file is used to configure the ZL8802, the factory default settings are restored to both the user and default stores in order to set the ZL8802 to an initialized state. Since the default state of the ZL8802 is to be enabled when the enable pin is high, it is possible for the ZL8802 to be enabled while the PMBus™ commands are sent to the ZL8802 during the configuration process.

The Enable pin is edge triggered to achieve fast turn-off times. As a result, minimum Enable high and Enable low pulse widths must be observed to ensure correct operation. The minimum high and low pulse widths are dependent on the configured rise, fall and delay times and can be calculated using Equations 1 and 2:

$$\text{EN low} > \text{TOFF\_DELAY} + \text{TOFF\_FALL} + 10.5\text{ms} \quad \text{(EQ. 1)}$$

$$\text{EN high} > \text{TON\_DELAY} + \text{TON\_RISE} + \text{POWER\_GOOD\_DELAY} + 5.5\text{ms} \quad \text{(EQ. 2)}$$

EN low and EN high times shorter than these minimums may result in the device not responding to the trailing edge of the pulse. For example, a EN low pulse below the EN low minimum pulse width may stay in the OFF state until a valid EN low pulse is applied to the EN pin.

Power-Good

The ZL8802 provides a power-good (PG0, PG1) signal for each channel that indicates the output voltage is within a specified tolerance of its target level and no fault condition exists. By default, the PG pin will assert if the output is within 10% of the target voltage. These limits and the polarity of the pin may be changed using PMBus™ commands.

A PG delay period is defined as the time from when all conditions within the ZL8802 for asserting PG are met to when the PG pin is actually asserted. This feature is commonly used instead of using an external reset controller to control external digital logic. By default, the ZL8802 PG delay is set equal to 1ms. The PG delay may be set using a PMBus™ command as described in “POWER_GOOD_DELAY (D4h)” on page 66.

Power Management Functional Description

Output Overvoltage Protection

The ZL8802 offers an internal output overvoltage protection circuit that can be used to protect sensitive load circuitry from being subjected to a voltage higher than its prescribed limits. A hardware comparator is used to compare the actual output voltage (seen at the VSEN pin) to a programmable threshold set to 10% higher than the target output voltage (the default setting). If the VSEN voltage exceeds this threshold, the PG pin will deassert and the device can then respond in the following ways:

1. Shut down and stay off until the fault has cleared and the device has been disabled and reenabled.
2. Shut down, and when the fault is no longer present, attempt to restart.

Refer to “VOUT_OV_FAULT_RESPONSE (41h)” on page 37 for details on how to select specific overvoltage fault response options using the VOUT_OV_FAULT_RESPONSE command.

Output Prebias Protection

The ZL8802 provides prebiased start-up operation in 2-channel and single device 2-phase operation. Prebias protection is not provided when operating in current sharing 4-, 6- or 8-phase configurations. An output prebias condition exists when an externally applied voltage is present on a power supply's output before the power supply's control IC is enabled. Certain applications require that the converter not be allowed to sink current during start up if a prebias condition exists at the output. The ZL8802 provides prebias protection by sampling the output voltage prior to initiating an output ramp.

If a prebias voltage lower than the desired output voltage is present after the Ton-delay time the ZL8802 starts switching with a duty cycle that matches the prebias voltage. This ensures that the ramp-up from the prebias voltage is monotonic. The output voltage is then ramped to the desired output voltage at the ramp rate set by the TON_RISE command.

The resulting output voltage rise time will vary depending on the prebias voltage, but the total time elapsed from the end of the Ton-delay time to when the Ton-rise time is complete and the output is at the desired value will match the preconfigured ramp time (see Figure 6).

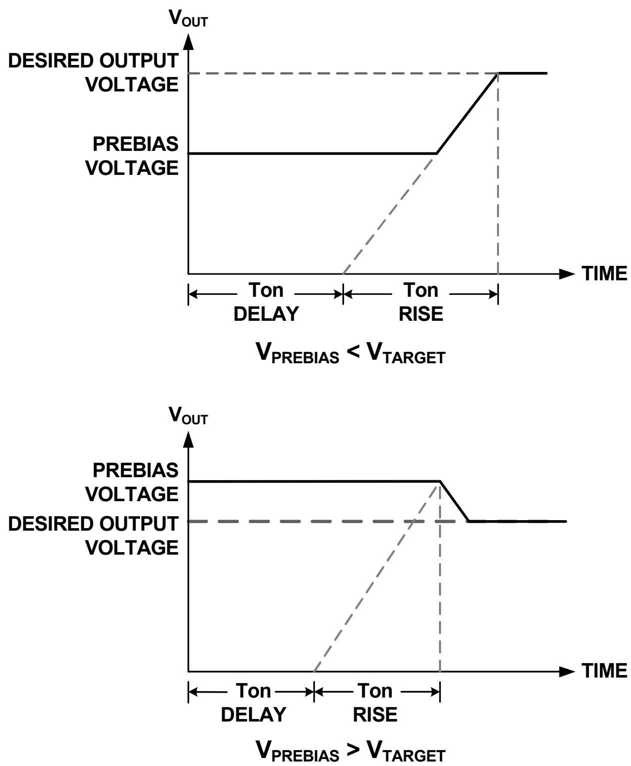


FIGURE 6. OUTPUT RESPONSES TO PREBIAS VOLTAGES

If a prebias voltage higher than the target voltage exists after the preconfigured Ton-delay time and Ton-rise time have completed, the ZL8802 starts switching with a duty cycle that matches the prebias voltage. This ensures that the ramp-down from the prebias voltage is monotonic. The output voltage is then ramped down to the desired output voltage

If a prebias voltage higher than the overvoltage limit exists, the device will not initiate a turn-on sequence and will stay off.

Output Overcurrent Protection

The ZL8802 can protect the power supply from damage from an overloaded or shorted output. Once the current limit threshold has been selected (see "Current Limit Configuration" on page 18), the user may determine the desired response to the fault condition. The following overcurrent protection response options are available:

1. Shut down and stay off until the device has been disabled and reenabled.
2. Shut down and restart continuously after a delay.

Refer to the "PMBus™ Command Detail" on page 27 for details on how to select specific overvoltage fault response options using the IOUT_OC_FAULT_RESPONSE command.

SPS CURRENT SENSING

By default, the ZL8802 senses current by utilizing the IMON output from the ISL9922X Smart Power Stage (SPS). A 6:1 resistor divider is needed between the SPS IMON output and the ISENA and ISENB inputs of the ZL8802, as shown in Figure 7.

Using an ISL9922x device will provide the best current sense accuracy with no action needed from the user.

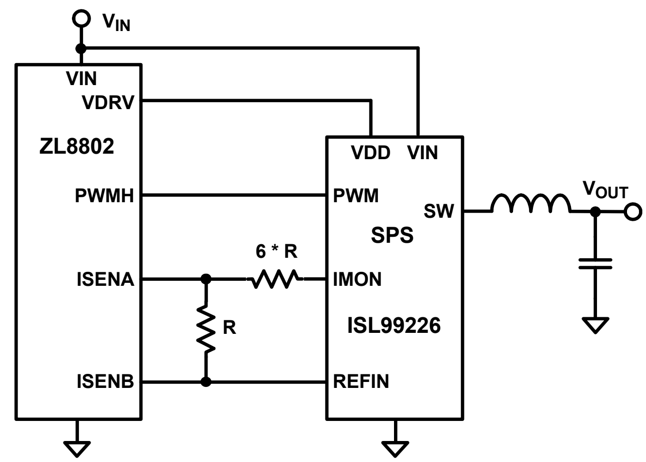


FIGURE 7. SPS CURRENT SENSING

DRMOS CURRENT SENSING

If a DrMOS device must be used, the ZL8802 can also use the inductor DCR current sensing technique. Current sensing is achieved with an R/C network as shown in Figure 8.

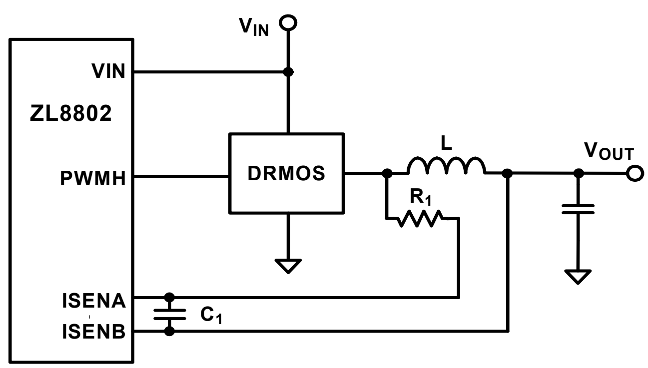


FIGURE 8. DCR CURRENT SENSING

For the voltage across C_1 to reflect the voltage across the DCR of the inductor, the time constant of the inductor must match the time constant of the RC network.

$$\tau_{RC} = \tau_{L/DCR}$$

$$R1 \cdot C1 = \frac{L}{DCR}$$

This capacitor, shown as C_1 in Figure 8, should be an X7R or better dielectric, and C_1 should be placed as close to the ZL8802 as possible for the best noise performance. The L and DCR values should be set using the INDUCTOR and IOUT(0/1)_CAL_GAIN commands. For *L*, use the average of the nominal value and the minimum value. Include the effects of tolerance, DC bias and switching frequency on the inductance when determining the minimum value of *L*. Use the typical room temperature value for *DCR*.

Current Limit Configuration

The ZL8802 gives the power supply designer several choices for the fault response during over or undercurrent condition. The user can select the number of violations allowed before declaring fault, a blanking time and the action taken when a fault is detected. These parameters can be configured using the ISENSE_CONFIG command.

The blanking time represents the time when no current measurement is taken. This is to avoid taking a reading just after a current load step (less accurate due to potential ringing). It is a configurable parameter from 0 to 832ns.

ZL8802 provides an adjustable maximum full scale sensing range. Three ranges are available: ±25mV, ±35mV and ±50mV maximum input voltage.

By default, current sensing is enabled during the inductor current down-slope period of the switching period (D’). In applications where the steady state duty cycle is >0.5, for example, a 5V to 3.3V converter, the ZL8802 can be configured to sense current during the inductor up-slope period of the switching cycle (D).

The user has the option of selecting how many consecutive overcurrent readings must occur before an overcurrent fault and subsequent shutdown are initiated. Either 1, 3, 5, 7, 9, 11 or 13 consecutive faults can be selected.

The current limit thresholds are set with 4 commands:

1. IOUT_OC_FAULT_LIMIT – This sets the overcurrent threshold that must be exceeded by the number of consecutive times chosen in ISENSE_CONFIG.
2. IOUT_UC_FAULT_LIMIT – This is the same as IOUT_OC_FAULT_LIMIT, but represents the negative current that flows lower FET during the D’ interval. Large negative currents can flow during faults such as a higher voltage rail being shorted to a lower voltage rail.
3. IOUT_AVG_OC_FAULT_LIMIT – This limit is similar to IOUT_OC_FAULT_LIMIT, but the limit represents an average reading over several switching cycles. Since it is an average, the response time is slower, but the limit can be set closer to the maximum average expected output current.
4. IOUT_AVG_UC_FAULT_LIMIT – This limit is similar to IOUT_AVG_OC_FAULT_LIMIT, but represents the negative current that flows lower FET during the D’ interval.

Input Current Monitor

The input current can be monitored through the IINN and IINP pins. The input current monitor input should be connected across a current sensing resistor in series with the input supply. The IINP pin is connected to the input supply side of the current sense resistor and the IINN pin is connected to the ZL8802 VDD side of the current sense resistor. Using the IIN_SCALE command, set the current sense resistor value. Select the current sense resistor value such that the maximum expected input current times the current sense resistor value does not exceed the maximum current sensing input voltage of 20mV.

If this feature is not used, IINN and IINP should be tied to VDD.

Thermal Overload Protection

The ZL8802 includes an on-chip thermal sensor that continuously measures the internal temperature of the die. This thermal sensor is used to provide both over-temperature and under-temperature protection. If the over-temperature limit is exceeded, or the temperature falls below the under-temperature limit, the ZL8802 is shut down. The over-temperature and under-temperature limits are set by the OT_FAULT_LIMIT and UT_FAULT_LIMIT respectively. The ZL8802 will not attempt to restart until the temperature has fallen below the OT_WARN_LIMIT for over-temperature faults or has risen above the UT_WARN_LIMIT for under-temperature faults. The default temperature limits are +125°C and -45°C, but the user may set the limits to different values if desired. Note that setting a higher over-temperature or under-temperature limit may result in permanent damage to the device. Once the device has been disabled due to an internal temperature fault, the user may select one of several fault response options as follows:

1. Shut down and stay off until the fault has cleared and the device has been disabled and reenabled.
2. Shut down and restart continuously after a delay.

Refer to “PMBus™ Command Detail” on page 27 for details on how to select specific overvoltage fault response options using the OT_FAULT_RESPONSE and UT_FAULT_ RESPONSE commands.

Voltage Tracking

Numerous high performance systems place stringent demands on the order in which the power supply voltages are turned on. This is particularly true when powering FPGAs, ASICs and other advanced processor devices that require multiple supply voltages to power a single die. In most cases, the I/O interface operates at a higher voltage than the core and therefore the core supply voltage must not exceed the I/O supply voltage according to the manufacturers' specifications.

The ZL8802 integrates a tracking scheme that allows one of its outputs (Channel 0 or Channel 1), or the single output in a dual phase application, to track a voltage that is applied to the VTRK pin with no external components required. The VTRK pin is an analog input that, when tracking mode is enabled, configures the voltage applied to the VTRK pin to act as a reference for the device’s output regulation.

Coincident. This mode configures the ZL8802 to ramp its output voltage at the same rate as the voltage applied to the VTRK pin until it reaches its desired output voltage. The device that is tracking another output voltage (slave) must be set to its desired steady state output voltage, i.e., VOUT_COMMAND is set to the final output voltage.

Ratiometric. This mode configures the ZL8802 to ramp its output voltage at a rate that is a percentage of the voltage applied to the VTRK pin. The default setting is 50%, but an external resistor string may be used to configure a different tracking ratio. The device that is tracking another output voltage (slave) must be set to its desired steady-state output voltage, i.e., VOUT_COMMAND is set to the final output voltage.

The master ZL8802 device in a tracking group is defined as the device that has the highest target output voltage within the group. This master device will control the ramp rate of all tracking devices and is not configured for tracking mode. The maximum tracking rise time is 1V/ms. The slave device must be enabled before the master.

Any device that is configured for tracking mode will ignore its Ton-delay and Ton-rise settings and its output will take on the turn-on/turn-off characteristics of the reference voltage present at the VTRK pin.

Tracking mode can be configured by using the TRACK_CONFIG command.

Note that current sharing groups that are also configured to track another voltage do not offer prebias protection; a minimum load should therefore be enforced to avoid the output voltage from being held up by an outside force.

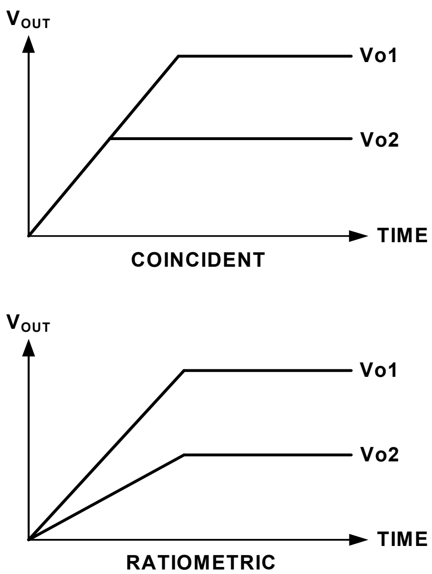


FIGURE 9. TRACKING MODES

External Voltage Monitoring

The voltage monitoring (TMON) pin is available to monitor the voltage supply for the external driver IC. The TMON input must be scaled by a 16:1 ratio in order to read-back the TMON voltage correctly. A 100kΩ and 6.65kΩ resistor divider is recommended. Overvoltage and undervoltage fault thresholds can be set using MFR_TMON_OV_FAULT_LIMIT and MFR_ TMON_UV_FAULT_LIMIT commands. The response to these limits are set using the TMON_OV_FAULT_RESPONSE and TMON_ UV_FAULT_RESPONSE commands. To ignore the TMON input, set the TMON_OV and _UV_FAULT_RESPONSEs to 00h.

Once the device has been disabled due to TMON fault, the user may select one of several fault response options as follows:

1. Shut down and stay off until the fault has cleared and the device has been disabled and reenabled.
2. Shut down and restart continuously after a delay.

SMBus Communications

The ZL8802 provides a SMBus digital interface. The ZL8802 can be used with any standard 2-wire SMBus host device. In addition, the device is compatible with SMBus version 2.0 and includes an SALRT line to help mitigate bandwidth limitations related to continuous fault monitoring. Pull-up resistors are required on the SMBus. The pull-up resistor may be tied to VR5 or to an external 3.3V or 5V supply as long as this voltage is present prior to or during device power-up. The ideal design will use a central pull-up resistor that is well-matched to the total load capacitance. The minimum pull-up resistance should be limited to a value that enables any device to assert the bus to a voltage that will ensure a logic 0 (typically 0.8V at the device monitoring point) given the pull-up voltage (5V if tied to VR5) and the pull-down current capability of the ZL8802 (nominally 4mA). A pull-up resistor of 10kΩ is a good value for most applications.

SMBus data and clock lines should be routed with a closely coupled return or ground plane to minimize coupled interference (noise). Excessive noise on the data and clock lines that cause the voltage on these lines to cross the high and low logic thresholds of 2.0V and 0.8V respectively will cause command transmissions to be interrupted and result in slow bus operation or missed commands. For less than 10 devices on an SMBus a 10kΩ resistor on each line provides good performance.

The ZL8802 accepts most standard PMBus™ commands. When enabling the device with ON_OFF_CONFIG command, it is recommended that the enable pin is tied to SGND.

In addition to bus noise considerations, it is important to ensure that user connections to the SMBus are compliant to the PMBus™ command standards. Any device that can malfunction in a way that permanently shorts SMBus lines will disable PMBus™ communications. Incomplete PMBus™ commands can also cause the ZL8802 to halt PMBus™ communications. This can be corrected by disabling, then reenabling the device.

Digital-DC Bus

The Digital-DC Communications (DDC) bus is used to communicate between Intersil Digital-DC devices, and within the ZL8802 itself. This dedicated bus provides the communication channel between devices for features such as sequencing, fault spreading and current sharing. **The DDC pin must be pulled-up to an external 2.5V to 5.0V supply, (or configured as a push-pull output using the USER_GLOBAL_CONFIG command) even if the ZL8802 is operating stand-alone**. In addition, the DDC pin must be pulled up or configured as a push-pull output before the Enable pin is set high. Push-pull mode can only be used when the ZL8802 is operating stand-alone. The DDC pin on all Digital-DC devices that utilize sequencing, fault spreading or current sharing must be connected together. The DDC pin on all Digital-DC devices in an application should be connected together. A pull-up resistor is required on the DDC bus in order to guarantee the rise time as follows:

$$\text{Riset time} = R_{PU} \bullet C_{LOAD} \leq 1\mu s \qquad \textbf{(EQ. 3)}$$

Where R_{PU} is the DDC bus pull-up resistance and C_{LOAD} is the bus loading. The pull-up resistor may be tied to VR5 or to an external 3.3V or 5V supply as long as this voltage is present prior to or during device power-up. As a rule of thumb, each device connected to the DDC bus presents approximately 12pF of capacitive loading. The ideal design will use a central pull-up resistor that is well-matched to the total load capacitance. In power module applications, the user should consider whether to place the pull-up resistor on the module or on the PCB of the end application. The minimum pull-up resistance should be limited to a value that enables any device to assert the bus to a voltage that will ensure a logic 0 (typically 0.8V at the device monitoring point) given the pull-up voltage (5V if tied to VR5) and the pull-down current capability of the ZL8802 (nominally 4mA). As with SMBus data and clock lines, the DDC data line should be routed with a closely coupled return or ground plane to minimize coupled interference (noise). Excessive noise on the DDC signal can cause the voltage on this line to cross the high and low logic thresholds of 2.0V and 0.8V respectively and will cause command transmissions to be interrupted and result in slow bus operation or missed commands. For less than 10 devices on the DDC bus a 10kΩ resistor provides good performance.

Phase Spreading

When multiple point-of-load converters share a common DC input supply, it is desirable to adjust the clock phase offset of each device such that not all devices have coincident rising edges. Setting each converter to start its switching cycle at a different point in time can dramatically reduce input capacitance requirements. Since the peak current drawn from the input supply is effectively spread out over a period of time, the peak current drawn at any given moment is reduced and the power losses proportional to I_{RMS}^2 are reduced.

In order to enable phase spreading, all converters must be synchronized to the same switching clock. Configuring the SYNC pin is described in "Configurable Pins" on page 12. Selecting the phase offset for the device is accomplished by selecting a device address according to Equation 4:

$$\text{Phase offset} = \text{device address} \times 45° \quad \text{(EQ. 4)}$$

The phase offset of each device may also be set to any value between 0° and 360° in 22.5° increments using the INTERLEAVE PMBus™ command.

Output Sequencing

A group of Intersil digital power devices may be configured to power up in a predetermined sequence. This feature is especially useful when powering advanced processors, FPGAs and ASICs that require one supply to reach its operating voltage prior to another supply reaching its operating voltage in order to avoid latch-up from occurring. Multidevice sequencing can be achieved by configuring each device using the SEQUENCE PMBus™ command.

Multiple device sequencing is achieved by issuing PMBus™ commands to assign the preceding device in the sequencing chain as well as the device that will follow in the sequencing chain.

The enable (EN) pins of all devices in a sequencing group must be tied together and driven high to initiate a sequenced turn-on of the group. Enable must be driven low to initiate a sequenced turn-off of the group. In order to achieve sequenced turn-off of a group of sequenced devices, all the devices should be configured to turn off using the "soft-off", or ramped down behavior, in the ON_OFF_CONFIG PMBus command.

When sequencing on, the first device to ramp up, called the "prequel", sends a message via the DDC bus to the next device, called the "sequel" when the prequel's Power-Good (PG) signal is driven high.

When sequencing off, the sequel will send a message to the prequel to begin the prequel's ramp down after the sequel has completed it's own ramp down.

Sequencing can also be accomplished by connecting the enable pin of a sequel device to the power-good pin of a prequel device. Sequencing is also achieved by using the TON_DELAY and TON_RISE commands and choosing appropriate delay and rise durations such that sequel devices start after their associated prequel devices. The drawback to this method is that if a prequel device fails to start properly, its sequel device will still start and ramp on according to its delay and rise time settings.

Fault Spreading

Digital-DC devices can be configured to broadcast a fault event over the DDC bus to the other devices in the group. When a fault occurs and the device is configured to shut down on a fault, the device will shut down and broadcast the fault event over the DDC bus. The other devices on the DDC bus will shut down together if configured to do so, and will attempt to restart in their prescribed order if configured to do so.

Active Current Sharing

The PWM outputs of the ZL8802 are used in parallel to create a dual phase power rail. The device outputs will share the current equally within a few percent, assuming all external sensing element variations and tolerances are negligible. Current sensing element tolerances must be taken into account, or adjusted for using the IOUT_CAL_GAIN and IOUT_CAL_OFFSET commands in any application.

The ZL8802 will current share between phases without utilizing output voltage droop.

Droop resistance is used in 4-phase current sharing to add artificial resistance in the output voltage path to control the slope of the load line curve, calibrating out the physical parasitic mismatches due to power train components and PCB layout.

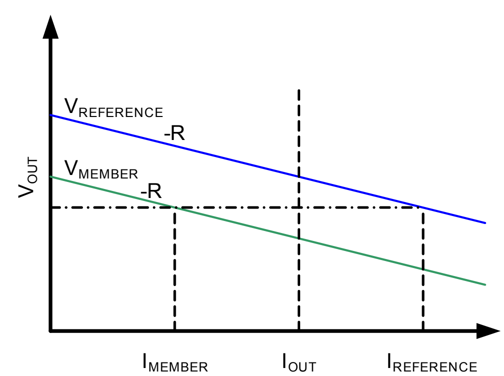


FIGURE 10. ACTIVE CURRENT SHARING

When current sharing up to 2 ZL8802s (4 phases total), the ZL8802 uses a low-bandwidth, first-order digital current sharing technique to balance the unequal device output loading by aligning the load lines of member devices to a reference device.

Upon system start-up, the lowest numbered phase is defined as the reference phase and all other phases are member phases.

The reference phase broadcasts its current over the DDC bus. The member phases use the reference current information to trim their reference voltages (V_{MEMBER}) to balance the current loading of each device in the system.

Figure 10 shows that, for load lines with identical slopes, the member reference voltage is increased towards the reference voltage which closes the gap between the inductor currents.

The relation between reference and member current and voltage is given by the following Equation 5:

$$V_{MEMBER} = V_{OUT} + R \times (I_{REFERENCE} - I_{MEMBER}) \quad \text{(EQ. 5)}$$

Where *R* is the value of the droop resistance. The VOUT_DROOP command is used to set the device output voltage droop to achieve 4-, 6- or 8-phase current sharing.

4-, 6- and 8-phase current sharing groups must have their DDC and SYNC pins tied together in order to achieve current sensing and ensure accurate phase offsets between current sharing phases.

Temperature Monitoring Using XTEMP Pin

Each channel of the ZL8802 supports measurement of an external device temperature using either a thermal diode integrated in a processor, FPGA or ASIC, or using a discrete diode-connected 2N3904 NPN transistor. Figure 11 illustrates the typical connections required. A noise filtering capacitor, not exceeding 100pF, should be connected across the external temperature sensing device. The external temperature sensors can be used to provide the temperature reading for over-temperature and under-temperature faults. The external sensors can also be used to provide more accurate temperature compensation for inductor DCR current sensing by being placed close to the inductor. These options for the external temperature sensors are selected using the User_config PMBus™ command.

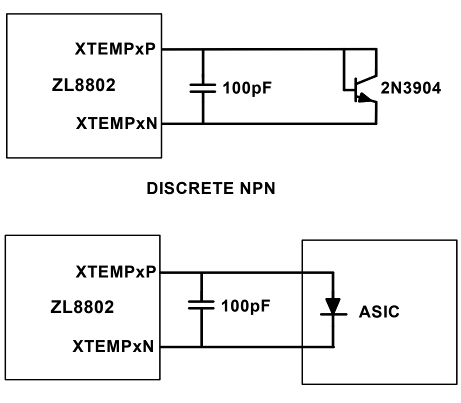


FIGURE 11. EXTERNAL TEMPERATURE MONITORING

Nonvolatile Memory and Security Features

The ZL8802 has internal nonvolatile memory where user configurations are stored. Integrated security measures ensure that the user can only restore the device to a level that has been made available to them. During the initialization process, the ZL8802 checks for stored values contained in its internal nonvolatile memory. The ZL8802 offers two internal memory storage units that are accessible by the user as follows:

User Store: The user store is the most commonly used store. It provides the ability to modify certain power supply settings while still protecting the equipment from modifying values that can lead to a system level fault. The equipment manufacturer would use the user store to achieve this goal.

Default Store: The default store is less commonly used. It provides a means to protect the circuit from damage by preventing the user from modifying certain values that are related to the physical construction of the circuit. In this case, the Original Equipment Manufacturer (OEM) would use the default store in a protected mode and allow the user to restore the device to its default settings. In this case the user store would be available to the end-user for making changes, but would restrict the user from restoring the device to the factory settings or modifying the default store.

The user store takes priority over the Default Store. If there are no values set in the user or default store, then the device will use the pin-strap setting value.

For details regarding protection of the user and default stores, see the PASSWORD PMBus command.

Monitoring via SMBus

A system controller can monitor a wide variety of different ZL8802 parameters through the SMBus interface. The device can monitor for fault conditions by monitoring the SALRT pin, which will be asserted when any number of preconfigured fault conditions occur.

The device can also be monitored continuously for any number of power conversion parameters including, but not limited to, the following:

- Input voltage
- Output voltage
- Input current
- Output current
- Internal junction temperature
- Temperature of an external device
- Switching frequency
- Duty cycle
- Fault status information

The PMBus™ Host should respond to SALRT as follows:

1. ZL device pulls SALRT low.
2. PMBus™ host detects that SALRT is now low, performs transmission with Alert Response Address to find which ZL device is pulling SALRT low.
3. PMBus™ host talks to the ZL device that has pulled SALRT low. The actions that the host performs are up to the system designer.

If multiple devices are faulting, SALRT will still be low after doing the above steps and will require transmission with the Alert Response Address repeatedly until all faults are cleared.

Please refer to “PMBus™ Command Detail” on page 27 for details on how to monitor specific parameters via the SMBus interface.

PMBus™ Command Summary

CODE	COMMAND NAME	DESCRIPTION	TYPE	DATA FORMAT	DEFAULT VALUE	DEFAULT SETTING
00h	PAGE	Selects Controller 0, 1, or both	R/W	BIT	00h	Page 0 Controller addressed
01h	OPERATION	Enable/disable, margin settings	R/W	BIT	00h	Immediate off, nominal margin
02h	ON_OFF_CONFIG	On/off configuration settings	R/W	BIT	17h	ENABLE pin control, active high
03h	CLEAR_FAULTS	Clears faults	Write	N/A	N/A	N/A
11h	STORE_DEFAULT_ALL	Stores values to default store	Write	N/A	N/A	N/A
12h	RESTORE_DEFAULT_ALL	Restores values from default store	Write	N/A	N/A	N/A
15h	STORE_USER_ALL	Stores values to user store	Write	N/A	N/A	N/A
16h	RESTORE_USER_ALL	Restores values from user store	Write	N/A	N/A	N/A
20h	VOUT_MODE	Reports V_{OUT} mode and exponent	Read	BIT	13h	Linear mode, exponent = -13
21h	VOUT_COMMAND	Sets nominal V_{OUT} set-point	R/W	L16u	N/A	Pin-strap setting
22h	VOUT_TRIM	Applies offset voltage to V_{OUT} set-point	R/W	L16s	0000h	0V
23h	VOUT_CAL_OFFSET	Applies offset voltage to V_{OUT} set-point	R/W	L16s	0000h	0V
24h	VOUT_MAX	Sets maximum V_{OUT} set-point	R/W	L16u	N/A	1.15 x VSET pin-strap setting
25h	VOUT_MARGIN_HIGH	Sets V_{OUT} set-point during margin high	R/W	L16u	N/A	1.05 x VSET pin-strap setting
26h	VOUT_MARGIN_LOW	Sets V_{OUT} set-point during margin low	R/W	L16u	N/A	0.95 x VSET pin-strap setting
27h	VOUT_TRANSITION_RATE	Sets V_{OUT} transition rate during margin commands	R/W	L11	BA00h	1V/ms
28h	VOUT_DROOP	Sets V/I slope for total rail output current (all phases combined)	R/W	L11	N/A	CFG pin-strap setting
33h	FREQUENCY_SWITCH	Sets switching frequency	R/W	L11	N/A	SYNC pin-strap setting
37h	INTERLEAVE	Configures phase offset during group operation	R/W	BIT	N/A	CFG pin-strap setting
38h	IOUT_CAL_GAIN	Sets impedance of current sense circuit	R/W	L11	B2AEh	0.67mΩ
39h	IOUT_CAL_OFFSET	Sets an offset to I_{OUT} sense circuit	R/W	L11	BD00h	-1.5A
40h	VOUT_OV_FAULT_LIMIT	Sets the V_{OUT} overvoltage fault threshold	R/W	L16u	N/A	1.10 x VSET pin-strap setting
41h	VOUT_OV_FAULT_RESPONSE	Sets the V_{OUT} overvoltage fault response	R/W	BIT	80h	Disable, no retry
44h	VOUT_UV_FAULT_LIMIT	Sets the V_{OUT} undervoltage fault threshold	R/W	L16u	N/A	0.85 x VSET pin-strap setting
45h	VOUT_UV_FAULT_RESPONSE	Sets the V_{OUT} undervoltage fault response	R/W	BIT	80h	Disable, no retry
46h	IOUT_OC_FAULT_LIMIT	Sets the I_{OUT} peak overcurrent fault threshold for each phase	R/W	L11	N/A	CFG pin-strap setting
4Bh	IOUT_UC_FAULT_LIMIT	Sets the I_{OUT} valley undercurrent fault threshold for each phase	R/W	L11	N/A	-1*IOUT_OC_FAULT_LIMIT from CFG pin-strap setting
4Fh	OT_FAULT_LIMIT	Sets the over-temperature fault limit	R/W	L11	EBE8h	+125°C
50h	OT_FAULT_RESPONSE	Sets the over-temperature fault response	R/W	BIT	BFh	Continuous retry, 280ms retry delay
51h	OT_WARN_LIMIT	Sets the over-temperature warning limit	R/W	L11	EB70h	+110°C
52h	UT_WARN_LIMIT	Sets the under-temperature warning limit	R/W	L11	DC40h	-30°C
53h	UT_FAULT_LIMIT	Sets the under-temperature fault limit	R/W	L11	E530h	-45°C
54h	UT_FAULT_RESPONSE	Sets the under-temperature fault response	R/W	BIT	BFh	Continuous retry, 280ms retry delay
55h	VIN_OV_FAULT_LIMIT	Sets the V_{IN} overvoltage fault threshold	R/W	L11	D380h	14V

PMBus™ Command Summary (Continued)

CODE	COMMAND NAME	DESCRIPTION	TYPE	DATA FORMAT	DEFAULT VALUE	DEFAULT SETTING
56h	VIN_OV_FAULT_RESPONSE	Sets the V_{IN} overvoltage fault response	R/W	BIT	80h	Disable, no retry
57h	VIN_OV_WARN_LIMIT	Sets the V_{IN} overvoltage warning threshold	R/W	L11	D360h	13.5V
58h	VIN_UV_WARN_LIMIT	Sets the V_{IN} undervoltage warning threshold	R/W	L11	N/A	1.1 x UVLO pin-strap setting
59h	VIN_UV_FAULT_LIMIT	Sets the V_{IN} undervoltage fault threshold	R/W	L11	N/A	UVLO pin-strap setting
5Ah	VIN_UV_FAULT_RESPONSE	Sets the V_{IN} undervoltage fault response	R/W	BIT	BFh	Continuous retries, 280ms retry delay
5Eh	POWER_GOOD_ON	Sets the voltage threshold for power-good indication	R/W	L16u	N/A	0.9 x VSET pin-strap setting
60h	TON_DELAY	Sets the delay time from enable to V_{OUT} rise	R/W	L11	CA80h	5ms
61h	TON_RISE	Sets the rise time of V_{OUT} after ENABLE and TON_DELAY	R/W	L11	CA80h	5ms
64h	TOFF_DELAY	Sets the delay time from DISABLE to start of V_{OUT} fall	R/W	L11	CA80h	5ms
65h	TOFF_FALL	Sets the fall time for VOUT after DISABLE and TOFF_DELAY	R/W	L11	CA80h	5ms
78h	STATUS_BYTE	First byte of STATUS_WORD	Read	BIT	00h	No faults
79h	STATUS_WORD	Summary of critical faults	Read	BIT	0000h	No faults
7Ah	STATUS_VOUT	Reports V_{OUT} warnings/faults	Read	BIT	00h	No faults
7Bh	STATUS_IOUT	Reports I_{OUT} warnings/faults	Read	BIT	00h	No faults
7Ch	STATUS_INPUT	Reports input warnings/faults	Read	BIT	00h	No faults
7Dh	STATUS_TEMP	Reports temperature warnings/faults	Read	BIT	00h	No faults
7Eh	STATUS_CML	Reports communication, memory, logic errors	Read	BIT	00h	No faults
80h	STATUS_MFR_SPECIFIC	Reports voltage monitoring/clock synchronization faults	Read	BIT	00h	no faults
88h	READ_VIN	Reports input voltage measurement	Read	L11	N/A	N/A
89h	READ_IIN	Reports input current measurement	Read	L11	N/A	N/A
8Bh	READ_VOUT	Reports output voltage measurement	Read	L16u	N/A	N/A
8Ch	READ_IOUT	Reports output current measurement	Read	L11	N/A	N/A
8Dh	READ_TEMPERATURE_1	Reports internal temperature measurement	Read	L11	N/A	N/A
8Eh	READ_TEMPERATURE_2	Reports external temperature measurement from XTEMP pins	Read	L11	N/A	N/A
8Fh	READ_TEMPERATURE_3	Reports external temperature measurement from VMON/TMON pin.	Read	L11	N/A	N/A
94h	READ_DUTY_CYCLE	Reports actual duty cycle	Read	L11	N/A	N/A
95h	READ_FREQUENCY	Reports actual switching frequency	Read	L11	N/A	N/A
98h	PMBUS_REVISION	Reports the PMBUS revision used	Read	BIT	22h	P1 R1.2, P2 R1.2
99h	MFR_ID	Sets a user defined identification	R/W	ASC	N/A	<null>
9Ah	MFR_MODEL	Sets a user defined model	R/W	ASC	N/A	<null>
9Bh	MFR_REVISION	Sets a user defined revision	R/W	ASC	N/A	<null>

PMBus™ Command Summary (Continued)

CODE	COMMAND NAME	DESCRIPTION	TYPE	DATA FORMAT	DEFAULT VALUE	DEFAULT SETTING
9Ch	MFR_LOCATION	Sets a user defined location identifier	R/W	ASC	N/A	<null>
9Dh	MFR_DATE	Sets a user defined date	R/W	ASC	N/A	<null>
9Eh	MFR_SERIAL	Sets a user defined serialized identifier	R/W	ASC	N/A	<null>
ADh	IC_DEVICE_ID	Reports device identification information	Read	CUS	49A02D00h	Intersil ZL8802
AEh	IC_DEVICE_REV	Reports device revision information	Read	CUS	01000000h	Initial Release
B0h	USER_DATA_00	Sets user defined data	R/W	ASC	N/A	<null>
CEh	MIN_VOUT_REG	Sets a minimum start-up voltage	R/W	L11	0000h	0mV
D0h	ISENSE_CONFIG	Configures current sensing circuitry	R/W	BIT	620Eh	Downslope, 5 fault count, 384ns blanking, high range
D1h	USER_CONFIG	Configures several user-level features	R/W	BIT	N/A	Set by CFG pin-strap setting
D2h	IIN_CAL_GAIN	Sets the resistance of the input current sensing resistor	R/W	L11	C200h	2mΩ
D3h	DDC_CONFIG	Configures the DDC addressing and current sharing	R/W	BIT	N/A	Set by pin-strapped PMBus™ address and CFG pin-strap setting
D4h	POWER_GOOD_DELAY	Sets the delay between PG threshold and PG assertion	R/W	L11	BA00h	1ms
D5h	MULTI_PHASE_RAMP_GAIN	Adjusts the ramp-up and ramp-down rate by setting the feedback gain	R/W	CUS	03h	3
D6h	INDUCTOR	Sets the inductor value	R/W	L11	B133h	0.3µH
D7h	SNAPSHOT_FAULT_MASK	Masks faults that cause a snapshot to be taken	R/W	BIT	0000h	No faults masked
D8h	OVUV_CONFIG	Configures output voltage OV/UV fault detection	R/W	BIT	00h	Low side FET off on fault, 1 violation triggers fault.
D9h	XTEMP_SCALE	Calibrates external temperature sensor	R/W	L11	BA00h	1/degree C
DAh	XTEMP_OFFSET	Offset calibration for external temperature sensor	R/W	L11	0000h	No offset
DBh	MFR_SMBALERT_MASK	Identifies which fault limits will not assert SALRT	R/W	Custom	00..00h	N/A
DCh	TEMPCO_CONFIG	Sets tempco settings	R/W	BIT	00h	0ppm/°C
DDh	PINSTRAP_READ_STATUS	Reads pin-strap settings	Read	BIT	N/A	Set by pin-straps
DFh	ASCR_CONFIG	Configures the ASCR settings	R/W	BIT	N/A	ASCRCFG pin-strap setting
E0h	SEQUENCE	DDC rail sequencing configuration	R/W	BIT	00h	Prequel and sequel disabled
E1h	TRACK_CONFIG	Configures voltage tracking.	R/W	BIT	00h	Tracking disabled
E2h	DDC_GROUP	Configures group ID, fault spreading, OPERATION and V_{OUT}	R/W	BIT	N/A	Set by CFG pin-strap
E4h	DEVICE_ID	Returns the device identifier string	Read	ASC	TBD	ZL8802, current revisions
E5h	MFR_IOUT_OC_FAULT_RESPONSE	Configures the I_{OUT} overcurrent fault response	R/W	BIT	80h	Disable, no retry
E6h	MFR_IOUT_UC_FAULT_RESPONSE	Configures the I_{OUT} undercurrent fault response	R/W	BIT	80h	Disable, no retry
E7h	IOUT_AVG_OC_FAULT_LIMIT	Sets the I_{OUT} average overcurrent fault threshold	R/W	L11	N/A	Set by CFG pin-strap
E8h	IOUT_AVG_UC_FAULT_LIMIT	Sets the I_{OUT} average undercurrent fault threshold	R/W	L11	N/A	-1* IOUT_AVG_OC_FAULT_LIMIT from CFG pin-strap setting

PMBus™ Command Summary (Continued)

CODE	COMMAND NAME	DESCRIPTION	TYPE	DATA FORMAT	DEFAULT VALUE	DEFAULT SETTING
E9h	USER_GLOBAL_CONFIG	Sets options pertaining to advanced features	R/W	BIT	N/A	Set by CFG pin-strap setting
EAh	SNAPSHOT	32-byte read-back of parametric and status values	Read	BIT	N/A	<null>
F0h	LEGACY_FAULT_GROUP	Configures fault group compatibility with older Intersil digital power devices	R/W	BIT	00000000h	<null>
F3h	SNAPSHOT_CONTROL	Snapshot feature control command	R/W	BIT	00h	N/A
F4h	RESTORE_FACTORY	Restores device to the hard-coded default values	Write	N/A	N/A	N/A
F5h	MFR_VMON_OV_FAULT_LIMIT	Sets the VMON overvoltage fault threshold	R/W	L11	C266h	2.4V, SPS OT trip voltage
F6h	MFR_VMON_UV_FAULT_LIMIT	Sets the VMON undervoltage fault threshold	R/W	L11	B0CCh	0.2V, corresponds to -50°C
F7h	MFR_READ_VMON	Reads the VMON voltage	Read	L11	N/A	N/A
F8h	VMON_OV_FAULT_RESPONSE	Configures the VMON overvoltage fault response	R/W	BIT	BFh	Continuous retry
F9h	VMON_UV_FAULT_RESPONSE	Configures the VMON undervoltage fault response	R/W	BIT	BFh	Continuous retry
FAh	SECURITY_LEVEL	Reports the security level	Read	Hex	01h	Public security level
FBh	PRIVATE_PASSWORD	Sets the private password string	R/W	ASC	00...00h	<null>
FCh	PUBLIC_PASSWORD	Sets the public password string	R/W	ASC	00...00h	<null>
FDh	UNPROTECT	Identifies which commands are protected	R/W	Custom	FF...FFh	No commands are protected

PMBus™ Use Guidelines

The PMBus is a powerful tool that allows the user to optimize circuit performance by configuring the ZL8802 for their application. When configuring the ZL8802 in a circuit, the ZL8802 should be disabled whenever most settings are changed with PMBus commands. Some exceptions to this recommendation are OPERATION, ON_OFF_CONFIG, CLEAR_FAULTS, VOUT_COMMAND, VOUT_MARGIN_HIGH, VOUT_MARGIN_LOW and ASCCR_CONFIG. While the device is enabled any command can be read. Many commands do not take effect until after the device has been reenabled, hence the recommendation that commands that change device settings are written while the device is disabled.

When sending the STORE_DEFAULT_ALL, STORE_USER_ALL, RESTORE_DEFAULT_ALL and RESTORE_USER_ALL commands, it is recommended that no other commands are sent to the device for 100ms after sending STORE or RESTORE commands.

In addition, there should be a 2ms delay between repeated READ commands sent to the same device. When sending any other command, a 5ms delay is recommended between repeated commands sent to the same device.

SUMMARY:

All commands can be read at any time.

Always disable the ZL8802 when writing commands that change device settings. Exceptions to this rule are commands intended to be written while the device is enabled, for example, VOUT_MARGIN_HIGH.

To be sure a change to a device setting has taken effect, write the STORE_USER_ALL command, then cycle input power and reenable the device.