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Crimzon® Infrared Microcontrollers

ZLP12840 OTP MCU

with Learning Amplification

Product Specification

PS024410-0108

PRELIMINARY

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Revision History

Each instance in Revision History reflects a change to this document from its previous revision. For more details, refer to the corresponding pages and appropriate links in the table below.

Date	Revision Level	Description	Page No
January 2008	10	Updated Table 61.	129
September 2007	09	Updated Features section, Figure 2, Figure 3, SMR1 Register Events, and Ordering Information section. Added Applications and Support Tools section.	1, 5, 8, 103, and 141
July 2007	08	Updated Disclaimer page and implemented style guide.	All
February 2007	07	Updated Voltage Detection section.	97
January 2006	06	Removed the trademark symbol (TM) from LXM.	All

Table of Contents

Architectural Overview

Zilog's ZLP12840 one-time-programmable (OTP) MCU is a member of the Crimzon® family of infrared microcontrollers. It provides a directly-compatible code upgrade path to other Crimzon MCUs, offers a robust learning function, and features up to 128 KB OTP read-only memory (ROM) and 1004 bytes of general-purpose random access memory (RAM). Two timers allow the generation of complex signals while performing other counting operations. A UART allows the ZLP12840 MCU to be a Slave/Master database chip. When the UART is not in use, the Baud Rate Generator can be used as a third timer. Enhanced Stop Mode Recovery (SMR) features allow the ZLP12840 MCU to awaken from STOP mode on any change of logic, and on any combination of the 12 SMR inputs. The SMR source can also be used as an interrupt source.

Many high-end remote control units offer a learning function. Simply stated, a learning function allows a replacement remote unit to learn most infrared signals from the original remote unit and regenerate the signal. However, the amplifying circuits of many learning remotes are expensive, are not tuned well. ZLP12840 MCU is the first chip dedicated to solve this problem because it offers a built-in tuned amplification circuit in a wide range of positions and battery voltages. The only external component required is a photodiode.

The ZLP12840 MCU greatly reduces system cost, yet improves learning function reliability. With all new features, the ZLP12840 MCU is excellent for infrared remote control and other MCU applications.

Features

Table 1 lists the memory, input/output (I/O), and power features of the ZLP12840 one-time-programmable microcontroller.

Table 1. ZLP12840 OTP MCU Features

Device	OTP ROM (KB)	RAM* (Bytes)	I/O Lines	Voltage Range
ZLP12840 MCU	32, 64, 96, 128	1004	24 or 16	2.0–3.6V

*General-purpose registers implemented as random access memory.

The ZLP12840 MCU supports 20 interrupt sources with 6 interrupt vectors that are listed below:

- Two from T8, T16 time-out and capture
- Three from UART Tx, UART Rx, UART BRG

- One from LVD
- 14 from SMR source P20-P27, P30-P33, P00, P07
  - Any change of logic from P20-P27, P30-P33 can generate an interrupt or SMR

Additional features include:

- IR learning amplifier
- Low power consumption—11 mW (typical)
- Three standby modes:
  - STOP—2 µA (typical)
  - HALT—0.8 mA (typical)
  - Low-Voltage Reset
- Intelligent counter/timer architecture to automate generation or reception and demodulation of complex waveform and pulsed signals:
  - One programmable 8-bit counter/timer with two capture registers and two load registers
  - One programmable 16-bit counter/timer with one 16-bit capture register pair and one 16-bit load register pair
  - Programmable input glitch filter for pulse reception
  - The UART baud rate generator can be used as another 8-bit timer when the UART is not in use
- Six priority interrupts
  - Three external/UART interrupts
  - Two assigned to counter/timers
  - One low-voltage detection interrupt
- 8-bit UART
  - R_X, T_X interrupts
  - 4800, 9600, 19200 and 38400 baud rates
  - Parity Odd/Even/None
  - Stop bits 1/2
- Low-Voltage Detection and High-Voltage Detection Flags
- Programmable Watchdog Timer/Power-On Reset circuits
- Two on-board analog comparators with independent reference voltages and programmable interrupt polarity
- One-time programmable EPROM option bits (ON/OFF)
  - Port 0 pins 0–3 pull-up transistors
  - Port 0 pins 4–7 pull-up transistors

- Port 2 pins 0–7 pull-up transistors
- EPROM Protection
- Watchdog timer enabled at Power-On Reset

Note: *All signals with an overline, "‾", are active Low. For example, B/$\overline{W}$, in which WORD is active Low, and $\overline{B}$/W, in which BYTE is active Low.*

Power connections use the conventional descriptions listed in Table 2.

Table 2. Power Connections

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

Functional Block Diagram

Figure 1 displays the functional blocks of the ZLP12840 microcontroller.

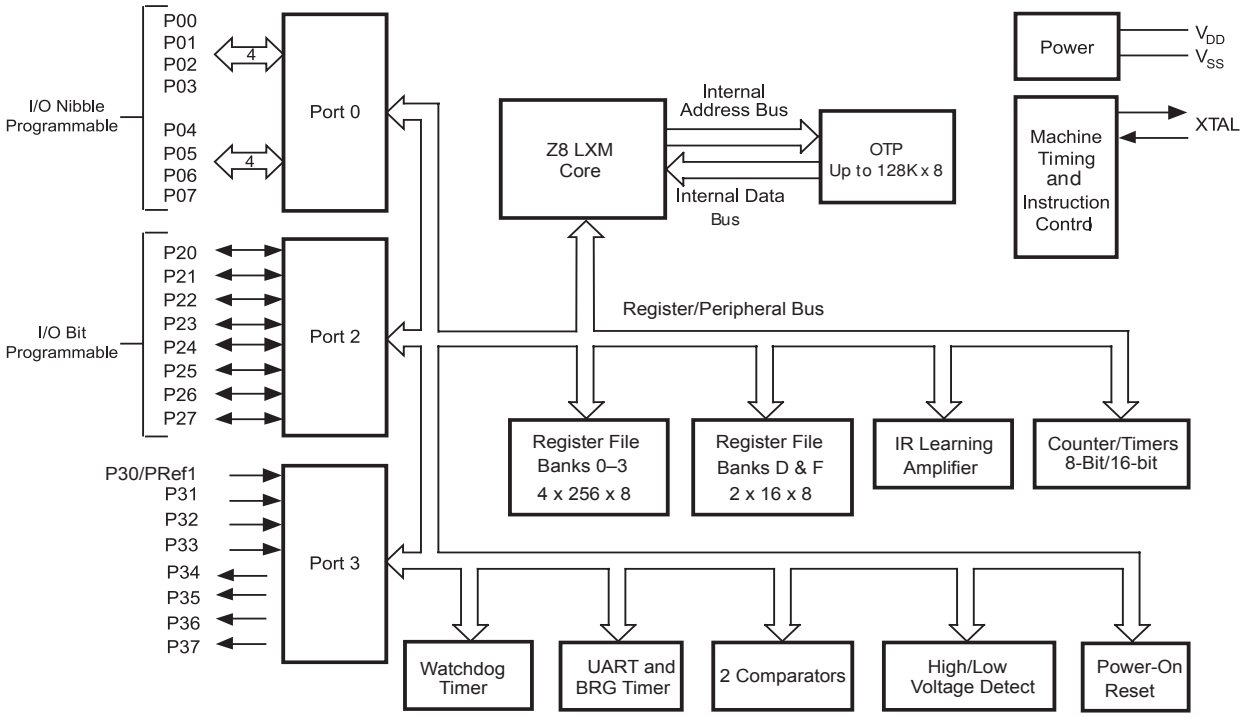

Figure 1. ZLP12840 MCU Functional Block Diagram

Pin Description

Figure 2 displays the pin configuration of the ZLP12840 device in the 20-pin PDIP, SOIC, and SSOP packages.

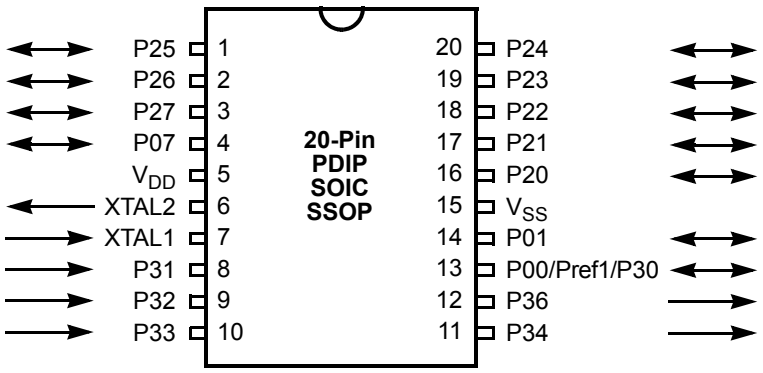

Figure 2. ZLP12840 MCU 20-Pin PDIP/SOIC/SSOP Pin Configuration

Table 3 describes the functions and signal directions of each pin within the 20-pin PDIP, SOIC, and SSOP packages sequentially by pin.

Table 3. ZLP12840 MCU 20-Pin PDIP/SOIC/SSOP Sequential Pin Identification

Pin No	Symbol	Function	Direction
1	P25	Port 2, bit 5	Input/Output
2	P26	Port 2, bit 6	Input/Output
3	P27	Port 2, bit 7	Input/Output
4	P07	Port 0, bit 7	Input/Output
5	V_{DD}	Power Supply	
6	XTAL2	Crystal oscillator	Output
7	XTAL1	Crystal oscillator	Input
8	P31	Port 3, bit 1	Input
9	P32	Port 3, bit 2	Input
10	P33	Port 3, bit 3	Input
11	P34	Port 3, bit 4	Output
12	P36	Port 3, bit 6	Output

Table 3. ZLP12840 MCU 20-Pin PDIP/SOIC/SSOP Sequential Pin Identification (Continued)

Pin No	Symbol	Function	Direction
13[1]	P00	Port 0, bit 0	Input/Output
	P30	Port 3, bit 0	Input
14	P01	Port 0, bit 1	Input/Output
15	V_{SS}	Ground	
16	P20	Port 2, bit 0	Input/Output
17	P21	Port 2, bit 1	Input/Output
18	P22	Port 2, bit 2	Input/Output
19	P23	Port 2, bit 3	Input/Output
20	P24	Port 2, bit 4	Input/Output

[1]When the Port 0 high-nibble pull-up option is enabled and the P30 input is Low, current flows through the pull-up to Ground.

Table 4 describes the functions and signal direction of each pin within the 20-pin PDIP, SOIC, and SSOP packages by function.

Table 4. ZLP12840 MCU 20-Pin PDIP/SOIC/SSOP Functional Pin Identification

Pin No	Symbol	Function	Direction
13[1]	P00	Port 0, bit 0	Input/Output
	P30	Port 3, bit 0	Input
14	P01	Port 0, bit 1	Input/Output
4	P07	Port 0, bit 7	Input/Output
16	P20	Port 2, bit 0	Input/Output
17	P21	Port 2, bit 1	Input/Output
18	P22	Port 2, bit 2	Input/Output
19	P23	Port 2, bit 3	Input/Output
20	P24	Port 2, bit 4	Input/Output
1	P25	Port 2, bit 5	Input/Output
2	P26	Port 2, bit 6	Input/Output
3	P27	Port 2, bit 7	Input/Output
8	P31	Port 3, bit 1	Input
9	P32	Port 3, bit 2	Input
10	P33	Port 3, bit 3	Input
11	P34	Port 3, bit 4	Output
12	P36	Port 3, bit 6	Output
5	V_{DD}	Power Supply	
15	V_{SS}	Ground	
7	XTAL1	Crystal oscillator	Input
6	XTAL2	Crystal oscillator	Output

[1]When the Port 0 high-nibble pull-up option is enabled and the P30 input is Low, current flows through the pull-up to Ground.

Figure 3 displays the pin configuration of the ZLP12840 device in the 28-pin PDIP, SOIC, and SSOP packages.

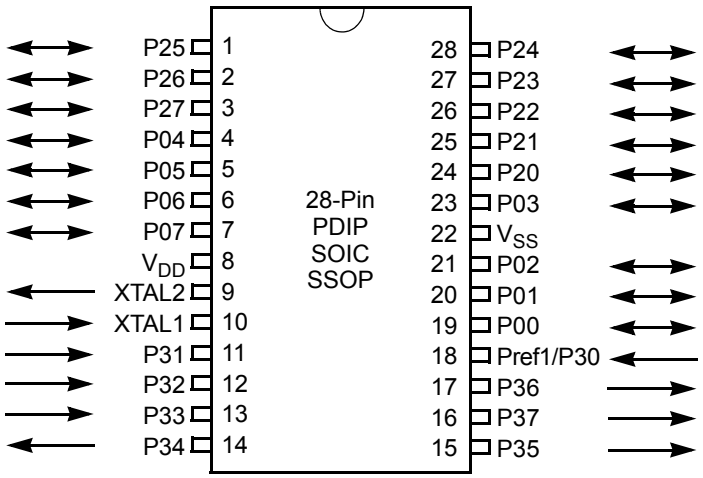

Figure 3. ZLP12840 MCU 28-Pin PDIP/SOIC/SSOP Pin Configuration

Table 5 describes the functions and signal directions of each pin within the 28-pin PDIP, SOIC, and SSOP packages sequentially by pin.

Table 5. ZLP12840 MCU 28-Pin PDIP/SOIC/SSOP Sequential Pin Identification

Pin	Symbol	Function	Direction
1	P25	Port 2, bit 5	Input/Output
2	P26	Port 2, bit 6	Input/Output
3	P27	Port 2, bit 7	Input/Output
4	P04	Port 0, bit 4	Input/Output
5	P05	Port 0, bit 5	Input/Output
6	P06	Port 0, bit 6	Input/Output
7	P07	Port 0, bit 7	Input/Output
8	V_{DD}	Power supply	
9	XTAL2	Crystal oscillator	Output
10	XTAL1	Crystal oscillator	Input
11	P31	Port 3, bit 1	Input
12	P32	Port 3, bit 2	Input
13	P33	Port 3, bit 3	Input
14	P34	Port 3, bit 4	Output
15	P35	Port 3, bit 5	Output
16	P37	Port 3, bit 7	Output
17	P36	Port 3, bit 6	Output
18	P30	Port 3, bit 0; connect to V_{CC} if not used	Input
19	P00	Port 0, bit 0	Input/Output
20	P01	Port 0, bit 1	Input/Output
21	P02	Port 0, bit 2	Input/Output
22	V_{SS}	Ground	
23	P03	Port 0, bit 3	Input/Output
24	P20	Port 2, bit 0	Input/Output
25	P21	Port 2, bit 1	Input/Output
26	P22	Port 2, bit 2	Input/Output
27	P23	Port 2, bit 3	Input/Output
28	P24	Port 2, bit 4	Input/Output

Table 6 describes the functions and signal directions of each pin within the 28-pin PDIP, SOIC, and SSOP packages by function.

Table 6. ZLP12840 MCU 28-Pin PDIP/SOIC/SSOP Functional Pin Identification

Pin	Symbol	Function	Direction
19	P00	Port 0, bit 0	Input/Output
20	P01	Port 0, bit 1	Input/Output
21	P02	Port 0, bit 2	Input/Output
23	P03	Port 0, bit 3	Input/Output
4	P04	Port 0, bit 4	Input/Output
5	P05	Port 0, bit 5	Input/Output
6	P06	Port 0, bit 6	Input/Output
7	P07	Port 0, bit 7	Input/Output
24	P20	Port 2, bit 0	Input/Output
25	P21	Port 2, bit 1	Input/Output
26	P22	Port 2, bit 2	Input/Output
27	P23	Port 2, bit 3	Input/Output
28	P24	Port 2, bit 4	Input/Output
1	P25	Port 2, bit 5	Input/Output
2	P26	Port 2, bit 6	Input/Output
3	P27	Port 2, bit 7	Input/Output
18	P30	Port 3, bit 0; connect to V_{CC} if not used	Input
11	P31	Port 3, bit 1	Input
12	P32	Port 3, bit 2	Input
13	P33	Port 3, bit 3	Input
14	P34	Port 3, bit 4	Output
15	P35	Port 3, bit 5	Output
17	P36	Port 3, bit 6	Output
16	P37	Port 3, bit 7	Output
8	V_{DD}	Power supply	
22	V_{SS}	Ground	
10	XTAL1	Crystal oscillator	Input
9	XTAL2	Crystal oscillator	Output

I/O Port Pin Functions

The ZLP12840 MCU features three 8-bit ports, which are described below.

- Port 0 is nibble-programmable as either input or output
- Port 2 is bit-programmable as either input or output
- Port 3 features four inputs on the lower nibble and four outputs on the upper nibble

Note: *Port 0 and 2 internal pull-ups are disabled on any pin or group of pins when programmed into output mode.*

Caution: *The CMOS input buffer for each port 0 or 2 pin is always connected to the pin, even when the pin is configured as an output. If the pin is configured as an open-drain output and no external signal is applied, a High output state can cause the CMOS input buffer to float. This might lead to excessive leakage current of more than 100 µA. To prevent this leakage, connect the pin to an external signal with a defined logic level or ensure its output state is Low, especially during STOP mode.*

Port 0, 1, and 2 have both input and output capability. The input logic is always present no matter whether the port is configured as input or output. When doing a READ instruction, the MCU reads the actual value at the input logic but not from the output buffer. In addition, the instructions of OR, AND, and XOR have the Read-Modify-Write sequence. The MCU first reads the port, and then modifies the value and load back to the port.

Precaution must be taken if the port is configured as open-drain output or if the port is driving any circuit that makes the voltage different from the desired output logic. For example, pins P00–P07 are not connected to anything else. If it is configured as open-drain output with output logic as ONE, it is a floating port and reads back as ZERO. The following instruction sets P00-P07 all Low.

```
AND P0,#%F0
```

Table 7 summarizes the registers used to control I/O ports. Some port pin functions can also be affected by control registers for other peripheral functions.

Table 7. I/O Port Control Registers

Address (Hex)						
12-Bit	Bank	8-Bit	Register Description	Mnemonic	Reset	Page No
000	0–3	00	Port 0	P0	XXh	21
002	0–3	02	Port 2	P2	XXh	23
003	0–3	03	Port 3	P3	0Xh	25
0F6	All	F6	Port 2 Mode Register	P2M	FFh	22
0F7	All	F7	Port 3 Mode Register	P3M	XXXX_X000b	24
0F8	All	F8	Port 0 Mode Register	P01M	X1XX_XXX1b	20
F00	F	00	Port Configuration Register	PCON	XXXX_X1X0b	20

Port 0

Port 0 is an 8-bit, bidirectional, CMOS-compatible port. Its eight I/O lines are configured under software control to create a nibble I/O port. The output drivers are push/pull or open-drain, controlled by bit 2 of the PCON register.

If one or both nibbles are required for I/O operation, they must be configured by writing to the Port 0 Mode Register (P01M). After a hardware reset or a Stop Mode Recovery, Port 0 is configured as an input port.

Port 0, bit 7 is used as the transmit output of the UART when UART Tx is enabled.The I/O function of Port 0, bit 7 is overridden by the UART serial output (TxD) when UART Tx is enabled (UCTL[7] = 1). The pin must be configured as an output for TxD data to reach the pin (P0M[6] = 0).

An optional pull-up transistor is available as an OTP option on all Port 0 bits with nibble select. For information on configuration, see Figure 4 on page 13.

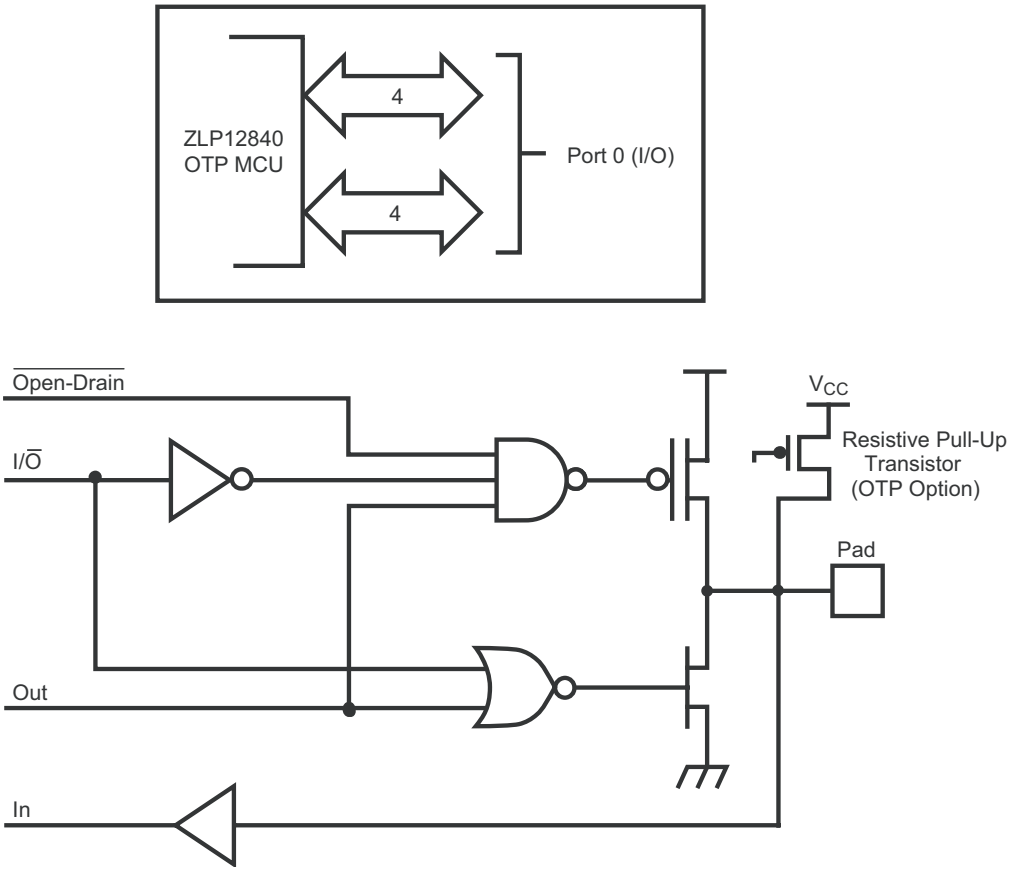

Figure 4. Port 0 Configuration

Port 2

Port 2 is an 8-bit, bidirectional, CMOS-compatible I/O port. Its eight I/O lines can be independently configured under software control as inputs or outputs. Port 2 is always available for I/O operation. An EPROM option bit is available to connect eight pull-up transistors on this port. Bits programmed as outputs are globally programmed as either push/pull or open-drain. The Power-On Reset function resets with the eight bits of Port 2 [P27:20] configured as inputs.

Port 2 also has an 8-bit input OR and AND gate and edge detection circuitry, which can be used to wake up the part. P20 can be programmed to access the edge-detection circuitry in DEMODULATION mode. For information on configuration, see Figure 5 on page 14.

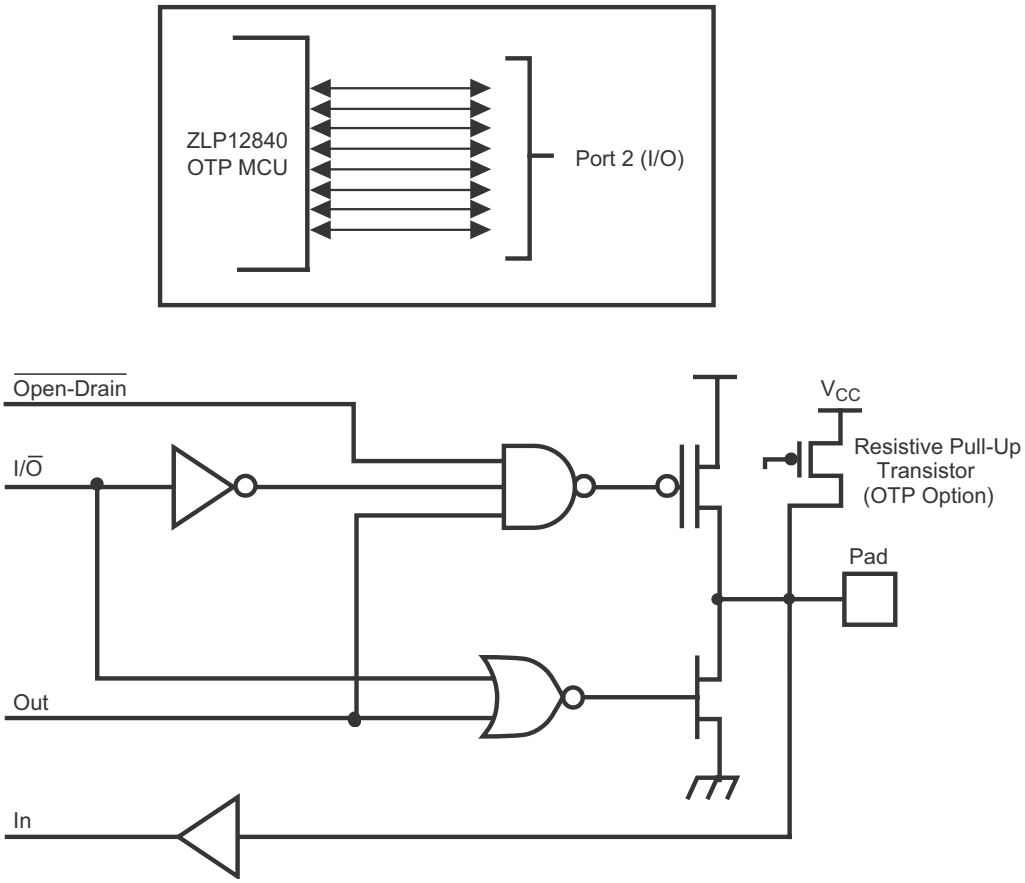

Figure 5. Port 2 Configuration

Port 3

Port 3 is a 8-bit, CMOS-compatible fixed I/O port. Port 3 consists of four fixed inputs (P33:P30) and four fixed outputs (P37:P34). P30, P31, P32, and P33 are standard CMOS inputs, and can be configured under software control as interrupts, as receive data input to the UART block, as input to comparator circuits, or as input to the IR learning AMP. P34, P35, P36, and P37 are push/pull outputs, and can be configured as outputs from the counter/timers. For information on configuration, see Figure 6 on page 15.

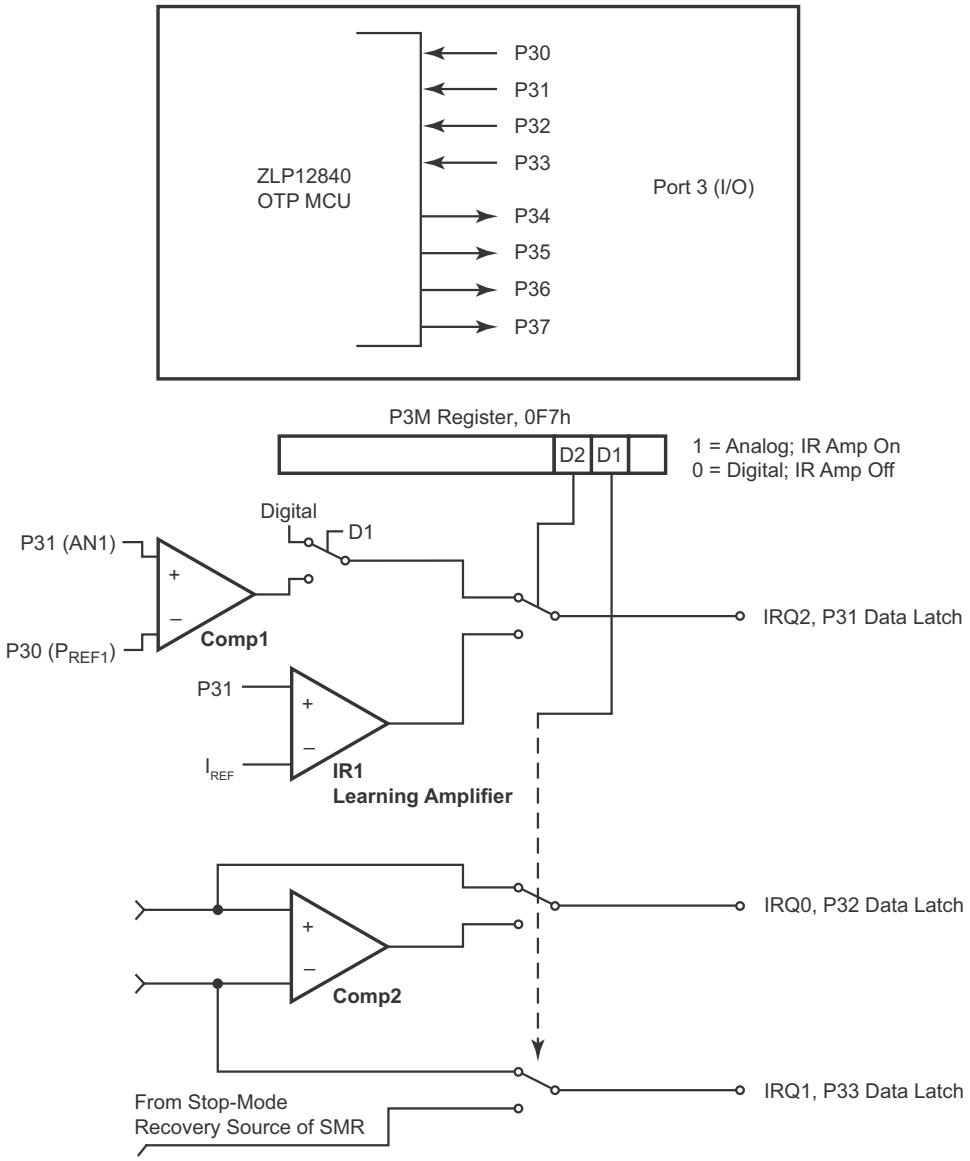

Figure 6. Port 3 Configuration

P31 can be used as an interrupt, analog comparator input, infrared learning amplifier input, normal digital input pin and as a Stop Mode Recovery source. When bit 2 of the Port 3 Mode Register (P3M) is set, P31 is used as the infrared learning amplifier, IR1. The reference source for IR1 is GND. The infrared learning amplifier is disabled during STOP mode. When bit 1 of P3M is set, the part is in ANALOG mode and the analog comparator, COMP1 is used. The reference voltage for COMP1 is P30 (P_{REF1}). When in ANALOG mode, P30 cannot be read as a digital input when the CPU reads bit 0 of the Port 3

Register; such reads always return a value of 1. Also, when in ANALOG mode, P31 cannot be used as a Stop Mode Recovery source because in STOP mode, the comparator is disabled, and its output will not toggle. The programming of Bit 2 of the P3M register takes precedence over the programming of Bit 1 in determining the function of P31. If both bits are set, P31 functions as an IR learning amplifier instead of an analog comparator. The output of the function selected for P31 can be used as a source for IRQ2 interrupt assertion (see Figure 6 on page 15). The IRQ2 interrupt can be configured to be based upon detecting a rising, falling, or edge-triggered input change using bit 6 and bit 7 of the IRQ register. The P31 output stage signal also goes to the Counter/Timer edge detection circuitry similar to P20.

P32 can be used as an interrupt, analog comparator, UART receiver, normal digital input and as a Stop Mode Recovery source. When bit 6 of UCTL is set, P32 functions as a receive input for the UART. When bit 1 of the P3M Register is set, thereby placing the part into ANALOG mode, P32 functions as an analog comparator, Comp2. The reference voltage for Comp2 is P33 ($P_{REF}2$). P32 can be used as a rising, falling or edge-triggered interrupt, IRQ0, using IRQ register bits 6 and 7. If UART receiver interrupts are not enabled, the UART receive interrupt is used as the source of interrupts for IRQ0 instead of P32. When in ANALOG mode P32 cannot be used as a Stop Mode Recovery source because the comparators are turned OFF in STOP mode.

When in ANALOG mode, P33 cannot be read through bit 3 of the Port 3 Register as a digital input by the CPU. In this case, a read of bit 3 of the Port 3 Register indicates whether a Stop Mode Recovery condition exists. Reading a value of 0 indicates that a Stop Mode Recovery condition does exist; if the ZLP12840 MCU is presently in STOP mode, it will exit STOP mode. Reading a value of 1 indicates that no condition exists to remove the ZLP12840 from STOP mode. Additionally, when in ANALOG mode, P33 cannot be used as an interrupt source. Instead, the existence of a Stop Mode Recovery condition can generate an interrupt, if enabled. P33 can be used as a falling-edge interrupt, IRQ1, when not in ANALOG mode. IRQ1 is also used as the UART T_X interrupt and the UART BRG interrupt. Only one source is active at a time. If bits 7 and 5 of UCTL are set to 1, IRQ1 will transmit an interrupt when the Transmit Shift Register is empty. If bits 0 and 5 of UCTL are set to 1 and bit 6 of UCTL is cleared to 0, the BRG interrupts will activate IRQ1.

Note: *Comparators and the IR amplifier are powered down by entering STOP mode. For P30:P33 to be used as a Stop Mode Recovery source during STOP mode, these inputs must be placed into DIGITAL mode. When in ANALOG mode, do not configure any Port 3 input as a Stop Mode Recovery source. The configuration of these inputs must be re-initialized after Stop Mode Recovery or Power-On Reset.*

Table 8. Summary of Port 3 Pin Functions

Pin	I/O	Counter/Timers	Comparator	Interrupt	IRAMP	UART
P30	IN		REF1			
P31	IN	IN	AN1	IRQ2	IR1	
P32	IN		AN2	IRQ0		UART Rx
P33	IN		REF2	IRQ1		
P34	OUT	T8	AO1		IROUT	
P35	OUT	T16				
P36	OUT	T8/T16				
P37	OUT		AO2			

Port 3 also provides output for each of the counter/timers and the AND/OR Logic (see Figure 7). Control is performed by programming CTR1 bits 5 and 4, CTR0 bit 0, and CTR2 bit 0.

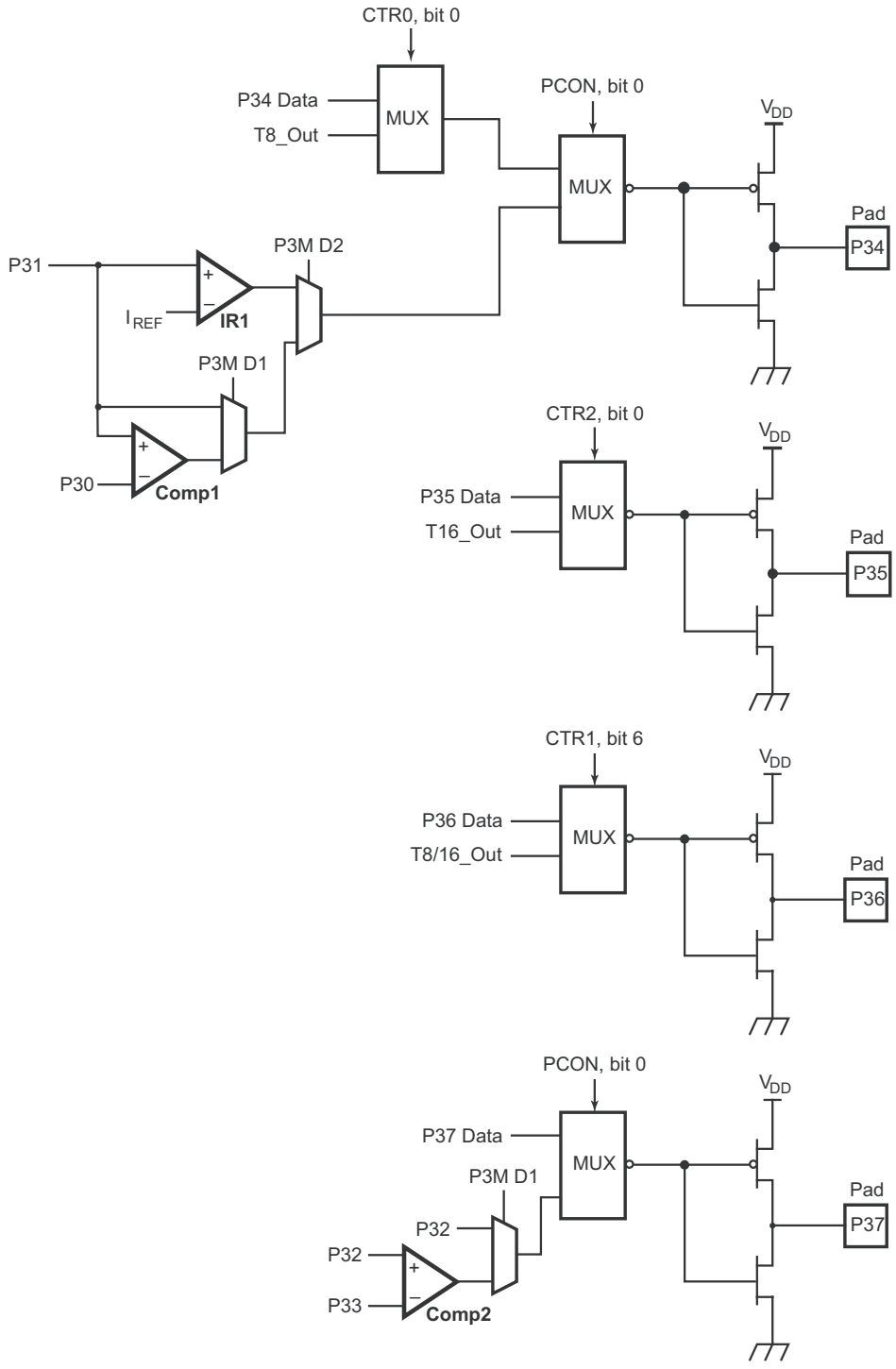

Figure 7. Port 3 Counter/Timer Output Configuration

Comparator Inputs

In ANALOG mode, P31 and P32 have a comparator front end. The comparator reference is supplied by P33 and P_{REF1}. In this mode, the P33 internal data latch and its corresponding IRQ1 are diverted to the Stop Mode Recovery sources (excluding P31, P32, and P33) as displayed in Figure 6 on page 15. In DIGITAL mode, P33 is used as bit 3 of the Port 3 input register, which then generates IRQ1.

Note: *Comparators are powered down by entering STOP mode. For P30:P33 to be used as a Stop Mode Recovery source, these inputs must be placed into DIGITAL mode.*

Comparator Outputs

The comparators can be programmed to be output on P34 and P37 by setting bit 0 of the PCON Register.

Port Configuration Register (PCON)

The Port Configuration (PCON) register (Table 9), configures the Port 0 output mode and the comparator output on Port 3. The PCON register is located in expanded register Bank F, address 00h.

Table 9. Port Configuration Register (PCON)

Bit	7	6	5	4	3	2	1	0
Field	Reserved					Port 0 Output Mode	Reserved	Comp./IR Amp. Output Port 3
Reset	X	X	X	X	X	1	X	0
R/W	—					W	—	W
Address	Bank F: 00h; Linear: F00h							

Bit Position	Value	Description
[7:3]	—	Reserved—Writes have no effect; reads 11111b.
[2]		Port 0 Output Mode—Controls the output mode of port 0. Write only; reads return 1.
	0	Open-drain
	1	Push/pull
[1]	—	Reserved—Writes have no effect; reads 1.
[0]		Comparator or IR Amplifier Output Port 3—Select digital outputs or comparator and IR amplifier outputs on P34 and P37. Write only; reads return 1.
	0	P34 and P37 outputs are digital.
	1	P34 is Comparator 1 or IR Amplifier output, P37 is Comparator 2 output.