Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

ZPA2326-0311A-R

Barometric Pressure Sensor
ZPA Series

Features

- **Very low current consumption**
- **Very stable in temperature drift**
- **Very low noise**
- **Small size SMD package**
  (L2.3 x W2.6 x H0.875 mm)

Applications

- **Mobile/Wearable device**
- **Weather forecasting**
- **Indoor navigation**
- **Z-axis detection**
- **Falling Detection**

Overview

Our product is capacitive type MEMS pressure sensor. It consists of a MEMS element, a Capacitor-to-Digital Converter (CDC) and a digital block with the digital correction, calibration non-volatile memory bits, FIFO, SPI and I2C interfaces. A pressure value can be acquired by the product calculating using two kinds of capacitance value, Csense and Cref, outputted from the MEMS element.

It can offer low current consumption, low drift for temperature change and low noise performance. Implementing full calibration function is included in ASIC. So it is very easy to use.

TABLE OF CONTENT

2. Specifications

2.1 Mechanical and electrical characteristics

Table 1. Characteristics list (At the time of Shipment)

Parameter		Condition	Min.	Typ.	Max.	Units
Package size	Area			2.3x2.6		mm
	Height				0.95	mm
Temperature range	Operating		-40		+85	degC
	Full accuracy		-10		+65	degC
Supply voltage (*1)		VDD	1.71	1.8	2.0	V
Negative supply voltage		VSS	0.0		0.0	V
Interface			SPI / I2C			
SPI frequency					1	MHz
I2C frequency					400	kHz
FIFO depth					24x16	Bits
Operation range			300		1100	hPa
Pressure resolution				1/64		Pa
Relative accuracy		T=+25degC, P range= 800 to1100hPa ΔP=100hPa		+/-0.1		hPa
Absolute accuracy		T= -10 to 65degC, P range= 800 to1100hPa		+/-0.8		hPa
Temperature drift coefficient		T= +10 to 65degC, P= 1000hPa Absolute value		0.8		Pa/degC
ODR			One-shot	11	23	S/s
Capacitance conversion time (*2)			41.5	83	166	ms
Current consumption (*3)		Device disabled		0.4		μA
		Device enabled. No measurements running.		19.5		μA
		Conversion time=1s		31.7		μA
		Conversion time=1/6s		6.3		μA
		Conversion time=1/12s		3.8		μA
Pressure RMS noise (*4)		Conversion time=1s		0.5		Pa_{rms}
		Conversion time=1/6s		1.1		Pa_{rms}
		Conversion time=1/12s		2.1		Pa_{rms}
Power-Up time		Waiting time from ENABLE bit set to '1' to next SPI/I2C access.			1	ms
Solder drifts				-0.5		hPa
Temperature resolution (*5)				0.1		degC
Temperature conversion time			3.4	3.5	3.6	ms
Temperature absolute accuracy		T= -10 to 10degC	-4		+4	degC
		T= 10 to 65degC	-2.5		+2.5	degC
Temperature noise (*6)		T= -10 to 65degC		0.05		$degC_{rms}$

Note:

*1. The rise time for this supply must be much more than 10µs.

*2. Typical conversion time corresponds to an ODR of 11S/s, minimum conversion time corresponds to an ODR of 23S/s; and maximum conversion time corresponds to an ODR whether 5S/s and 1S/s. The output when selecting ODR=1S/s is built by averaging of 5 samples measured at 5S/s.

*3. With One-shot mode (ODR=1S/s) at 1 sample/sec, T=25±2degC.

*4. For P= 1000hPa. The RMS noise is related to the CSENSE measurement.

*5. The measured temperature follows the equation : $Temp$[degC] = $Temp_{code}$ • 0.00649 – 176.83 where $Temp_{code}$ is the digital 16b code which can be read from the registers TEMP_OUT_H and TEMP_OUT_L.

*6. The outputted temperature by temperature sensor is product internal value.

2.2 Absolute maximum ratings

Table 2. Absolute maximum rating

Parameter	Condition	Min.	Max.	Units
Storage temperature		-40	+95	degC
Supply voltage	VDD	-0.3	+3.6	V
Input/output pin voltage		-0.3	VDD+0.3	V
ESD rating	HBM	-2	+2	kV
Overpressure			10,000	hPa

Note:

1. All voltage values are based on GND potential.
2. Do not use the sensor of deviating from the above mentioned ratings.

2.3 DC/AC characteristics for inputs and outputs

Digital inputs

Table 3. CMOS digital input with Schmitt-trigger (CS, SCLK/SCL, SDIN/SDA)

Parameter	Symbol	Condition	Min.	Max.	Units
High level input voltage	V_IH		0.7*VDD		V
Low level input voltage	V_IL			0.3*VDD	V
Negative-going threshold	VT_N	VDD=2.0V	0.63	0.975	V
Positive-going threshold	VT_P	VDD=2.0V	1.132	1.323	V
Input leakage current	I_LEAK	Low level input voltage=0.0V	-1	+1	µA

Digital outputs

Table 4. CMOS digital output (INT, SDIN/SDA)

Parameter	Symbol	Condition	Min.	Max.	Units
High level output voltage	V_OH		VDD-0.5		V
Low level output voltage	V_OL			VSS+0.4	V
Output drive strength	I_OH	VDD=2.0V and min V_OH at pin		4	mA
Output drive strength	I_OL	VDD=2.0V and max V_OL at pin		4	mA
Pull-up resistor	Rpup	For SDIN/SDA	(2)	(1)	
Rise time	Tr	(1)Standard-mode. For SDIN/SDA;(3)		1000	ns
		(1)Fast-mode. For SDIN/SDA;(3)	20	300	
Capacitance load	CL	(1)For SDIN/SDA, includes 10pF from the internal PAD		400	pF

Table 5. CMOS digital output tri-state(SDOUT/SA0)

Parameter	Symbol	Condition	Min.	Max.	Units
High level output voltage	V_OH		VDD-0.5		V
Low level output voltage	V_OL			VSS+0.4	V
Output drive strength	I_OH	VDD=2.0V and min V_OH at pin		4	mA
Output drive strength	I_OL	VDD=2.0V and max V_OL at pin		4	mA
Tri-state leakage current	I_OZ	To VSS	-0.4	0.4	µA

Note:

1. The maximum value of the pull-up resistor is defined by the following equation:

$$\mathrm{Rp}_{\max} = \frac{MAX(Tr)}{0.8473 * CL}$$

2. The minimum value of the pull-up resistor is defined as (VDD*pull-up* is the voltage connected to the pull-up resistor):

$$Rp_{min} = \frac{VDD_{pull-up} - V\_OL}{I\_OL}$$

3. For a selected Rp, which must to be Rp*min*<Rp<Rp*max*, the obtained rise time is:

$$Tr = 0.8473 * CL * Rp$$

3. Measurement direction

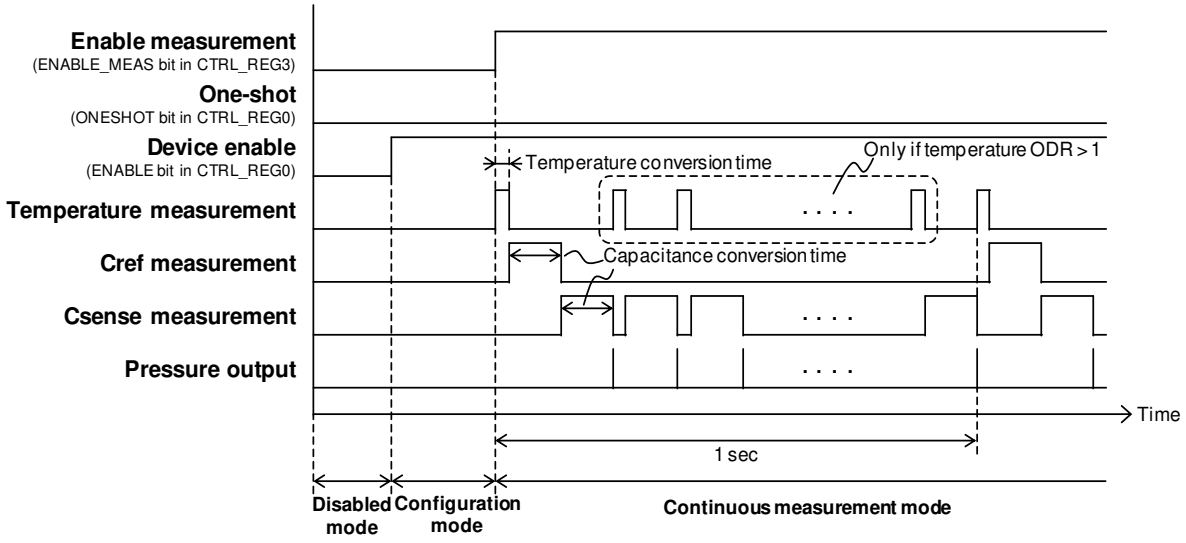
3.1 Technical description

Our product has the following four kinds of operating mode.

- **DISABLED MODE**: the product is completely disabled. Communication via SPI/I2C interface is allowed to enable the product or start an ONE-SHOT MODE..
- **CONFIGURATION MODE**: after enabling the product all register are accessible, and measurement configuration can be changed. Capacitance and temperature measurement s are not being run in this mode.
- **CONTINUOUS MEASUREMENT MODE**: after enabling this mode the temperature and capacitance measurement are running at their selected output data rate. Measurements are stopped by disabling this mode.
- **ONE-SHOT MODE**: this mode starts from the disabled mode, made a temperature and capacitance measurement and returns automatically to disabled mode. The measurement configuration can be change by entering into the configuration mode before starting the one-shot.

The following diagram describes our product operation when the continuous measurement is enabled after enabling the product.

Figure 1. Timing diagram for selecting continuous measurement mode

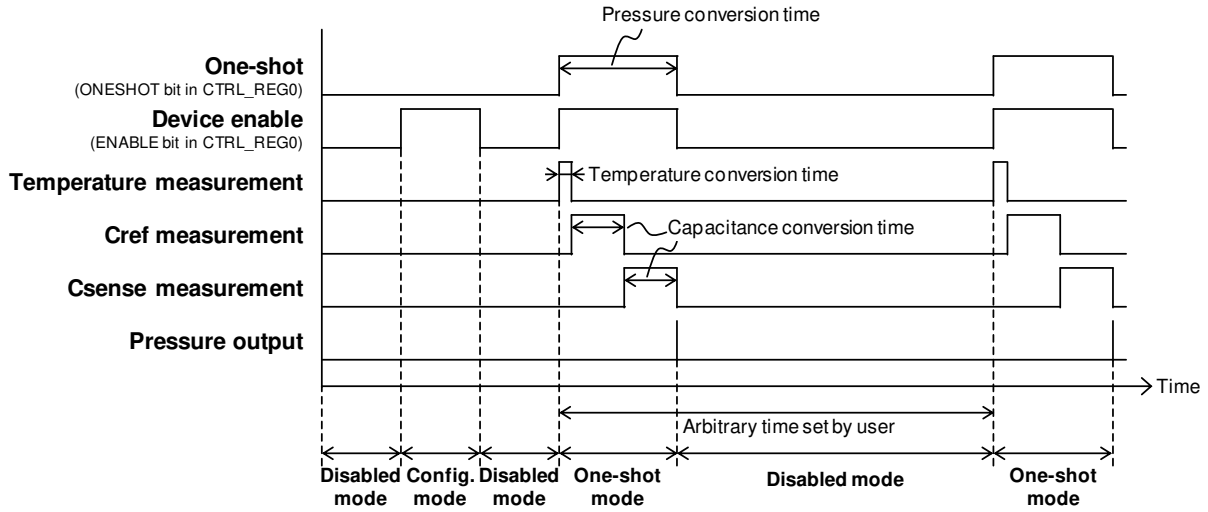


Note:

1. Pressure is calculated from sensing capacitance (Csense) and reference capacitance (Cref).
2. In the case of ODR="x" Hz, Csense is measured with a period of "1/(x+1)" sec.
3. Instead of measuring Csense, Cref is measured once every "x+1" times.
4. Pressure data is stored in output registers only after measuring Csense. With One-shot mode at 1 sample/sec

Operation when one-shot operation is selected:

Figure 2. Timing diagram for selecting one-shot mode

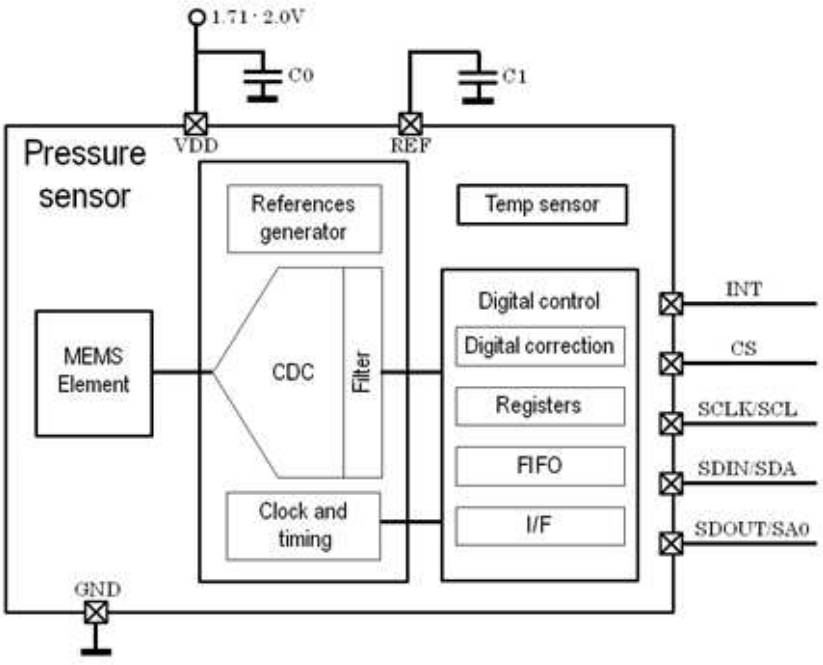


Note:

1. Pressure is calculated from Csense and Cref as with continuous measurement mode.
2. Csense and Cref are measured only one time per pressure measurement.
3. User can arbitrarily set time interval between pressure measurements.

3.2 Typical application circuit

Figure 3. Typical application circuit



3.3 Connecting components information

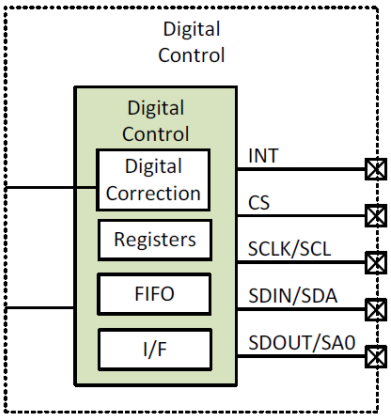
Table 6. Connecting components list

Parameter	Symbol	Min.	Max.	Unit	Note
Supply decoupling capacitance	C0	100		nF	For noise elimination purpose to VDD. C0 should better be mounted as closely as possible to the Sensor. Recommended part number is GRM033R61A104ME84 (MURATA) or similar one.
Reference decoupling capacitance	C1	100		nF	For noise elimination purpose to REF. C1 should better be mounted as closely as possible to the Sensor. Recommended part number is GRM033R61A104ME84 (MURATA) or similar one.

3.4 Digital interfaces

The following figure shows the block diagram of the digital logic, which includes the digital correction, the register map, FIFO and digital interface.

Figure 4. Digital control block diagram



The registers embedded in our product may be accessed through both I2C and SPI serial interfaces. The serial interfaces are mapped onto the same pads. To select the I2C interface, CS line must be tied high (i.e. connected to DVDD). In I2C mode, the SDOUT pin is reconfigured as the LSB of the device address word.

3.5 I2C interface

Our product I2C is a bus slave. The I2C is employed to write data into registers whose content can also be read back. There are two signals associated with the I2C bus: the serial clock line (SCL) and the serial data line (SDA). The latter is a bi-directional line used for sending and receiving the data to/from the interface. Both lines have to be connected to VDD through external pull-up resistors. The I2C interface is compliant with fast mode (400 kHz) I2C standards. The following table shows the pins description for I2C interface:

Table 7. Pins description for I2C interface

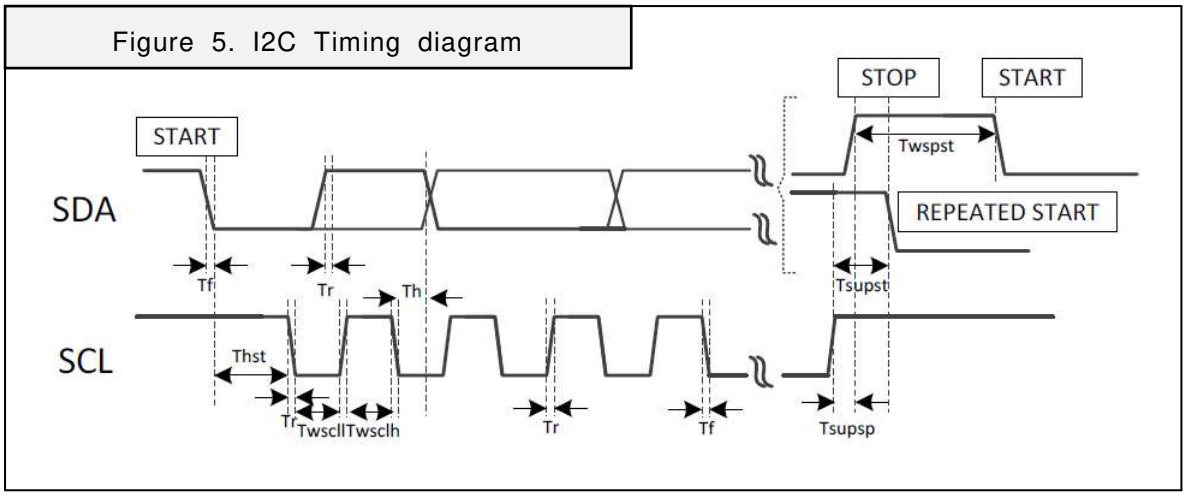
Pin name	Note
CS	Set to '1'
SCLK / SCL	I2C serial clock (SCL)
SDIN / SDA	I2C serial data
SDOUT / SA0	I2C less significant bit of the device address (SA0)

I2C slave timing values are described in the following table (the measurement points are done at 0.2·VDD and 0.8·VDD):

Table 8. I2C slave timing values

Parameter	Symbol	Units	Standard Mode		Fast Mode	
			Min.	Max.	Min.	Max.
SCL frequency	Fscl	kHz		100		400
SCL low time	Twscll	µs	4.7		1.3	
SCL high time	Twsclh		4.0		0.6	
SDA setup	Tsup	ns	250		100	
SDA hold time	Th	µs	0.01	3.45	0	0.9
SCL and SDA rise time	Tr	ns		1000		300
SCL and SDA fall time	Tr			300		300
Start condition hold time	Thst	µs	4		0.6	
Repeated start condition setup time	Tsupst		4.7		0.6	
Stop condition setup time	Tsupsp		4		0.6	
Bus free time between start-stop	Twspst		4.7		1.3	

Figure 5. I2C Timing diagram



3.6 I2C operation

The transaction on the bus is started through a START (ST) signal. A start condition is defined as a HIGH to LOW transition on the data line while the SCL line is held HIGH. After this has been transmitted by the master, the bus is considered busy.

The next byte of data transmitted after the start condition contains the address of the slave in the first 7 MSBs and the eighth bit (LSB) tells whether the master is receiving data from the slave or transmitting data to the slave.

When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the master. The slave address (SAD) associated to The device is 101110xb. The SDO/SA0 pad can be used to modify the less significant bit of the device address. If the SA0 pad is connected to voltage supply, LSB is ‘1’ (address 1011101b), otherwise if the SA0 pad is connected to ground, the LSB value is ‘0’ (address 1011100b). This solution permits to connect and address two different product to the same I2C lines.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line LOW so that it remains stable low during the HIGH period of the acknowledge clock pulse. A receiver which has been addressed is obliged to generate an acknowledge after each byte of data received.

The I2C embedded in The device behaves like a slave device and the following protocol must be adhered to. After the start condition (ST) a slave address is sent, once a slave acknowledge (SAK) has been returned, a 8-bit sub-address (SUB) will be transmitted: the 7 LSB represents the actual register address while the MSB enables address auto increment. If the MSB of the SUB field is ‘1’, the SUB (register address) will be automatically increased to allow multiple data read/write.

The slave address is completed with a Read/Write bit. If the bit was '1' (Read), a repeated START (SR) condition must be issued after the two sub-address bytes; if the bit is '0' (Write) the master will transmit to the slave with direction unchanged. The following table explains how the SAD+read/write bit pattern is composed, listing all the possible configurations.

SAD+Read/Write patterns

Command	SAD[6:1]	SAD[0] = SA0	R/W	SAD+R/W
Read	101110	0	1	1011 1001 (B9h)
Write	101110	0	0	1011 1000 (B8h)
Read	101110	1	1	1011 1011 (BBh)
Write	101110	1	0	1011 1010 (BAh)

Transfer when master is writing one byte to slave

Master	ST	SAD+W		SUB		DATA		SP
Slave			SAK		SAK		SAK	

Transfer when master is writing multiple bytes to slave

Master	ST	SAD+W		SUB		DATA		DATA		SP
Slave			SAK		SAK		SAK		SAK	

Transfer when master is receiving (reading) one byte of data from slave

Master	ST	SAD+W		SUB		SR	SAD+R			NMAK	SP
Slave			SAK		SAK			SAK	DATA		

Transfer when master is receiving (reading) multiple bytes of data from slave

Master	ST	SAD+W		SUB		SR	SAD+R			MAK		NMAK	SP
Slave			SAK		SAK			SAK	DATA		DATA		

Data are transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes transferred per transfer is unlimited. Data is transferred with the most significant bit (MSB) first. If a receiver can't receive another complete byte data until it has performed some other functions, it can hold the clock line, SCL LOW to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases the data line. If a slave receiver does not acknowledge the slave address (i.e. it is not able to receive because it is performing some real time function) the data line must be kept HIGH by the slave. The master can then abort the transfer. A LOW to HIGH transition on the SDA line while the SCL line is HIGH is defined as a STOP condition. Each data transfer must be terminated by the generation of a STOP (SP) condition.

In order to read multiple bytes incrementing the register address, it is necessary to assert the most significant bit of the subaddress field. In other words, SUB(7) must be equal to 1 while SUB(6-0) represents the address of the first register to be read. In the presented communication format MAK is Master acknowledge and NMAK is no master acknowledge.

3.7 SPI interface

The following table shows the pins description for 4-wires SPI interface:

Table 9. Pins description for 4-wires SPI interface

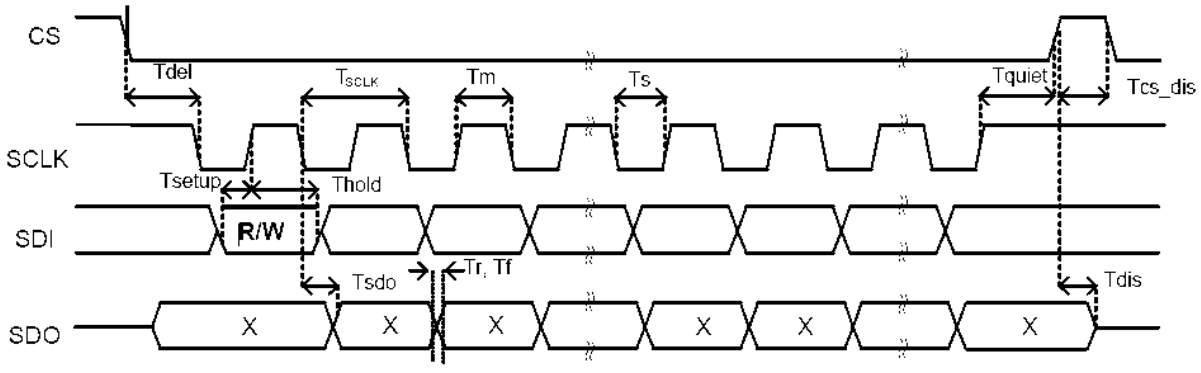
Pin name	Note
CS	0: SPI enabled
SCLK / SCL	SPI serial port clock (SCLK)
SDIN / SDA	SPI serial data input
SDOUT / SA0	SPI serial data output

SPI slave timing values are described in the following table (the measurement points are done at 0.2·VDD and 0.8·VDD):

Table 10.SPI slave timing values

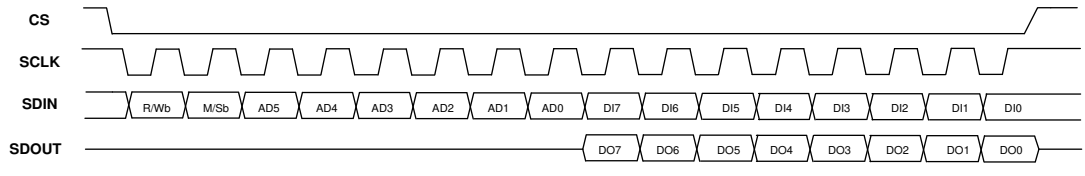
Parameter	Symbol	Units	Min.	Max.
SPI clock frequency	Fsclk	MHz		1
1/(SPI clock frequency)	Tsclk	ns	1000	
CS falling edge to SCLK falling edge	Tdel		25	
SCLK rising edge to CS rising edge	Tquiet		25	
CS rising edge to SDO disabled	Tdis			25
CS deassertion between SPI communications	Tcs_dis		1000	
SCLK low pulse width	Ts		0.3* Tsclk	
SCLK high pulse width	Tm		0.3* Tsclk	
SDI valid before SCLK rising edge	Tsetup		25	
SDI valid after SCLK rising edge	Thold		50	
SCLK falling edge to SDO output transition	Tsdo			50
SDO output low to output high transition	Tr			25
SDO output high to output low transition	Tf			25

Figure 6. SPI Timing diagram



The device SPI is a bus slave. The SPI allows to write and read the registers of the device. The serial interface interacts with the outside world with 4 wires: CS, SCLK, SDIN and SDOUT.

Figure 7 .Read and write protocol



CS is the serial port enable and it is controlled by the SPI master. It goes low at the start of the transmission and returns to high at the end. **SCLK** is the serial port clock and it is controlled by the SPI master. It is stopped high when **CS** is high (no transmission). **SDIN** and **SDOUT** are respectively the serial port data input and output. Those lines are driven at the falling edge of **SCLK** and should be captured at the rising edge of **SCLK**.

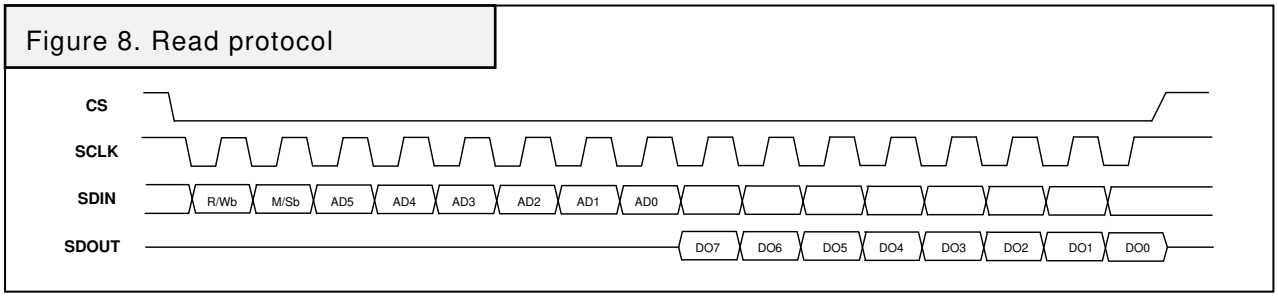
Both the read register and write register commands are completed in 16 clock pulses or in multiples of 8 in the case of multiple bytes read/write. Bit duration is the time between two falling edges of **SCLK**. The first bit (bit 0) starts at the first falling edge of **SCLK** after the falling edge of **CS** while the last bit (bit 15, bit 23, ...) starts at the last falling edge of **SCLK** just before the rising edge of **CS**.

bit 0: RW bit. When 0, the data DI(7:0) is written into the device. When 1, the data DO(7:0) from the device is read. In the latter case, the chip will drive **SDOUT** at the start of bit 8.
bit 1: MS bit. When 0, the address will remain unchanged in multiple read/write commands.
When 1, the address will be auto incremented in multiple read/write commands.
bit 2-7: address AD(5:0). This is the address field of the indexed register.
bit 8-15: data DI(7:0) (write mode). This is the data that is written into the device (MSb first).
bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

In multiple read/write commands further blocks of 8 clock periods are added. When the MS bit is 0 the address used to read/write data remains the same for every block. When MS bit is 1 the address used to read/write data is increased at every block. The function and the behavior of **SDIN** and **SDOUT** remain unchanged.

3.8 SPI read

Figure 8. Read protocol



The SPI Read command is performed with 16 clock pulses. The multiple byte read command is performed adding blocks of 8 clock pulses at the previous one.

bit 0: READ bit. The value is 1.

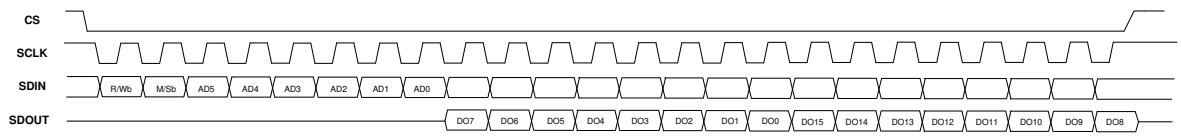
bit 1: MS bit. When 0 do not increment address, when 1 increment address in multiple readings.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

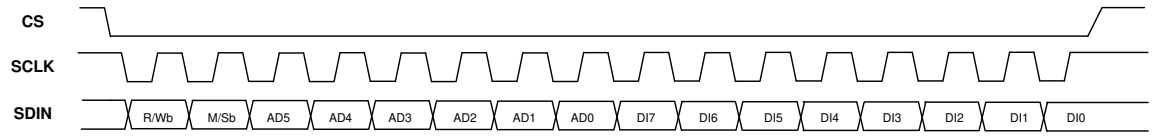
bit 16-... : data DO(...-8). Further data in multiple byte readings.

Figure 9. Multiple bytes SPI read protocol (2 bytes example)



3.9 SPI write

Figure 10. Write protocol



The SPI Write command is performed with 16 clock pulses. The multiple byte write command is performed adding blocks of 8 clock pulses at the previous one.

bit 0: WRITE bit. The value is 0.

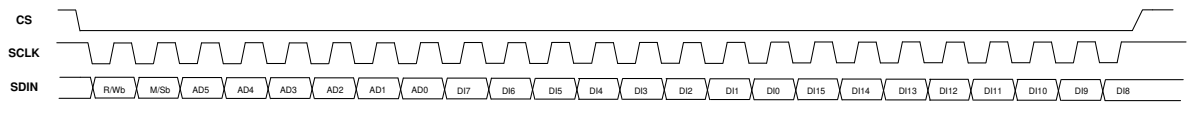
bit 1: MS bit. When 0 do not increment the address, when 1 increment the address in multiple writings.

bit 2 -7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that is written in the device (MSb first).

bit 16-... : data DI(...-8). Further data in multiple byte writings.

Figure 11. Multiple bytes SPI write protocol (2 bytes example)



3.10 SPI read in 3-wires mode

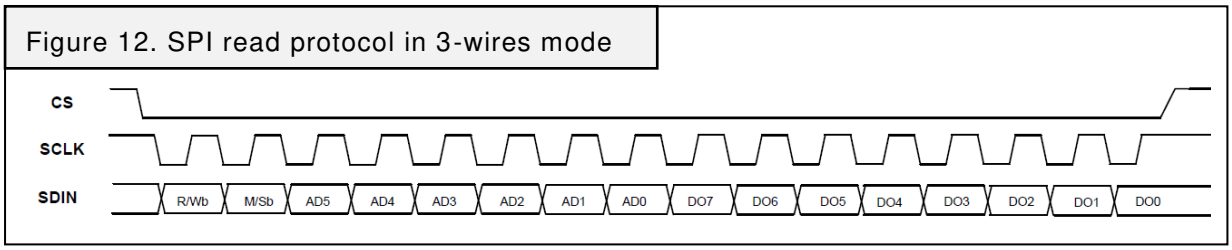
The following table shows the pins description for 3-wires SPI interface:

Table 11. Pins description for 3-wires SPI interface

Pin name	Note
CS	0: SPI enabled
SCLK / SCL	SPI serial port clock (SCLK)
SDIN / SDA	SPI serial data input / output. Pull-up resistor needed

A 3-wires mode is entered by setting to '1' bit SIM (SPI serial interface mode selection) in CTRL_REG3. The SDIN/SDA pin needs to be connected to an external pull-up resistor, as described in 3.3.2.

Figure 12. SPI read protocol in 3-wires mode



The SPI read command is performed with 16 clock pulses:

bit 0: READ bit. The value is 1.

bit 1: MS bit. When 0, do not increment the address, when 1, increment the address in multiple readings.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSB first).

Multiple read command is also available in 3-wires mode.

3.11 FIFO operation

The product contains a FIFO with 16 positions to store values of the pressure.

The FIFO operation is controlled by the STATUS_REG. When the FIFO is empty, the bit FIFO_EMPTY is set (high). When the FIFO is full, the bit FIFO_FULL is set (high). If a new pressure value arrives once the FIFO is FULL, P_OD overrun bit is set high.

The interrupts can be configured so that they activate when the FIFO is FULL or EMPTY.

When the FIFO is not empty, and a value is read from all data registers (PRESS_OUT_XL, PRESS_OUT_L and PRESS_OUT_H registers), this value is automatically deleted from the FIFO.

When the FIFO is full and a new pressure value needs to be written, the oldest value in the FIFO will be deleted to allow for the newest value to be written.

3.12 Interrupt operation

The interrupts can be enabled and disabled via a CTRL_REG1 register. (see CTRL_REG1 register information in page 22)
. Once an interrupt happens, the interrupt source can be read in INTERRUP_SOURCE. Reading the INTERRUPT_SOURCE register will automatically delete it and will reset the pin values to the disabled state.

3.13 Heading2

The device contains a set of registers which are used to control its behavior and to retrieve pressure and temperature data. The register address, made up of 7 bits, is used to identify them and to read/write the data through the serial interface.

Table 12. Register address map

Name	Type	Register address (HEX)	Register address (Binary)	Default	Function and comment
Reserved (do not modify)		00-07 0B-0E			Reserved
REF_P_XL	R/W	08	000 1000	0000 0000	
REF_P_L	R/W	09	000 1001	0000 0000	
REF_P_H	R/W	0A	000 1010	0000 0000	
DEVICE_ID	R	0F	000 1111	1011 10’SA0’1	Reserved
RES_CONF	R/W	10	001 0000	0000 0000	
Reserved (do not modify)		11-1F			Reserved
CTRL_REG0	R/W	20	010 0000	0000 0000	
CTRL_REG1	R/W	21	010 0001	0011 1111	
CTRL_REG2	R/W	22	010 0010	0000 0000	
CTRL_REG3	R/W	23	010 0011	0011 0000	Reserved
INT_SOURCE_REG	R	24	010 0100	0000 0000	Interrupt status
THS_P_LOW_REG	R/W	25	010 0101	0000 0000	Thresholds interrupt
THS_P_HIGH_REG	R/W	26	010 0110	1111 1111	Thresholds interrupt
STATUS_REG	R	27	010 0111	0000 0000	
PRESS_OUT_XL	R	28	010 1000	Output	Pressure value XL
PRESS_OUT_L	R	29	010 1001	Output	Pressure value L
PRESS_OUT_H	R	2A	010 1010	Output	Pressure value H
TEMP_OUT_L	R	2B	010 1011	Output	Temperature value L
TEMP_OUT_H	R	2C	010 1100	Output	Temperature value H
Reserved (Do not modify)		2D-4B			Reserved

Registers marked as “Reserved” must not be changed. The writing to those registers may cause permanent damages to the device. The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered-up.

3.14 Register description

REF_P_XL

7	6	5	4	3	2	1	0
REFL7	REFL6	REFL5	REFL4	REFL3	REFL2	REFL1	REFL0

This reference pressure register contains the lower part of the reference pressure that is subtracted to the sensor output pressure. The full value is REF_P_XL & REF_P_H & REF_P_L and is represented as 2’s complement.

REF_P_L

7	6	5	4	3	2	1	0
REFL15	REFL14	REFL13	REFL12	REFL11	REFL10	REFL9	REFL8

This reference pressure register contains the middle part of the reference pressure that is subtracted to the sensor output pressure. The full value is REF_P_XL & REF_P_H & REF_P_L and is represented as 2’s complement.

REF_P_H

This reference pressure register contains the higher part of the reference pressure that is subtracted to the sensor output pressure. The full value is REF_P_XL & REF_P_H & REF_P_L and is represented as 2’s complement.

7	6	5	4	3	2	1	0
REFL23	REFL22	REFL21	REFL20	REFL19	REFL18	REFL17	REFL16

RES_CONF

This register configures the resolution of the pressure and temperature measurements.

7	6	5	4	3	2	1	0
	AVGT2	AVGT1	AVGT0	AVGP3	AVGP2	AVGP1	AVGP0

AVGP3-AVGP0 configure the number of averages of the pressure measurements. AVGT2-AVGT0 configure the number of averages of the temperature measurements. The pressure or temperature meassurement final data rate is the selected ODR2-0 (CTRL_REG3) divided by the selected number of averages (AVGP3-AVGP0). The default setting of this register is 0 after powering up the device. The current consumption does not change by changing the number of internal averages.

Bits can be configured as described in the following tables.

Table 13. Internal averages of pressure measurements

AVGP3	AVGP2	AVGP1	AVGP0	Nr. Internal averages
0	0	0	0	1
0	0	0	1	2
0	0	1	0	4
0	0	1	1	8
0	1	0	0	16
0	1	0	1	32

AVGT2-AVGT0 bits can be configured as described in the following table.

Table 14. Internal averages of temperature measurements

AVGT2	AVGT1	AVGT0	Nr. Internal averages
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16

DEVICE_ID

This register contains the device identifier number. For our product the device number is set to 0xBB.

7	6	5	4	3	2	1	0
1	0	1	1	1	0	SA0	1

CTRL_REG0

This register controls the functionality of several blocks.

7	6	5	4	3	2	1	0
						ENABLE	ONE-SHOT

Bit 1: ENABLE is the chip enable of the device. When the device is enabled, we can read and write the complete register map via the SPI/I2C. The device should also be enabled for normal operating mode. The device will be disabled when ENABLE = '0' (default value after boot) and enabled when ENABLE is set to '1'. Between enabling the device and the next SPI/I2C access there should be a time of Tpup.

Bit 0: ONE_SHOT bit is used to start a new conversion. In this situation a single acquisition of temperature and pressure is started when ONE_SHOT bit is set to '1'. At the end of conversion the new data are available in the output registers, the ONE_SHOT bit is automatically reset to '0'.

The precission of the ONE-SHOT pressure measurement can be configured with the ODR2-0 bits in CTRL_REG3 which are used to set the CDC oversampling ratio and therefore the pressure measurement conversion time. The ODR2-0 bits selects the number of clock cycles required to produce a conversion result. The device is automatically powered-down after the conversion ends. The avegared current consumption depends on the length of the conversion. The temperature is meassured only one time per presure measurement. Internal averaging is not applicable in one-shot mode.

Table 15. Pressure measurement conversion time

ODR2	ODR1	ODR0	Pressure Conversion time(s)
0	0	0	Reserved
0	0	1	1
0	1	0	1/3
0	1	1	1/6
1	0	0	1/12
1	0	1	1/3
1	1	0	1/6
1	1	1	1/12

The pressure or temperature meassurement final data rate is the selected ODR2-0 (CTRL_REG3) divided by the selected number of averages (AVGP3-AVGP0).

CTRL_REG1

This register controls the functionality of several blocks.

7	6	5	4	3	2	1	0
		Mask_shortcut	Mask_fifo_e	Mask_fifo_f	Mask_data_ready	Mask_dpl_event	Mask_dph_event

Bit 5: when set to '1' masks the shortcut event to produce an interrupt. Default value is '1'.

Bit 4: when set to '1' masks the FIFO empty event to produce an interrupt. Default value is '1'.

Bit 3: when set to '1' masks the FIFO full event to produce an interrupt. Default value is '1'.

Bit 2: when set to '1' masks the DATA READY event to produce an interrupt. Default value is '1'.

Bit 1: when set to '1' masks the pressure low event to produce an interrupt. Default value is '1'.

Bit 0: when set to '1' masks the pressure high event to produce an interrupt. Default value is '1'.

The device features one fully-programmable interrupt sources (INT) which may be configured to trigger different pressure events.

CTRL_REG2

This register controls the functionality of several blocks.

7	6	5	4	3	2	1	0
Tri-state	INT_H_L	PP_OD			SWRESET	AUTOZERO	

Bit 7: when set to '1', the interrupt (INT) pin is set in high impedance mode. Default value is '0'

Bit 6: INT_H_L: Interrupt active high, low. Default value: 0. (0: active high; 1: active low)

Bit 5: PP_OD: Push-pull/open drain selection on interrupt pads. Default value: 0. (0: push-pull; 1: open drain)

Bit 2: SWRESET is the software reset bit. The device is reset to the power on configuration if the SWRESET bit is set to '1'.

Bit 1: AUTO_ZERO, when set to '1', the latest pressure written in the the PRESS_OUT_H & PRESS_OUT_L & PRESS _OUT_XL register is copied in the REF_P_H & REF_P_L & REF_P_XL and kept as reference. In the next preassure measurement PRESS_OUT_H & PRESS_OUT_L & PRESS _OUT_XL is the difference between this reference and the pressure sensor value. At the end of the autozeroing process, the AUTO_ZERO bit comes back to '0'.

The reference pressure can be modified by the user by writing in the registers REF_P_H & REF_P_L & REF_P_XL.

CTRL_REG3

This register controls the functionality of several blocks.

7	6	5	4	3	2	1	0
ENABLE_MEAS	ODR2	ODR1	ODR0				SIM

Bit 7: ENABLE_MEAS, when set to '1' activates the pressure and temperature measurements. The device should be enabled (via ENABLE in CTRL_REG0) for measurements to start.

Bit 6 to Bit 4: ODR2- ODR1 - ODR0 bits allow to change the output data rates of pressure and temperature samples. ODR2, ODR1 and ODR0 bits can be configured as described in the following table.

Table 16. Temperature measurement conversion time

ODR2	ODR1	ODR0	Pressure data rate	Temperature output data rate
0	0	0	Reserved	Reserved
0	0	1	1 S/s	1 S/s
0	1	0	5 S/s	1 S/s
0	1	1	11 S/s	1 S/s
1	0	0	23 S/s	1 S/s
1	0	1	5 S/s	5 S/s
1	1	0	11 S/s	11 S/s
1	1	1	23 S/s	23 S/s

Bit 0: SIM bit selects the SPI serial interface mode. When SIM is '0' (default value) the 4-wire interface mode is selected and data coming from the device are sent to pin #7 SDOUT. In 3-wire interface mode, output data are sent to pin SDIN/SDOUT.

INT_SOURCE

This register informs on the status of the interrupts.

7	6	5	4	3	2	1	0
IA		SHORTCUT	FIFOE	FIFOF	DATA_READY	PL	PH

INT_SOURCE register is cleared by reading INT_SOURCE register. The INT1(2) pins are also cleared.

Bit 7: IA: Interrupt Active.(0: no interrupt has been generated; 1: one or more interrupt events have been generated).

Bit 5: SHORTCUT: when set to 1 indicates if a shortcut between the sensor terminals has occured during the last measurement.

Bit 4: FIFOE: FIFO empty interrupt bit. (0: FIFO is not empty; 1: FIFO is empty).

Bit 3: FIFOF: FIFO full interrupt bit. (0: FIFO is not full; 1: FIFO is full).

Bit 2: DATA_READY event: one pressure measurement is completed and available in the FIFO.

Bit 1: PL: Differential pressure Low. (0: no interrupt has been generated; 1: Low differential pressure event has occurred, the digital word of the bits [23:16] of the pressure measurement are smaller than the bits of the THS_P_L register.)

Bit 0: PH: Differential pressure High. (0: no interrupt has been generated; 1: High differential pressure event has occurred the digital word of bits [23:16] of the pressure measurement are bigger than the bits of the THS_P_H register.)

THS_P_L

This register is the pressure threshold for the interrut alerts. It corresponds to the 8 MBS's of the pressure measurements. The regiter format is 2's complement allowing negative pressure thresholds.

7	6	5	4	3	2	1	0
THS_P_L[7]	THS_P_L[6]	THS_P_L[5]	THS_P_L[4]	THS_P_L[3]	THS_P_L[2]	THS_P_L[1]	THS_P_L[0]

This register contains the low threshold to compare with the 8 MSB of the pressure register. The default value of this register is 0x00.

THS_P_H

This register is the pressure threshold for the interrut alerts. It corresponds to the 8 MBS's of the pressure measurements. The regiter format is 2's complement allowing negative pressure thresholds.

7	6	5	4	3	2	1	0
THS_P_H[7]	THS_P_H[6]	THS_P_H[5]	THS_P_H[4]	THS_P_H[3]	THS_P_H[2]	THS_P_H[1]	THS_P_H[0]

This register contains the high threshold to compare with the 8 MSB of the pressure register. The default value of this register is 0xFF.

STATUS_REG

This register provides information on the data availability and the FIFO status.

7	6	5	4	3	2	1	0
0	0	P_OR	T_OR	FIFO_F	FIFO_E	P_DA	T_DA

The content of this register is updated every ODR cycle, regardless of BDU value in CTRL_REG1.
P_DA is set to 1 whenever a new pressure sample is available. P_DA is cleared anytime PRESS_OUT_H register is read.

T_DA is set to 1 whenever a new temperature sample is available. T_DA is cleared anytime TEMP_OUT_H register is read.

FIFO_FULL is set to 1 whenever the FIFO is full.
FIFO_EMPTY is set to 1 whenever the FIFO is empty.

P_OR bit is set to '1' whenever new pressure data is available and FIFO FULL was set in the previous ODR cycle and not cleared. P_OR is cleared anytime PRESS_OUT_H register is read.

T_OR is set to '1' whenever new temperature data is available and T_DA was set in the previous ODR cycle and not cleared. T_OR is cleared anytime TEMP_OUT_H register is read.

PRESS_OUT_XL

This register provides information on the pressure measurements. This is the top position of the FIFO.

7	6	5	4	3	2	1	0
POUT7	POUT6	POUT5	POUT4	POUT3	POUT2	POUT1	POUT0

PRESS_OUT_L

This register provides information on the pressure measurements. This is the top position of the FIFO.

7	6	5	4	3	2	1	0
POUT15	POUT14	POUT13	POUT12	POUT11	POUT10	POUT9	POUT8

PRESS_OUT_H

This register provides information on the pressure measurements. This is the top position of the FIFO.

7	6	5	4	3	2	1	0
POUT23	POUT22	POUT21	POUT20	POUT19	POUT18	POUT17	POUT16

The 24 bits from the registers PRESS_OUT_H, PRESS_OUT_L and PRESS_OUT_XL provides the value of the pressure(in 2's complement format). The 18 MSBs correspond directly to a value in Pa. In other words the output value has an LSB of 1/64 Pa.

TEMP_OUT_L

This register provides information on the temperature measurements.

7	6	5	4	3	2	1	0
TOUT7	TOUT6	TOUT5	TOUT4	TOUT3	TOUT2	TOUT1	TOUT0

TEMP_OUT_H

This register provides information on the temperature measurements.

7	6	5	4	3	2	1	0
TOUT15	TOUT14	TOUT13	TOUT12	TOUT11	TOUT10	TOUT9	TOUT8

The 16 bits from the registers TEMP_OUT_H and TEMP_OUT_L provide the digital code of the temperature in unsigned format. Temperature information can be obtained by conversion formula in P7.