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Reference Design

Z8F2480 Power Monitor with eZ80F91 Webserver

RD002702-0814

Overview

This reference design integrates a Z8F2480-based AC power monitor with Zilog's eZ80F91 Webserver Module to showcase the capability of an optically-isolated Z8F2480 MCU-based power monitor to measure AC input voltage, AC load current, voltage/current phase shift, the power factor of the load, and to communicate via a standard Ethernet interface and webserver.

The Z8F2480 MCU and the eZ80F91 Webserver Module are connected for easy mounting. The load is powered via a single-phase AC line with voltage in the range of 90V to 240V RMS at 50Hz or 60Hz. The Z8F2480 MCU-based power board provides current to a power load and provides optically-isolated I^2C signals to communicate with the eZ80F91 Module.

This reference design can be used as a basis for developing systems that can control different power installations, including motors and lighting ballasts.

Note: The source code file associated with this reference design, RD0027-SC01.zip, is available free for download from the Zilog website. This source code has been tested with version 5.2.0 of ZDSII for Z8 Encore! XP MCUs. Subsequent releases of ZDSII may require you to modify the code supplied with this application note.

Features

This reference design features the following elements:

- 90–240V AC RMS input voltage range
- Load current up to 3amps
- Less than 5mA average current consumed from an AC line in either monitoring or standby modes
- 3750V isolation voltage between the AC line and the eZ80F91 MCU

Potential Applications

This reference design can be used to develop a number of applications; the brief list below offers two ideas.

- Remote-operated commercial or architectural lighting monitors
- Remote-operated AC motors or other devices

Discussion

This Z8F2480 Power Monitor/eZ80F91 Webserver reference design consists of a base power board with an eZ80F91 Module affixed to it, as shown in Figure 1; the Module is located on the bottom of the board, as shown in Figure 2. This base power board, hereafter referred to in this document as a Power Board, is a two-layer surface-mount platform that provides easy probe access points to all AC inputs and outputs, thereby allowing the user to quickly connect and measure electrical characteristics and waveforms.

The Power Board is powered from the same single-phase AC line with a 90-240V voltage range to which a load is connected; it is able to provide up to 3 A current to the load.

The dimensions of the Power Board are 3.1" (L) x 2.9" (W) x 0.7" (H) without the eZ80F91 Webserver Module attached. Figure 1 shows a top view of the Power Board, and Figure 2 shows the assembled Power Board/eZ80F91 Module combination.

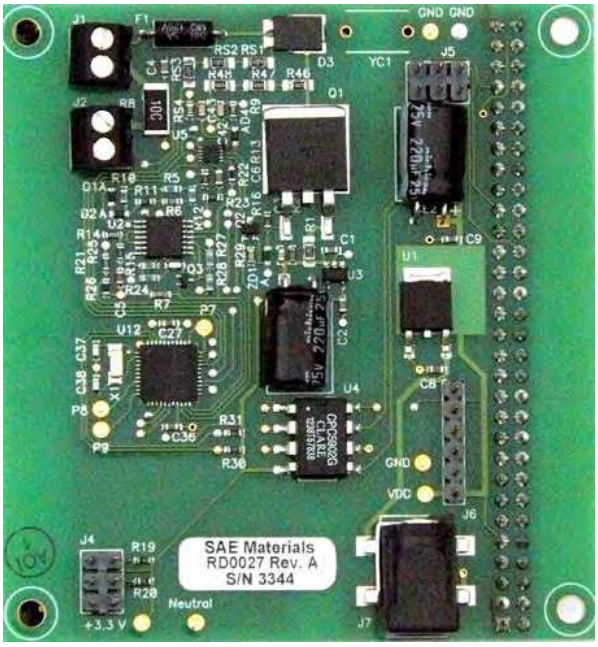

Figure 1. Base Power Board, Top View

Figure 2. eZ80F91 Module, Top View

To learn more about the eZ80F91 Module, refer to the eZ80Acclaim!/eZ80AcclaimPlus! Ethernet Modules Product Specification (PS0306).

A block diagram of the Power Board is shown in Figure 3.

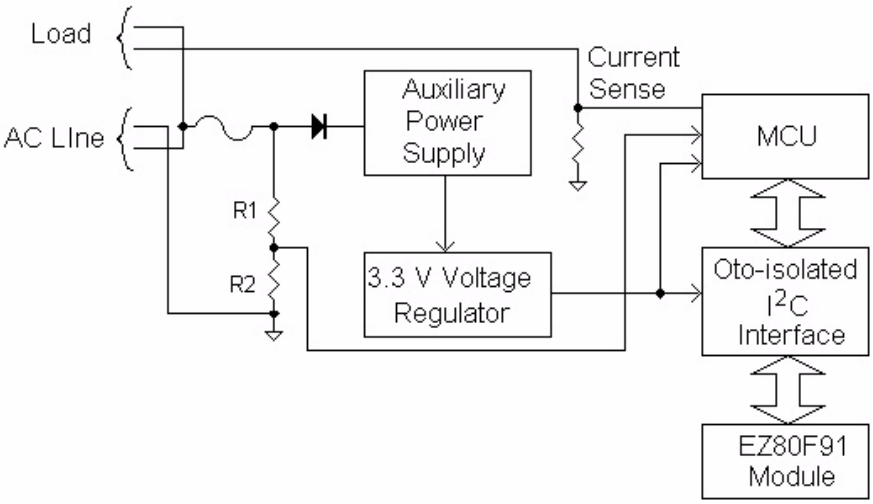

Figure 3. Block Diagram: A Z8F2480 Power Monitor and eZ80F91 Webserver with a Range Switch

Warning: The Power Board is electrically connected to AC power. It contains points with high voltage (up to 400 V). If any measurements will be performed on the Power Board, a power supply with an isolation transformer should be used to avoid electrical shock. Persons working with this Power Board should be fully qualified to work with high voltage devices.

Load current is not fuse-protected. It is up to the user to protect the AC line in the event of a short circuit caused by a load connected to the Power Board.

Z8F2480 Power Monitor

The Z8F2480 Power Monitor (i.e, the Power Board) contains an auxiliary power supply with a depletion-mode MOSFET (Q1; IXTA08N50D2), a Zener diode (ZD1), and resistors R1 and R2, which provide +5 V to drive a voltage regulator (U3). The 3.3 V output of U3 in turn drives the Z8F2480 MCU and the optically-isolated I^2C interface. A MOSFET (Q2), operated by the Z8F2480 MCU, is used to decrease power dissipation on Q1 by turning Q1 off when AC voltage is significantly above the voltage stored on capacitor CE1. For a visual representation of this circuit, see Appendix A. Schematic Diagrams on page 22.

Resistive dividers RS1–RS3/RS4 provide a signal to the Z8F2480 MCU for AC voltage measurements, while resistive dividers R46–R48/R9 furnish a signal to the MCU's internal comparator to synchronize the Q2 gate signal with the AC phase.

Current sense resistor R8 provides a signal for the MCU to determine a load current amplitude, as well as a current zero crossing point to determine the phase shift between the AC voltage and the load current.

Figure 4 shows the location of components on the Power Board.

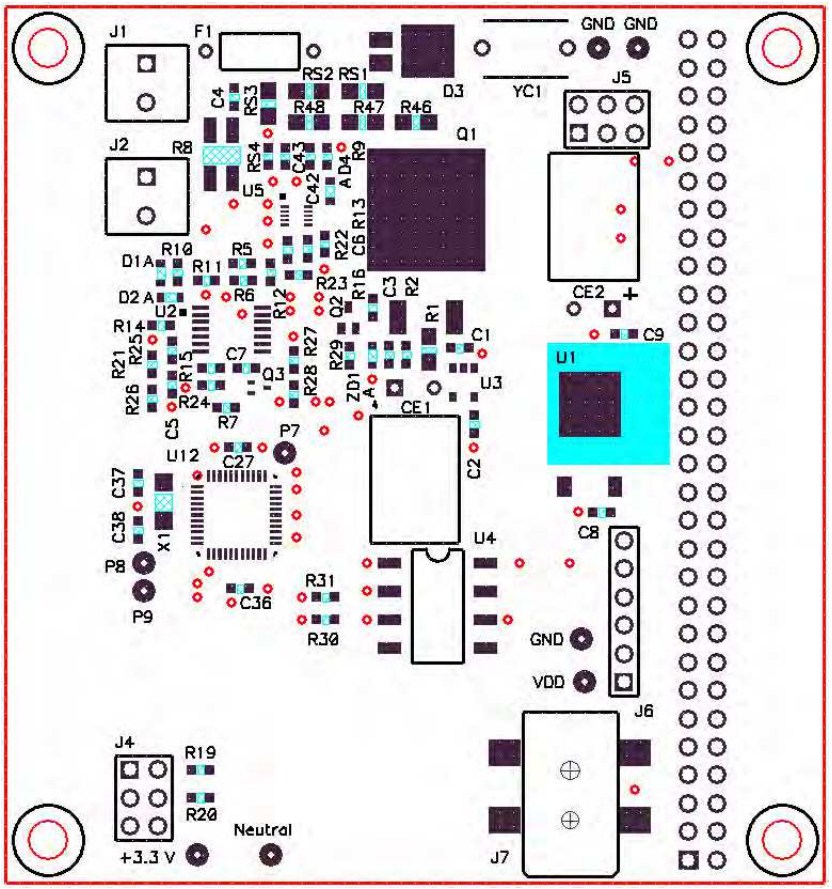

Figure 4. Location of Components on the Power Board

To minimize power dissipation on the current sense resistor, its resistance value is set very low, and a signal conditioner with a detector/amplifier (U2A–C) and a MOSFET (Q3) is used to increase the signal to an acceptable level for the MCU.

A comparator (U2D) is used to provide overvoltage/overcurrent information to the Z8F2480 MCU.

An optically-isolated I^2C interface (U4) creates a communication channel between the Power Board's Z8F2480 MCU and the eZ80F91 Webserver Module connected to J3.

A power jack (J7) is used to provide +5 V from a wall adapter to drive the eZ80F91 Module. This voltage is reduced to 3.3 V by a linear voltage regulator (U1) and is applied to the eZ80F91 Module through connector J3, to which the Module is mounted.

Debug connectors J4–J6 are for factory use only and may ship unassembled on the Power Board.

eZ80F91 Webserver Module

A top view of the eZ80F91 Module is shown in Figure 2 on page 2. To learn more about the eZ80F91 Module, refer to the eZ80Acclaim!/eZ80AcclaimPlus! Ethernet Modules Product Specification (PS0306).

Principles of Operation

After main power is applied to the Power Board, the auxiliary power supply on the eZ80F91 Module becomes active and the voltage on capacitor CE1 rises. After the voltage on capacitor CE1 reaches 5 V, the linear voltage regulator (U3) becomes active and supplies 3.3 V to the Z8F2480 MCU (U12) to initiate a Power-On Reset (POR) cycle of the MCU.

After the POR cycle completes, the Z8F2480 firmware configures one of its internal comparators (C1) to generate a high-level output when the half-wave rectified (HWR) AC voltage on R9 exceeds an internal threshold (i.e., approximately 0.4 V), thereby activating Q2 to create a negative gate/source voltage (VGS) on depletion-mode MOSFET Q1. In turn, Q1 is caused to turn off when VGS reaches its cutoff threshold (approximately –4 V), thereby limiting the power dissipated by Q1 during its positive half-cycle. When the voltage on R9 is below the Z8F2480 MCU's internal threshold, Comparator C1 output is low, Q2 turns off, and Q1 turns back on to recharge CE1.

Next, the Z8F2480 MCU delays approximately 5 seconds to ensure that its high-precision 20 ppm 32 kHz oscillator is stable. The MCU, by using its more-accurate external oscillator, then self-calibrates the accuracy of its 2.7648 MHz Internal Precision Oscillator (IPO) to allow the software to accurately measure the period of the AC signal, which is later transmitted to the eZ80F91 Module over the optically-isolated I^2C bus, converted to a frequency, and displayed on the eZ80F91 web page.

As part of the initialization sequence, the Z8F2480 MCU's ADC converter is configured to measure the output voltage of the signal conditioner/amplifier circuit (Q3 source). Depending on the setting of Switch U5-A, this amplifier output is either a scaled representation of the AC voltage (as determined by the voltage on RS4) or a scaled representation of the load current (as determined by the voltage drop across the current sense resistor R8). Switch U5-B controls the amplifier gain. When PB5 is active High, the amplifier output is approximately 5.3 times the low-gain amplifier output (PB5 Low). The Z8F2480 firmware always measures (RS4) voltage using the high-gain setting. Initially, current is measured using the low-gain setting. When the gain-select switch is set to low gain, the firmware switches to the high-gain setting when the peak ADC input (PC0) falls below approximately 220 mV (i.e., corresponding to a load current of approximately 770 mA RMS). When the gain-select switch is in the high-gain setting, the firmware switches to the low-gain setting when the peak ADC input (PC0) goes above 1280 mV (i.e., corresponding to a load current of approximately 810 mA RMS).

The final step performed during system initialization is to configure the Z8F2480 MCU's Multi-Channel Timer (MCT) to capture time stamps (measured in IPO clock ticks) just before, and just after, the full-wave rectified (FWR) amplifier output signal goes through a zero crossing (using the voltage on R26 as a reference threshold). These time stamps are captured by connecting the amplifier output to the noninverting input of the Z8F2480 MCU's Internal Comparator C0 and connecting the threshold voltage to the inverting input of Comparator C0. The output of Comparator C0 is connected to MCT channels C and D, and the MCT is configured such that a time stamp is captured on the rising edge (Channel C) and falling edge (Channel D) of C0OUT. MCT channels A and B are similarly configured to capture time stamps on the rising and falling edges of the output of Comparator C1, which is High for most of the positive AC half-cycle when the voltage on R9 exceeds the Z8F2480 MCU's internal reference voltage of 0.4 V.

MCT interrupts are used to measure the AC period and estimate when the next amplifier output peak will occur. This estimate of when the next peak occurs will only be accurate if the load signal is periodic and if the actual AC peak occurs at the exact midpoint between the rising and falling edges of the output of Comparator C0 (e.g., the load signal is sinusoidal). If the load signal meets these conditions, then a secondary timer can be used to generate an interrupt just before the next expected amplifier output peak, thereby allowing the software to obtain ADC samples to measure the peak AC voltage/load current.

The Z8F2480 firmware maintains a rolling average of the number of IPO clock ticks between the last nine HWR peak AC voltages on R9. An instantaneous period is calculated by subtracting the time stamp of the last HWR AC peak voltage (i.e., the midpoint of the Channel A and Channel B time stamps) from the time stamp of the current HWR AC peak voltage. The average period is recalculated on each MCT Channel B interrupt (C1 falling edge) using the last eight delta-times between HWR peaks.

Because the AC period remains relatively constant between zero crossings of the FWR amplifier output, software can set a timeout to occur just before a half-period from the location of the last amplifier output peak (i.e., the midpoint of the MCT Channel C and Channel D time stamps). When the timer expires, a fixed number of ADC samples are taken such that the sampling window begins just before the expected peak occurs and ends just after the expected peak occurs. The largest ADC reading observed during this sampling interval determines the peak voltage of the amplifier output signal.

ADC measurements are taken for both FWR peaks that occur during each AC period. The FWR amplifier output peak that occurs within a quarter of a period of the HWR voltage peak is referred to as the *positive peak*, and the FWR peak that is more than a quarter-period from the HWR peak is the *negative peak*. When reporting the AC voltage and load current to the eZ80F91 webserver, the positive and negative peak values are averaged to provide the voltage and current amplitudes, thereby eliminating offset errors that might be introduced by the signal conditioning and amplification circuit.

By periodically toggling Switch U5-A, the software can alternate between measuring the amplitude of the load current (i.e., the voltage drop across R8) and the amplitude of the FWR AC voltage (the voltage drop across RS4) through the Z8F2480 MCU's ADC block. The software changes the position of Switch U5-A every 9 AC periods just after the falling edge of the negative FWR half-cycle. No ADC samples are taken during the AC

period immediately after the switch is toggled to allow for one initial period measurement and to synchronize to the positive half-cycle of the FWR amplifier output. During the next eight AC periods, individual measurements of the positive and negative FWR amplitudes are averaged together, as are the number of IPO timer ticks between the peak HWR voltage (reference) and positive peak FWR amplifier output to determine the *phase* of the FWR signal. After eight sets of samples have been averaged with Switch U5-A in the voltage position and eight sets of samples have been averaged with Switch U5-A in the current position, the phase shift between voltage and current is calculated by subtracting the load current tick delay (i.e., the I-phase) from the AC voltage tick delay (V-phase) to determine the phase shift between the FWR voltage and FWR current signals.

Firmware running on the Z8F2480 MCU constantly performs these measurements and updates the average AC period, input voltage, load current, and phase shift between peak load voltage and current approximately every 18AC periods (or about 3 times per second).

The eZ80F91 Webserver Module contains a web page that displays the last set of AC measurements obtained by the Z8F2480 MCU. These measurements are transmitted over the optically-isolated I^2C bus established through U4. The eZ80F91 Webserver Module is the I^2C Master, and polls the Z8F2480 MCU (operating as the I^2C slave) to obtain new measurement data. I^2C requests can be initiated by this Master at any time; however, the Z8F2480 MCU only responds to requests for AC measurements when it is otherwise idle. If the Z8F2480 MCU is actively performing a measurement or updating an average, the I^2C request remains pending until the active AC measurement operation/calculation completes. After obtaining the raw measurements, scripts on the web page convert the data into a human-readable format and display the results. A sample of the measurements displayed on the web page is shown in Figure 5.

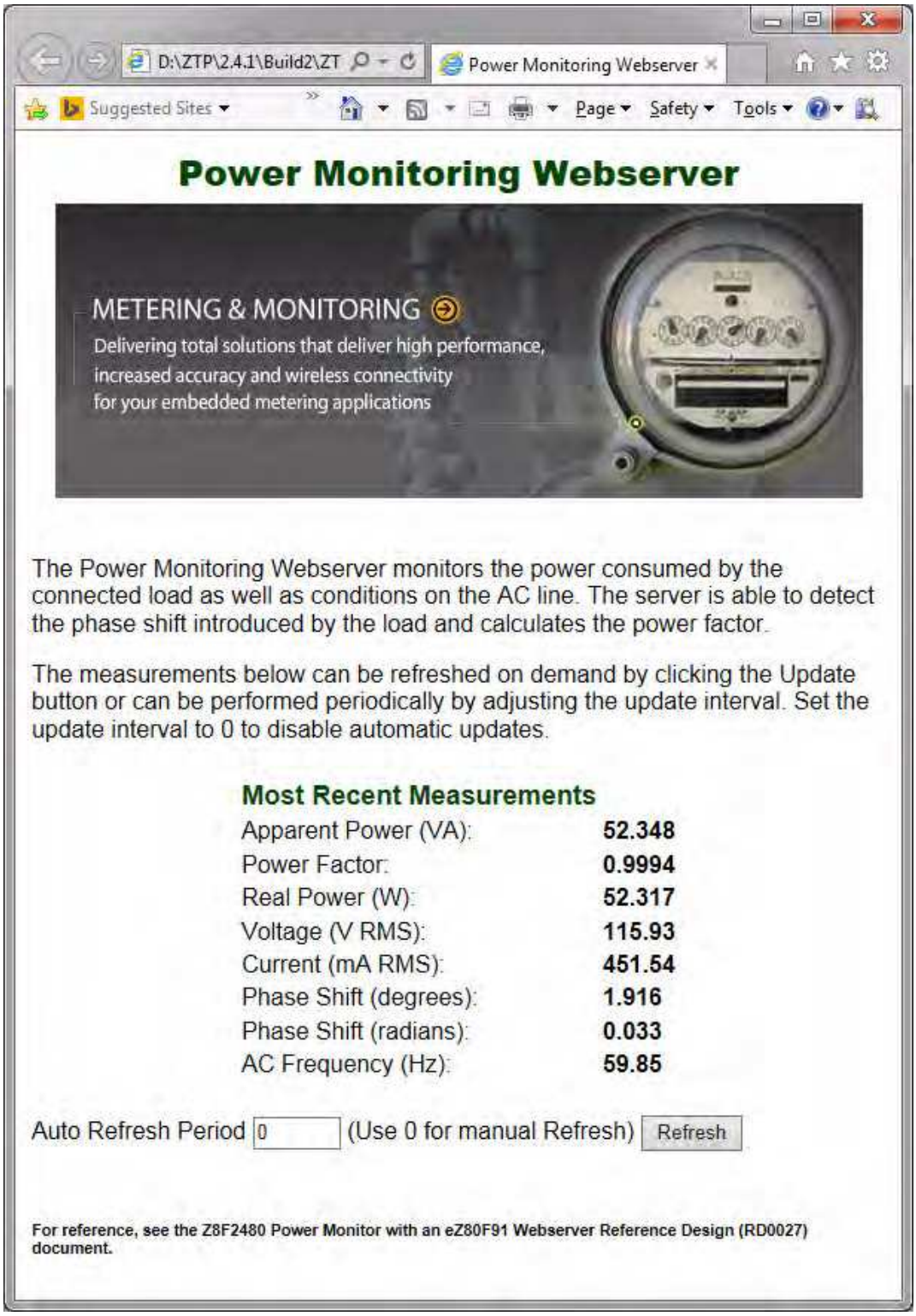

Figure 5. Monitored Measurements Displayed on a Web Page

The measurement values are displayed when the web page is reloaded, when the Refresh button on the page is clicked, or automatically every *n* seconds as determined by the setting of the Automatic Refresh Period on the web page.

Note: When input exceeds recommended operating conditions, the web page shown in Figure 5 will display a warning message.

Setup, Configuration and Use

This section describes how to set up, configure, and operate this reference design.

Setup

This Power Monitor with an eZ80F91 Webserver reference design is delivered with software installed and ready to use. However, be aware that the unit may require calibration. To learn more about calibrating the unit, see the Calibration section on page 15.

To view the Power Monitor web page, observe the following procedure.

1. Disconnect AC power from the Power Board and attach the eZ80F91 Webserver Module to the bottom of the Power Board. Be sure to properly align Pin 1 of J2 on the Webserver Module with Pin 1 of the Power Board to prevent bending any pins. Note that pin 60 of J2 on the Module (located at the bottom right of J2) is missing, and that Pin 1 of J2 is located at the top left corner of J2. Do not attempt to connect J1 on the eZ80F91 Webserver Module to the Power Board; refer to Figure 2 on page 2.
2. Connect an Ethernet cable between the RJ45 connector (P1) on the eZ80F91 Webserver Module and the switch or hub that will be used by the PC to browse the Power Monitor web page. This connection will ensure that the PC and the eZ80F91 Webserver will be assigned an IP address within the same subnet.

Note: The eZ80F91 Webserver has been preconfigured to use DHCP to obtain IP parameters; this setting is appropriate for most networks. If your network uses DHCP, proceed to Step 3. However, if the LAN segment to which the eZ80F91 Webserver module is connected uses static IP addresses, it will be necessary to recompile the eZ80F91 project and reprogram the Module. In this instance, it will be necessary to download and install Zilog Developer Studio (ZDSII) for eZ80Acclaim! version 5.2.0 (or later) with RZP and TCP/IP Object Code; this software can be downloaded free from the Zilog Store. After installing ZDSII, proceed to the Recompiling the eZ80F91 Webserver Software section on page 13.

3. If you have not yet installed the software for this reference design, see the hardcopy insert included in your kit, or navigate the default installation filepath, which is:

   `C:\Program Files (x86)\Zilog\ZRD0027PLM0ZRD_<version>\Docs\`

4. Connect the Zilog UART-to-Serial Adapter (part number 99C1067-001G, included in the Kit) to Jumper J6 on the Power Board.
5. Connect a serial cable between the DB9 connector of the Zilog Serial Adapter and a COM port on your PC, as shown in Figure 6.

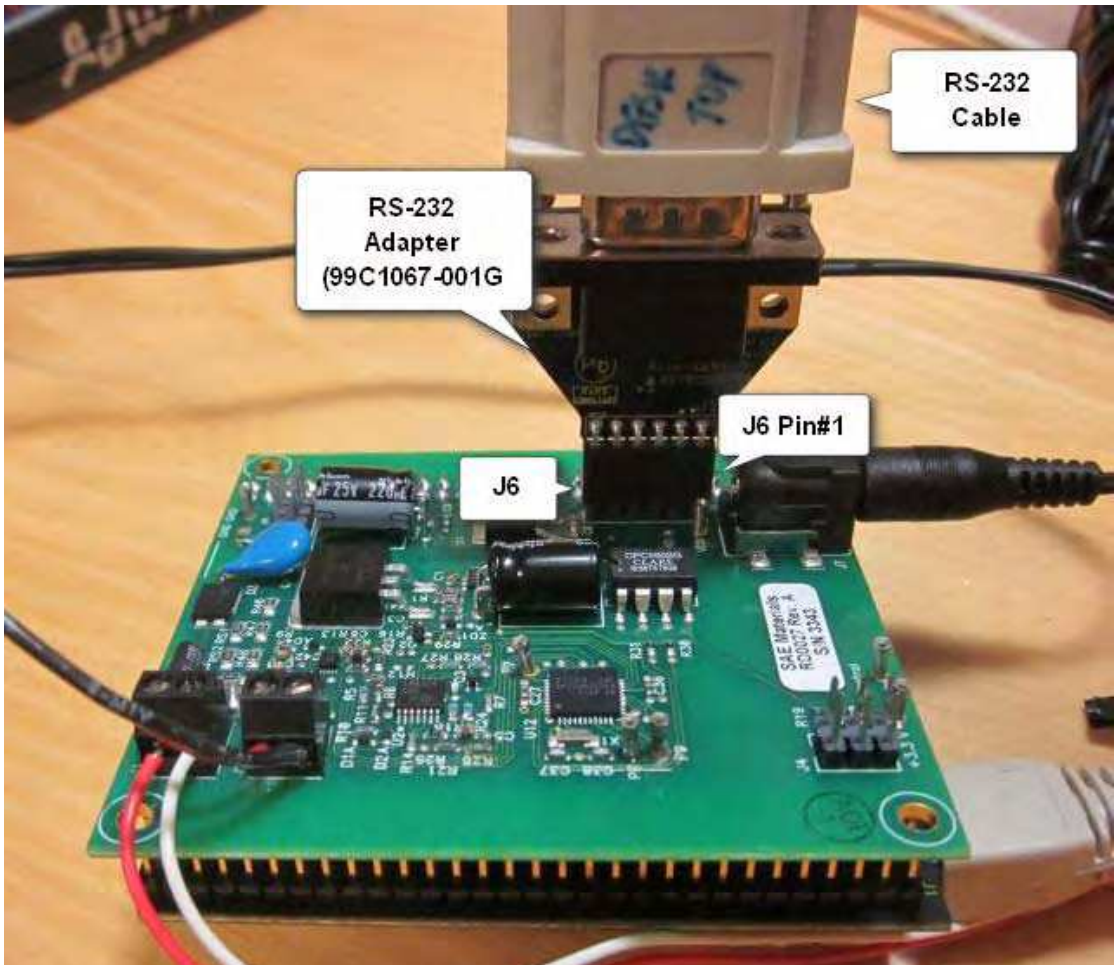

Figure 6. Power Board with Zilog UART-to-Serial Adapter

6. On your PC, launch a terminal emulation program such as Tera Term or HyperTerminal. Configure this terminal program for 57600 8N1.
7. To apply AC power to the Power Board, plug in the 5V wall adapter, and connect the barrel connector from the end of the wall adapter cord to Connector J7 on the Power Board.
8. During system initialization, the eZ80F91 Webserver Module displays its IP address in the terminal window, as shown in the following example:

```
10 Mbps Half-Duplex Link established
Querying DHCP Server...
DHCP OK

Initializing network stack...

IF  IP addr         Def Gtway       State   Type       H/W Addr
0   192.168.1.72    192.168.1.254   UP      Ethernet   0 :90:23:0 :F :91

HTTPD ready
```

9. When the IP address of the eZ80F91 Webserver Module has been determined, open a web browser (such as Internet Explorer) on the PC. In the address bar, enter the IP address of the eZ80F91 Module as displayed by the terminal program.

Note: DHCP servers will typically reassign the same IP address to a device if it is restarted within a short period of time. Therefore, on subsequent attempts to view the Power Monitor web page, it is usually not necessary to connect the Zilog Serial Adapter to the Power Board or use the terminal program. Instead, simply enter the IP address last used by the eZ80F91 Webserver to access the Power Monitor web page.

10. Each time the Power Monitor web page is refreshed, it shows the most recent AC measurements obtained by the Power Board. To obtain an updated set of measurement values, click the **Refresh** button on the web page. To cause the web page to automatically refresh the display, change the Auto Refresh Period from 0 seconds to a nonzero value, then click the **Refresh** button. The Refresh button will then change to a Stop button; therefore, to stop automatic updates of the AC measurements, click the **Stop** button.

Powering the Board and Module

The Power Board receives its power from the same one-phase AC source as the load, with a voltage range of 90V to 240V RMS. If any measurements on the Board will be performed, an isolated power source (i.e., an isolation transformer) should be used to avoid the hazards of electrical shock and board damage.

The eZ80F91 Module requires an isolated +5V source (via wall adapter) connected to Power Jack J7 on the Power Board; for reference, see Figure 4 on page 4.

The Board wakes up with a delay time of approximately one second; the load is connected immediately. Load current is not fuse-protected; therefore, external protection should be implemented to prevent damage to the AC line and the Board in the event of a short circuit.

Warning: The Power Board is electrically connected to AC power and contains points with high voltage (up to 400V). If any measurements will be performed on this reference design, a power supply with an isolation transformer should be used to avoid electrical shock.

Persons working with this reference design should be fully qualified to work with high voltage devices.

Recompiling the Power Monitor Software

The Power Board is delivered with software installed and ready to use. The source code is available in the RD0027-SC01.zip file that is included with this reference design; modifications to this software are not expected to be required. However, should you prefer to make changes and/or learn more about how the software operates, you must obtain a copy of the ZDSII for Z8 Encore! Integrated Development Environment before being able to modify the software and reprogram the Power Board.

Observe the following procedure to download and install the ZDSII software.

1. Download the latest version of ZDSII – Z8 Encore! from the Downloadable Software category of the Zilog Store.
2. Run the software installation file and follow the on-screen instructions to install ZDSII – Z8 Encore!.

To recompile the Power Board software, observe the following procedure:

1. Launch the ZDSII – Z8 Encore! program by navigating via the Windows **Start** menu to **All Programs** → **Zilog** → **ZDS II_Z8Encore! <version_number>** → **ZDSII_Z8Encore! <version_number>**.
2. From the **File** menu, select **Open Project** to display the Open dialog box.
3. In the Open dialog, browse the following default installation filepath:

   `C:\Program Files (x86)\Zilog\ZRD0027PLM0ZRD_1.0\Firmware\Src`
4. From the `Src` folder, select the `RD0027.zdsproj` file, and click **Open** to display the initial ZDSII program screen. To view the source files, double-click the **Project Files** folder on the left side of the IDE interface. Double-click an individual file to open the file in the ZDSII file editor.
5. Click the **Rebuild All** toolbar icon (indicated in Figure 7). When the build completes, a `Build Succeeded` message will appear.

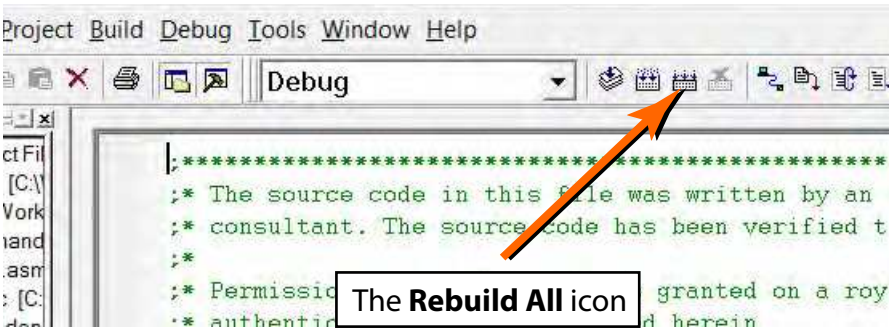

Figure 7. The Rebuild All Icon in ZDSII

6. To reprogram the Power Board, it is necessary to use a Zilog debug tool such as the USB SmartCable. Before proceeding to download new code to the Power Board, disconnect AC power from the Power Board. Next, connect a 6V (or higher) DC power supply between pins J1-1 (+) and J1-2 (–). This step safely provides power to the Z8F2480 MCU on the Power Monitor Board for the purpose of reprogramming the firmware without a direct connection to AC main power.
7. Connect the 6-pin ribbon cable between the USB SmartCable and the Power Board's J4 connector.
8. In the ZDSII IDE, click the **Download** icon ( ) to reprogram the Power Board.
9. When the download is complete, disconnect the power on J1-1 and J1-2. Next, disconnect the 6-pin ribbon cable from the Power Board's J4 connector. Then, with AC power OFF, reconnect AC power to the Power Board's J1 terminal.

Recompiling the eZ80F91 Webserver Software

The Webserver Module is delivered with software installed and ready to use. However, this software may require calibrating to accurately display voltage and current values. Source code for the Webserver Module is available in the RD0027-SC01.zip file that is included with this reference design. To modify the software and/or learn more about how the software operates, users must obtain a copy of the ZDSII for eZ80Acclaim! Integrated Development Environment before being able to modify the software and reprogram the Module.

Observe the following procedure to download and install the ZDSII software.

1. Download the latest version ZDSII – eZ80Acclaim! from the Downloadable Software category of the Zilog Store.
2. Run the software installation file and follow the on-screen instructions to install ZDSII – eZ80Acclaim!.

To recompile the Webserver software, observe the following procedure:

1. Launch the ZDSII – eZ80Acclaim! program by navigating via the Windows **Start** menu to: **All Programs → Zilog → ZDSII_eZ80Acclaim!_<version_number> → ZDSII_eZ80Acclaim! <version_number>**.
2. From the **File** menu, select **Open Project** to display the Open dialog box.
3. In the Open dialog, browse the following default installation filepath:

   ```
   C:\Program Files (x86)\Zilog\ZDSII_eZ80Acclaim!_5.2.1\
   ZTP\ZTP2.4.1_Lib\ZTP\SamplePrograms\F91_WebServer
   ```

4. From the `F91_WebServer` folder, select the `ZTPDemo_eZ80F91x150MODG.zdsproj` file and click **Open** to display the initial ZDSII program screen. To view the source files, double-click the **Project Files** folder on the left side of the IDE interface. Double-click an individual file to open the file in the ZDSII file editor.
5. Click the **Rebuild All** toolbar icon (seen in Figure 7). When the build completes, a `Build Succeeded` message will appear.

   If changes are made to the `index.html` file, it will be necessary to delete the ZDSII-generated `index_htm.c` file located in the `RD0027_PM_Web\F91_WebServer\WebSite` path before performing a **Rebuild All**. Deleting this file ensures that ZDSII will regenerate the `index_htm.c` file and include any changes made to the file in the new program image.

Note: If it is necessary to use static IP addresses, then change the value of the `b_use_dhcp` variable in the `ZTPConfig.c` file from TRUE to FALSE. Additionally, the default values used in the `ifTbl` array for the Ethernet interface may require modification to match the static IP configuration assigned by your network administrator. It is not necessary to make any changes to the `ZTPConfig.c` file if the network uses a DHCP server to assign IP parameters.

6. To reprogram the Power Board, it is necessary to use a Zilog debug tool such as the USB SmartCable. Before proceeding to download new code to the Power Board, disconnect AC power from the Power Board, but leave the 5V wall adapter plugged into an AC outlet.
7. Connect the 6-pin ribbon cable between the USB SmartCable and the Power Board's J5 connector.
8. In the ZDSII IDE, click the **Download** icon ( ) to reprogram the Webserver Module.
9. When the download is complete, disconnect the 6-pin ribbon cable from the Power Board, then unplug the 5V wall adapter from the Webserver Module.
10. Reconnect AC main power to the Power Board, then plug in the 5V wall adapter.

Calibration

The Z8F2480 Power Monitor board software measures voltage and currents by using an internal analog-to-digital converter (ADC). The web page that the PC browser obtains from the eZ80F91 Webserver contains javascript that converts ADC values into voltages or currents. For this javascript to display accurate voltage/current values, equations in the script must be calibrated for the particular Z8F2480 Power Monitor board attached to the eZ80F91 Webserver Module. There are three equations that must be adjusted to accomplish this calibration, namely: voltage, high current range, and low current range.

The calibration process computes the slope and y intercept of a set of (x,y) data points that span the range of current/voltage inputs. For each data point, the (median) value of the ADC input is the independent variable (x), and the actual line voltage/load current is the dependent variable (y). At least two data points are required to compute the slope and y intercept, but multiple data points may be used to improve the accuracy of interpolated values. As more data points are used for calibration, it will be necessary to use PC software capable of performing a linear least-squares regression analysis. Both free and professional analysis tools are readily available on the Internet.

When calibration is complete, the values to be modified in the javascript are shown below for reference:

```
V = 0.41763816126957 * LineVoltage + 5.2586067419112;
if( LoadCurrent & 0x8000 )
{
  I = 5.183353039 * (LoadCurrent & 0x7FFF) + 42.05404895723;
}
else
{
  I = 0.96950933849967 * LoadCurrent + 15.774942218407;
}
```

Observe the following procedure to perform voltage calibration.

1. Connect an AC power supply capable of producing the desired range of line voltage (e.g., 90V to 240V) to the Power Board.
2. Using a known (purely resistive) load, sweep the input voltage from *min* to *max* in 5V or 10V increments.
   a. For each input voltage, note the value displayed on the web page and covert this value to a raw ADC value using the following equation (which is contained in the `index.htm` javascript file):

      ```
      V = 0.41763816126957 * LineVoltage + 5.2586067419112;
      ```

      For example, if the web page displays a voltage of 211.99V, this voltage value corresponds to an ADC value of:

      ROUND((211.99 - 5.25861) / 0.41764) = 495

b. Alternatively, enter the `i2c_tracce on` command on the eZ80F91 console to cause the last AC measurement results to be displayed. For example, consider the following trace:

```
Period b3c5  V 01ef  I 81f0  Phase 0000 IPO 002a08dd
Period b3c1  V 01f0  I 81ef  Phase 0000 IPO 002a08dd
Period b3c2  V 01ef  I 81ef  Phase 0000 IPO 002a08dd
Period b3c3  V 01ef  I 81f0  Phase 0000 IPO 002a08dd
Period b3c0  V 01ef  I 81ef  Phase 0000 IPO 002a08dd
```

The average ADC voltage value of these 5 traces is `0x01EFh` (495 decimal).

c. Construct a table of (x,y) values in which the x value corresponds to the average ADC reading value (see above); the y value corresponds to the actual AC input voltage (RMS). In the running example, if the average ADC value is 495 when the AC input voltage is 205V RMS, then the data point obtained is (495,205).

3. After sweeping through all input voltages, use a linear least-squares analysis tool to determine the slope and Intercept values that provide the lowest amount of errors over the voltage range sampled.
4. Next, modify the `index.htm` javascript file located in the `ZTPDemo_RD0027\Website` folder and edit the voltage equation to use the calibrated slope and intercept values.
5. Delete the compiler-generated `index_htm.c` file, rebuild the project, and reprogram the eZ80F91 target.

   a. Note that after modifying the javascript file, it may be necessary to force the browser to reload the web page by using CTRL+F5 instead of clicking the Reload button.
   b. Additionally, note that it may take 7 to 8 seconds for the browser to display measurement data if the eZ80F91 MCU is reprogrammed while the browser is running.
6. Repeat this voltage calibration with the new slope and intercept to verify that the measurement results are within the desired level of accuracy. In some instances, it may be necessary to repeat this process a second time.

Low-Gain Current Calibration

Observe the following procedure to perform a low-gain current calibration.

1. When calibrating load current, configure the AC signal generator to produce the expected nominal line voltage (e.g., 120V) and modify the load resistance to sweep through the upper current range.
   a. It will be necessary to insert an AC ammeter in series with the load to measure the actual load current and adjust the load resistance to step the current by approximately 10mA for each measurement.

b. Note that the voltage on PB5 of the Z8F2480 determines whether the amplifier's high-gain or low-gain range is used.

2. Typically, the amplifier will be configured for low gain when the load current is above 810mA RAM, and low gain when the load current is below 770mA RMS. Between 770mA and 810mA, either gain setting can be used. Additionally, note that these thresholds will vary from one development kit to the next, as determined by the characteristics of their respective circuit components.

3. The calibration process is then performed for each step in the upper current range recording (x,y) values, in which the x value corresponds to the average ADC reading value, and the y value corresponds to the actual AC load current (RMS).

   a. The default transfer equation used in the javascript for low-gain current is:

   I = 0.96950933849967 * LoadCurrent + 15.774942218407

   b. As with voltage measurements, the output of the `i2c_trace on` console command can be used to obtain the ADC values.

4. Use the same linear least-square regression analysis to determine the calibrated slope and coefficient to be used in the javascript equation.

5. Repeat the low-gain calibration to obtain the desired input accuracy.

High-Gain Current Calibration

The process for calibrating the high-gain slope and intercept values in the javascript transfer equation are very similar to the low-gain calibration process. The only difference is to use load currents below the low-to-high-gain threshold of the measurement board (nominally at an ADC input voltage of 810mA).

The default high-gain transfer equation is:

I = 5.183353039 * (LoadCurrent & 0x7FFF) + 42.05404895723

Electrical Specifications

This section describes the electrical characteristics of this reference design and reflects all available data as a result of testing prior to qualification and characterization. As such, the data presented in this document is subject to change.

Table 1 lists the maximum voltage, current and temperature ratings for this reference design.

Table 1. Absolute Maximum Ratings

Parameter	Rating	Unit
AC voltage RMS maximum	250	V
Load current	3.3	A

Note: The maximum AC rating is 250V; however, normal operation ranges up to 240V only. When input voltage exceeds 240V, the web page shown in Figure 5 will display a warning message.

Table 1. Absolute Maximum Ratings (Continued)

Parameter	Rating	Unit
Storage temperature range	–40 to +120	°C
Operating temperature range	–30 to +80	°C
Isolation voltage between the AC line and the eZ80F91 Webserver Module	3750	V

Note: The maximum AC rating is 250 V; however, normal operation ranges up to 240 V only. When input voltage exceeds 240 V, the web page shown in Figure 5 will display a warning message.

Note: Stresses greater than those listed in Table 1 may cause permanent damage to the eZ80F91 Webserver Module or to the Power Board. These ratings are stress ratings only. Operation of the devices described at any condition outside those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods affects device reliability.

Table 2 lists the recommended voltage and temperature conditions for this reference design.

Table 2. Recommended Operating Conditions

Parameter	Rating	Unit
AC voltage RMS range	90–240	V
Ambient temperature range	–20 to +45	°C

Table 3 lists the electrical operating characteristics for this reference design.

Table 3. Electrical Operating Characteristics

Name	Condition	Min.	Typ.	Max.	Units
Power Board load current		0.15		3	A
Input current	Power Board consumption only from AC line, average value at 120 V RMS.		5		mA

Related Documentation

The documents associated with reference design are listed in Table 4. Each of these documents can be obtained from the Zilog website by clicking the link associated with its Document Number.

Table 4. Z8F2480 Power Monitor with eZ80F91 Webserver Documentation

Document Number	Description
RD0027	This Z8F2480 Power Monitor with eZ80F91 Webserver Reference Design document
PS0306	eZ80Acclaim!/eZ80AcclaimPlus! Ethernet Module Product Specification
PS0250	Z8 Encore! XP F1680 Product Specification
PS0270	eZ80F91 ASSP Product Specification
FL0164	Z8F2480 Power Monitor with eZ80F91 Webserver Kit Insert

Ordering Information

This reference design is available as a kit, as shown in the Kit Contents section that follows. It can be purchased from the Zilog Store – simply click the Store Product ID listed in Table 5.

Table 5. Zilog Store Ordering Information

Part Number	Description	Store Product ID
ZRD0027PLM0ZRD	Z8F2480 Power Monitor with eZ80F91 Webserver Reference Design	RD10035

Kit Contents

The Z8F2480 Power Monitor with eZ80F91 Webserver Reference Design contains the following items:

- Z8F2480 AC Monitor Power Board
- eZ80F91 Webserver Module
- 5 VDC power supply
- UART-to-RS232 adapter
- Z8F2480 Power Monitor with eZ80F91 Webserver Kit Insert (FL0164)

Note: The eZ80F91 Webserver Module and the Z8F2480 MCU on the Power Board are preprogrammed by Zilog during manufacturing.

Results

Figures 9 and 10 diagram the voltage and current measurement errors of a calibrated Z8F2480 Power Monitor with eZ80F91 Webserver with respect to the AC voltage and load current, respectively (60Hz line frequency).

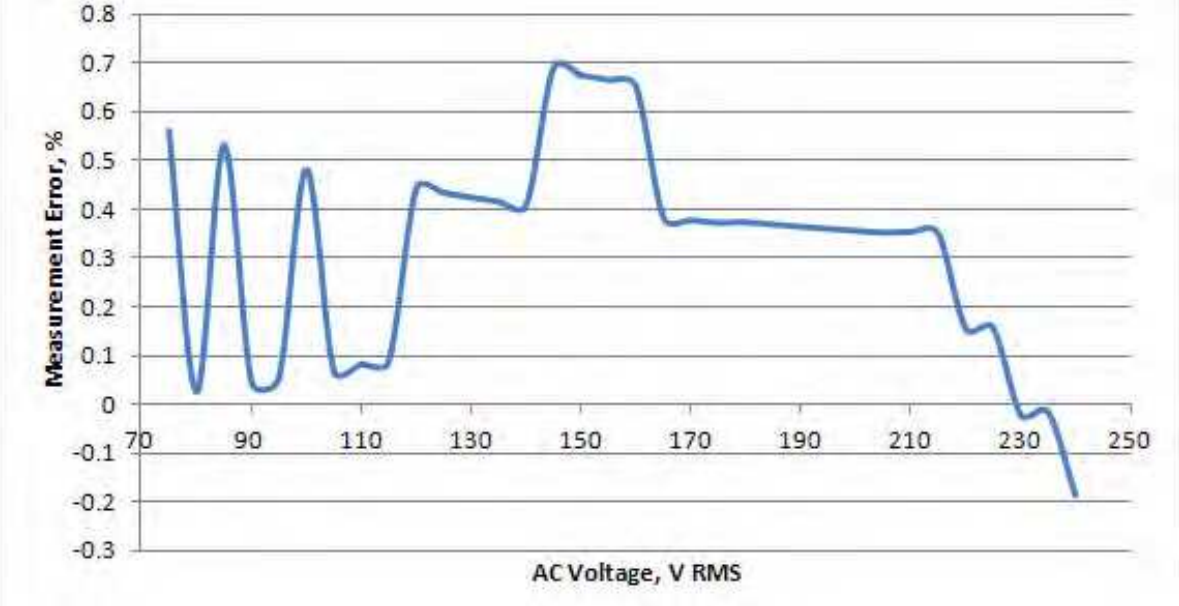

Figure 8. Voltage Measurement Error vs. AC Voltage

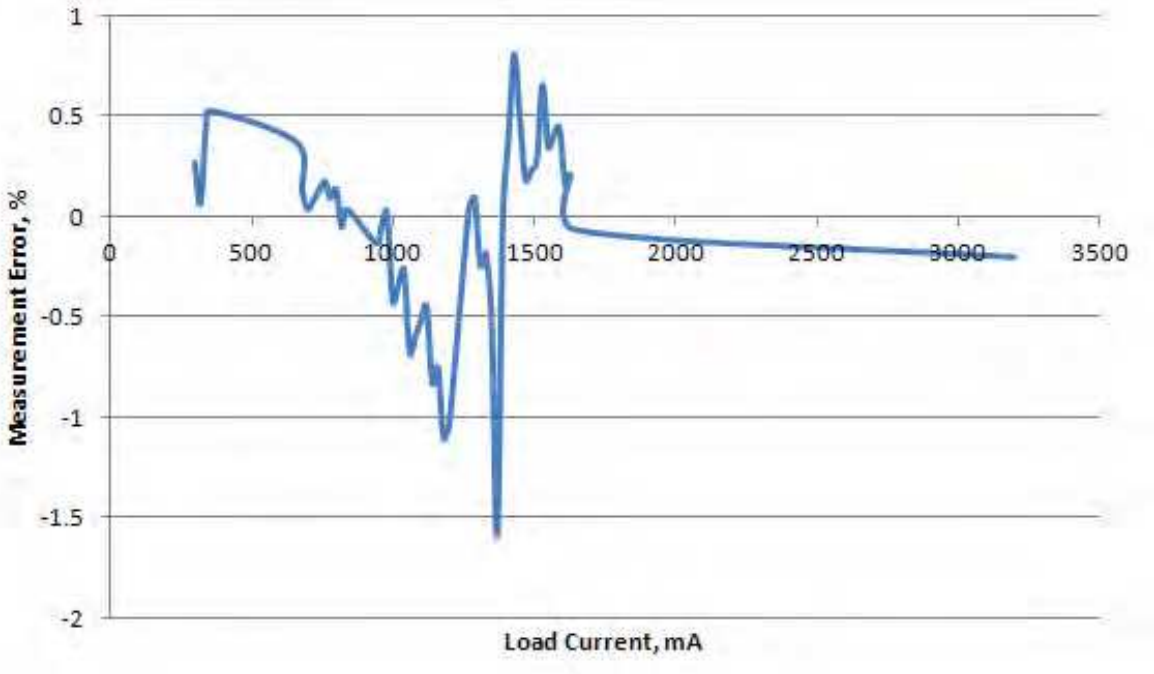

Figure 9. Current Measurement Error vs. Load Current

Summary

When calibrated, this Z8F2480 Power Monitor with an eZ80F91 Webserver reference design is able to measure line voltages and load currents over an entire input range with an error rate of less than 2%.

The accuracy of the phase shift measurement in this reference design was not analyzed; however, when using purely resistive loads (i.e., current and voltage in-phase), the web page typically shows a power factor close to 1, as expected, suggesting that at least for resistive loads, the system is reasonably accurate.

Although no attempt was made to calibrate the displayed line frequency, the Z8F2480 Power Monitor software does perform a self-calibration of its Internal Precision Oscillator (IPO) just after startup that improves the accuracy of the line frequency measurement displayed on the web page. When used with 60Hz systems, the displayed frequency contains less than 2% error. It is expected that the displayed frequency will also be within 2% of the AC line frequency for 50Hz systems.

Appendix A. Schematic Diagrams

Figure 10 displays a schematic diagram of the Power Board.

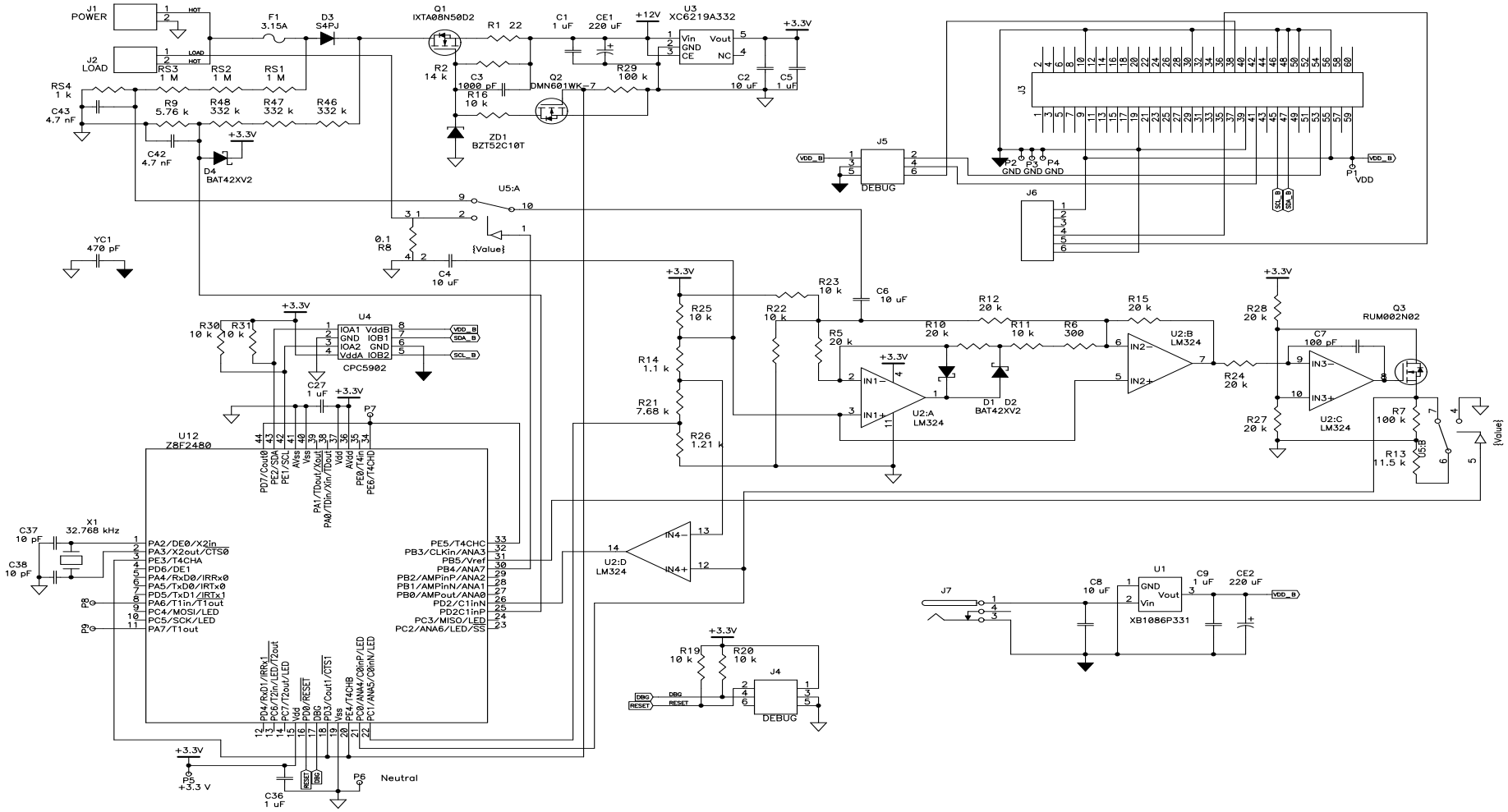

Figure 10. Schematic Diagram of the Z8F2480 MCU-Based Power Board

Appendix B. Bill Of Materials

The bills of materials used to build the two major components of this reference design are located in the following paths upon installation of the RD0027-SC01 software that accompanies this document.

```
<Install Directory>\ZRD0027PLM0ZRD_1.0\PCB\eZ80F91 Webserver\
99C1380-002G\99C1380-002G.xls

<Install Directory>\ZRD0027PLM0ZRD_1.0\PCB\Z8F2480 Power Monitor\
99C1432-001G\AC_Test_Board_2_BOM.doc
```

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