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Brief Description

The ZSC31010 is a sensor signal conditioner integrated circuit, which enables easy and precise calibration of resistive bridge sensors via EEPROM. When mated to a resistive bridge sensor, it will digitally correct offset and gain with the option to correct offset and gain coefficients and linearity over temperature. A second-order compensation can be enabled for temperature coefficients of gain or offset or bridge linearity. The ZSC31010 communicates via IDT's ZACwire™ serial interface to the host computer and is easily mass calibrated in a Windows® environment. Once calibrated, the output pin Sig™ can provide selectable 0 to 1 V, rail-to-rail ratiometric analog output, or digital serial output of bridge data with optional temperature data.

Features

- Digital compensation of sensor offset, sensitivity, temperature drift, and non-linearity

- Accommodates differential sensor signal spans, from 3 mV/V to 105 mV/V

- ZACwire™ One-Wire Interface (OWI)

- Internal temperature compensation and detection via bandgap PTAT (proportional to absolute temperature)

- Output options: rail-to-rail analog output voltage, absolute analog voltage, digital ZACwire™ One-Wire Interface (OWI)

- Optional sequential output of both temperature and bridge readings on ZACwire™ digital output

- Fast response time, 1 ms (typical)

- High voltage protection up to 30 V with external JFET

- Chopper-stabilized true differential ADC

- Buffered and chopper-stabilized output DAC

Benefits

- No external trimming components required

- Simple PC-controlled configuration and calibration via ZACwire™ One-Wire Interface

- High accuracy (±0.1% FSO @ -25 to 85°C; ±0.25% FSO @ -50 to 150°C)

- Single pass calibration – quick and precise

- Suitable for battery-powered applications

- Small SOP8 package

Available Support

- Development Kit available

- Mass Calibration Kit available

- Support for industrial mass calibration available

- Quick circuit customization possible for large production volumes

Physical Characteristics

- Supply voltage 2.7 to 5.5 V, with external JFET 5.5V to 30 V

- Current consumption depending on adjusted sample rate: 0.25 mA to 1 mA

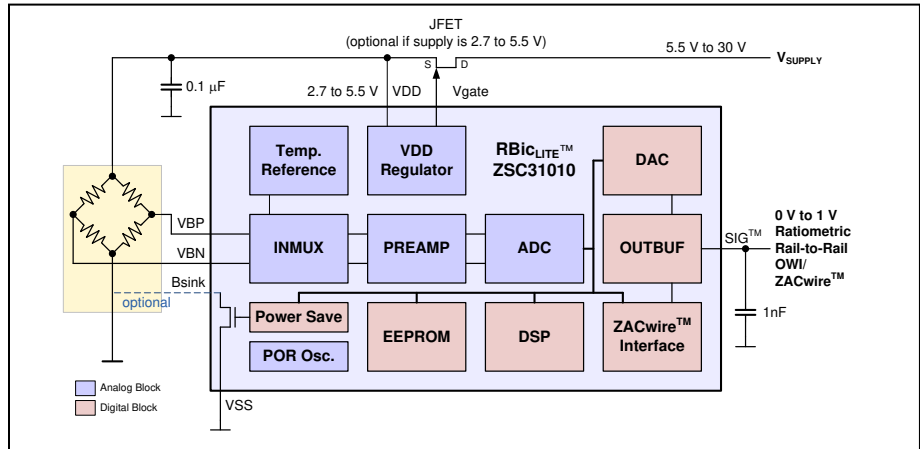- Wide operational temperature: –50 to +150°C

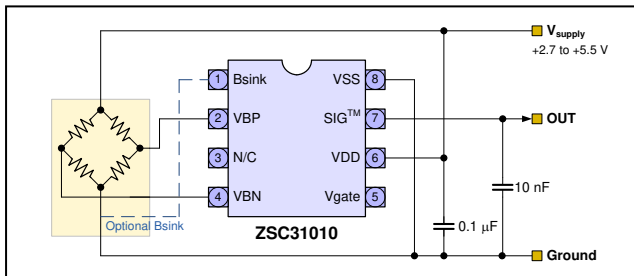### *ZSC31010 Application Circuit – Digital Output*
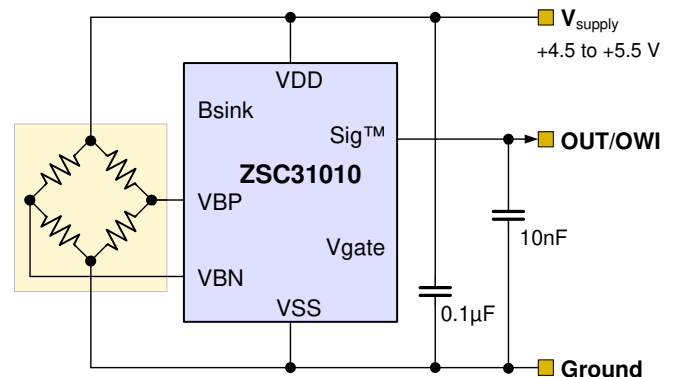
ZSC31010 Block Diagram
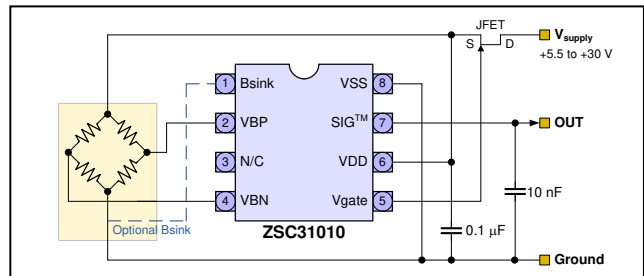
Highly Versatile Applications in Many Markets Including

- ❖ *Industrial*
- ❖ *Building Automation*
- ❖ *Office Automation*
- ❖ *White Goods*
- ❖ *Automotive*
- ❖ *Portable Devices*
- ❖ *Your Innovative Designs*

Rail-to-Rail Ratiometric Voltage Output Applications

Absolute Analog Voltage Output Applications

Ordering Examples *(Please see section 11 in the data sheet for additional options.)*

Sales Code	Description	Package
ZSC31010CEB	ZSC31010 Die — Temperature range: -50°C to +150°C	Unsawn on Wafer
ZSC31010CEC	ZSC31010 Die — Temperature range: -50°C to +150°C	Sawn on Wafer Frame
ZSC31010CEG1	ZSC31010 SOP8 (150 mil) — Temperature range: -50°C to +150°C	Tube: add "-T" to sales code Reel: add "-R"
ZSC31010KIT	ZSC31010 ZACwire™ SSC Evaluation Kit: Communication Board, SSC Board, Sensor Replacement Board, USB Cable, 5 IC Samples	Kit

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Tech Support
www.IDT.com/go/support

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1   Electrical Characteristics

1.1.   Absolute Maximum Ratings

Note: The absolute maximum ratings are stress ratings only. The device might not function or be operable above the operating conditions given in section 1.2. Stresses exceeding the absolute maximum ratings might also damage the device. In addition, extended exposure to stresses above the recommended operating conditions might affect device reliability. IDT does not recommend designing to the "Absolute Maximum Ratings."

Parameter	Symbol	Conditions	Min	Max	Unit
Analog Supply Voltage	V_{DD}		-0.3	6.0	V
Voltages at Analog I/O – In Pin	V_{INA}		-0.3	VDD+0.3	V
Voltages at Analog I/O – Out Pin	V_{OUTA}		-0.3	VDD+0.3	V
Storage Temperature Range	T_{STG}		-50	150	°C
Storage Temperature Range	$T_{STG\,<10h}$	For periods < 10 hours	-50	170	°C

Note: Also see Table 6.1 regarding soldering temperature and storage conditions for the SOP-8 package.

1.2.   Recommended Operating Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Analog Supply Voltage to Ground	V_{DD}		2.7	5.0	5.5	V
Analog Supply Voltage (with external JFET Regulator)	V_{SUPP}		5.5	7	30	V
Common Mode Voltage	V_{CM}		1		V_{DDA} - 1.3	V
Ambient Temperature Range [1, 2]	T_{AMB}		-50		150	°C
External Capacitance between V_{DD} and Ground	C_{VDD}		100	220	470	nF
Output Load Resistance to V_{DD}	$R_{L,OUT}$		2.5	10		kΩ
Output Load Resistance to V_{SS} [3) 4)]	$R_{L,OUT}$		2.5	20		kΩ
Output Load Capacitance [5]	$C_{L,OUT}$		1	10	15	nF
Bridge Resistance [6]	R_{BR}		0.2		100	kΩ
Power ON Rise Time	t_{PON}				100	ms

[1] Note that the maximum EEPROM programming temperature is 85°C.

[2] If buying die, designers should use caution not to exceed maximum junction temperature by proper package selection.

[3] When using the output for digital calibration, no pull down resistor is allowed.

[4] For loads less than 20 kΩ to VSS an equivalent strength (or lower) pull-up resistor must be added.

[5] Using the output for digital calibration, $C_{L,OUT}$ is limited by the maximum rise time $T_{ZAC,rise}$.

[6] Note: Minimum bridge resistance is only a factor if using the Bsink feature. The nominal R_{DS}(ON) of the Bsink transistor is 10 Ω when operating at V_{DD} = 5 V, and 15 Ω when operating at V_{DD} = 3.0 V. This does give rise to a ratiometricity inaccuracy that becomes greater with low bridge resistances.

1.3. Electrical Parameters

See important table notes at the end of the table. Note: For parameters marked with an asterisk, there is no verification in mass production; the parameter is guaranteed by design and/or quality observation.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
1.3.1. Supply/Regulation Characteristics						
Supply Voltage	V_{DD}		2.7	5.0	5.5	V
Supply Current (varies with update rate and output mode)	I_{DD}	At minimum update rate		0.25		mA
		At maximum update rate		1.0	1.2	
Temperature Coefficient – Regulator (worst case) *	TC_{REG}	Tem. -10°C to 120°C			35	ppm/K
		Temp. < -10°C and > 120°C			100	
Power Supply Rejection Ratio *	PSRR	DC < 100 Hz (JFET regulation loop using mmbf4392 and 0.1 µF decoupling cap)	60			dB
		AC < 100 kHz (JFET regulation loop using mmbf4392 and 0.1 µF decoupling cap)	45			dB
Power-On Reset Level	POR		1.4		2.6	V
1.3.2. Analog Front-End (AFE) Characteristics						
Leakage Current Pin VBP,VBN	I_{IN_LEAK}				±10	nA
1.3.3. EEPROM Parameters						
Number Write Cycles	n_{WRI_EEP}	At 150°C At 85°C			100 100k	Cycles
Data Retention	t_{WRI_EEP}	At 100°C			10	Years
1.3.4. A/D Converter Characteristics						
ADC Resolution	r_{ADC}			14		Bit
Integral Nonlinearity (INL) [1]	INL_{ADC}		-4		+4	LSB
Differential Nonlinearity (DNL) *	DNL_{ADC}		-1		+1	LSB
Response Time	$T_{RES,ADC}$	Varies with update rate. Value given at fastest rate.		1		ms
1.3.5. Analog Output (DAC and Buffer) Characteristics						
Max. Output Current	I_{OUT}	Max. current maintaining accuracy	2.2			mA
Resolution	r_{OUT}	Referenced to V_{DD}			11	Bit
Absolute Error	E_{ABS}	DAC input to output	-10		+10	mV
Differential Nonlinearity *	DNL	No missing codes	-0.9		+1.5	LSB_{11Bit}
Upper Output Voltage Limit	V_{OUT}	R_L = 2.5 kΩ	95%			V_{DD}
Lower Output Voltage Limit	V_{OUT}				16.5	mV

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
1.3.6. ZACwire™ Serial Interface						
ZACwire™ Line Resistance *	$R_{ZAC,line}$	The rise time $T_{ZAC,rise}$ must be $2 * R_{ZAC,line} * C_{ZACload} \leq 5\mu s$. If using a pull-up resistor instead of a line resistor, it must meet this specification.			3.9	kΩ
ZACwire™ Load Capacitance *	$C_{ZAC,load}$		0	1	15	nF
ZACwire™ Rise Time *	$T_{ZAC,rise}$				5	µs
Voltage Level Low *	$V_{ZAC,low}$			0	0.2	V_{DD}
Voltage Level High *	$V_{ZAC,low}$		0.8	1		V_{DD}
1.3.7. System Response Characteristics						
Start-Up-Time	t_{STA}	Power-up to output			10	ms
Response Time	t_{RESP}	Update_rate = 1 kHz (1 ms)		1	2	ms
Sampling Rate	f_S	Update_rate = 1 kHz (1 ms)		1000		Hz
Overall Linearity Error	E_{LIND}	Bridge input to output – Digital		0.025	0.04	%
Overall Linearity Error	E_{LINA}	Bridge input to output – Analog		0.1	0.2	%
Overall Ratiometricity Error	RE_{out}	±10%VDD, not using Bsink feature			0.035	%
Overall Accuracy – Digital (only IC, without sensor bridge)	AC_{outD}	-25°C to 85°C			±0.1%	%FSO
		-50°C to 150°C			±0.25%	
Overall Accuracy – Analog (only IC, without sensor bridge) [2), 3)]	AC_{outA}	-25°C to 85°C			±0.25%	%FSO
		-40°C to 125°C			±0.35%	
		-50°C to 150°C			±0.5%	

[1)] Note: This is ± 4 LSBs to the 14-bit A-to-D conversion. This implies absolute accuracy to 12 bits on the A-to-D result. Non-linearity is typically better at temperatures less than 125°C.

[2)] Not included is the quantization noise of the DAC. The 11-bit DAC has a quantization noise of ± ½ LSB = 1.22 mV (5V VDD) = 0.025%

[3)] Analog output range 2.5% to 95%.

1.4.   Analog Inputs versus Output Resolution

The ZSC31010 incorporates an extended 14-bit charge-balanced ADC, which allows for a single gain setting on the pre-amplifier to handle bridge sensitivities from 1.2 to 36 mV/V while maintaining 8 to 12 bits of output resolution with a default analog gain of 24. Selectable gain settings allow accommodating bridges with different sensitivities. The tables below illustrate the minimum resolution achievable for a variety of bridge sensitivities. The yellow shadowed fields indicate that for these input spans with the selected analog gain setting, the quantization noise is higher than 0.1% FSO.

Table 1.1   ADC Resolution Characteristics for an Analog Gain of 6

Analog Gain 6				
Input Span [mV/V]			Allowed Offset (+/- % of Span) [1]	Minimum Guaranteed Resolution [Bits]
Min	Typ	Max		
57.3	80.0	105.8	38%	13.3
50.6	70.0	92.6	53%	13.1
43.4	60.0	79.4	73%	12.9
36.1	50.0	66.1	101%	12.6
28.9	40.0	52.9	142%	12.3
21.7	30.0	39.7	212%	11.9
[1] In addition to Tco, Tcg				

Table 1.2   ADC Resolution Characteristics for an Analog Gain of 12

Analog Gain 12				
Input Span [mV/V]			Allowed Offset (+/- % of Span) [1]	Minimum Guaranteed Resolution [Bits]
Min	Typ	Max		
43.3	60.0	79.3	3%	13.0
36.1	50.0	66.1	17%	12.7
25.3	35.0	46.3	53%	12.2
18.0	25.0	33.0	101%	11.7
14.5	20.0	26.45	142%	11.4
7.2	10.0	13.22	351%	10.4
3.6	5.0	6.6	767%	9.4
[1] In addition to Tco, Tcg				
Note: Yellow shadowing indicates that for these input spans with the selected analog gain setting, the quantization noise is > 0.1% FSO.				

Table 1.3   ADC Resolution Characteristics for an Analog Gain of 24

Analog Gain 24				
Input Span [mV/V]			Allowed Offset (+/- % of Span) [1]	Minimum Guaranteed Resolution [Bits]
Min	Typ	Max		
16	25.0	36	25%	12.6
12.8	20.0	28.8	50%	12
6.4	10.0	14.4	150%	11
3.2	5.0	7.2	400%	10
1.6	2.5	3.6	900%	9
0.8	1.2	1.7	2000%	8
[1] In addition to Tco,Tcg Note: Yellow shadowing indicates that for these input spans with the selected analog gain setting, the quantization noise is > 0.1% FSO.				

Table 1.4   ADC Resolution Characteristics for an Analog Gain of 48

Analog Gain 48				
Input Span [mV/V]			Allowed Offset (+/- % of Span) [1]	Minimum Guaranteed Resolution [Bits]
Min	Typ	Max		
10.8	15.0	19.8	3%	13
7.2	10.0	13.2	35%	12.4
4.3	6.0	7.9	100%	11.7
2.9	4.0	5.3	190%	11.1
1.8	2.5	3.3	350%	10.4
1.0	1.4	1.85	675%	9.6
0.72	1.0	1.32	975%	9.1
[1] In addition to Tco,Tcg Note: Yellow shadowing indicates that for these input spans with the selected analog gain setting, the quantization noise is > 0.1% FSO.				

2   Circuit Description

2.1.   Signal Flow and Block Diagram

The ZSC31010 resistive bridge sensor interface ICs were specifically designed as a cost-effective solution for sensing in building automation, industrial, office automation, and white goods applications. The RBic$_{Lite}$™ employs IDT's high precision bandgap with proportional-to-absolute temperature (PTAT) output; a low-power 14-bit analog-to-digital converter (ADC, A2D, A-to-D); and an on-chip DSP core with EEPROM to precisely calibrate the bridge output signal. Three selectable output modes, two analog and one digital, offer the ultimate in versatility across many applications.

The ZSC31010 rail-to-rail ratiometric analog output Vout signal (0 to 5 V, Vout @ VDD = 5 V) suits most building automation and automotive requirements. Typical office automation and white goods applications require the 0 to 1 Vout signal, which in the ZSC31010 is referenced to the internal bandgap. Direct interfacing to microprocessor controllers is facilitated via IDT's single-wire serial ZACwire™ digital interface.

The ZSC31010 is capable of running in high-voltage (5.5 to 30 V) systems when combined with an external JFET.

Figure 2.1   ZSC31010 Block Diagram
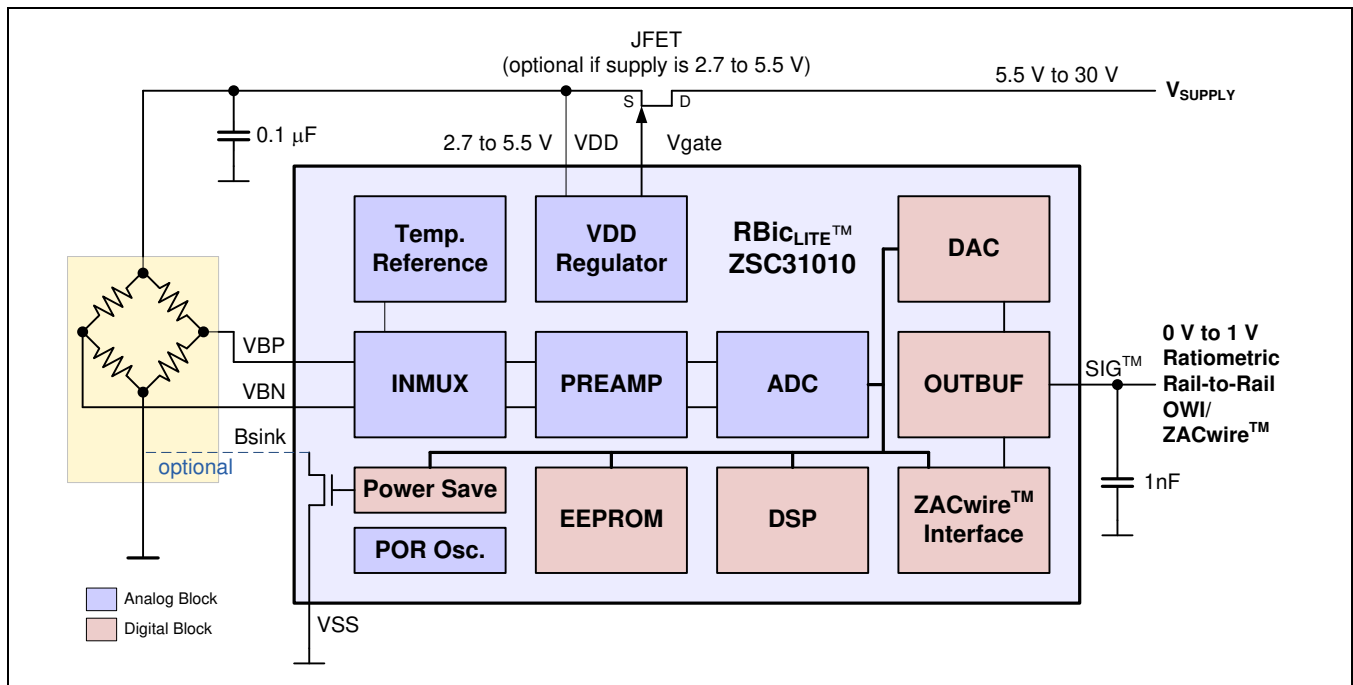
2.2. Analog Front End

2.2.1. Bandgap/PTAT and PTAT Amplifier

The highly linear Bandgap/PTAT provides the PTAT signal to the ADC, which allows accurate temperature conversion. In addition, the ultra-low ppm-Bandgap provides a stable voltage reference over temperature for the operation of the rest of the IC.

The PTAT signal is amplified through a path in the pre-amplifier (PREAMP) and fed to the ADC for conversion. The most significant 12 bits of this converted result are used for temperature measurement and temperature correction of bridge readings. When temperature is output in Digital Mode, only the most significant 8 bits are given.

2.2.2. Bridge Supply

The voltage driven bridge is usually connected to V_{DD} and ground. As a power savings feature, the ZSC31010 also includes a switched transistor to interrupt the bridge current via the Bsink pin. The transistor switching is synchronized to the A/D-conversion and released after finishing the conversion. To utilize this feature, the low supply of the bridge should be connected to Bsink instead of ground.

Depending on the programmable update rate, the average current consumption (including bridge current) can be reduced to approximately 20%, 5% or 1%.

2.2.3. PREAMP Block

The differential signal from the bridge is amplified through a chopper-stabilized instrumentation amplifier with very high input impedance, designed for low noise and low drift. This PREAMP provides gain for the differential signal and re-centers its DC to $V_{DD}/2$. The output of the PREAMP block is fed into the A/D-converter. The calibration sequence performed by the digital core includes an auto-zero sequence to null any drift in the PREAMP state over temperature.

The PREAMP is nominally set to a gain of 24. Other possible gain settings are 6, 12, and 48.

The inputs to the PREAMP from the VBN/VBP pins can be reversed via an EEPROM configuration bit.

2.2.4. Analog-to-Digital Converter (ADC)

A 14-bit/1 ms 2nd-order charge-balancing ADC is used to convert signals coming from the PREAMP. The converter, designed in full differential switched-capacitor technique, is used for converting the various signals to the digital domain. This principle offers the following advantages:

- High noise immunity because of the differential signal path and integrating behavior
- Independent from clock frequency drift and clock jitter
- Fast conversion time owing to second order mode

Four selectable values for the zero point of the input voltage allow the conversion to adapt to the sensor's offset parameter. The conversion rate varies with the programmed update rate. The fastest conversion rate is 1 k samples/s; the response time is then 1 ms. Based on a best fit, the Integral Nonlinearity (INL) is < 4 LSB_{14Bit}.

2.3. Digital Signal Processor

A digital signal processor (DSP) is used for processing the converted bridge data as well as for performing temperature correction and for computing the temperature value for output on the digital channel.

The DSP reads correction coefficients from the EEPROM and can correct for

- Bridge Offset
- Bridge Gain
- Variation of Bridge Offset over Temperature (Tco)
- Variation of Bridge Gain over Temperature (Tcg)
- A Single Second Order Effect (SOT - Second Order Term)

The EEPROM contains a single SOT that can be applied to correct one and only one of the following:

- 2nd order behavior of bridge measurement
- 2nd order behavior of Tco
- 2nd order behavior of Tcg

(For more details, see section 3.6.1.)

If the SOT applies to correcting the bridge reading, then the correction formula for the bridge reading is represented as a two step process as follows:

$$ZB = Gain\_B(1 + \Delta T * Tcg) * (BR\_Raw + Offset\_B + \Delta T * Tco) \tag{1}$$

$$BR = ZB(1.25 + SOT * ZB) \tag{2}$$ `

Where:

BR	= Corrected Bridge reading that is fed as digital or analog output on Sig™ pin
ZB	= Intermediate result in the calculations
BR_Raw	= Raw Bridge reading from ADC
T_Raw	= Raw Temperature reading converted from PTAT signal
Gain_B	= Bridge gain term
Offset_B	= Bridge offset term
Tcg	= Temperature coefficient gain
Tco	= Temperature coefficient offset
ΔT	= (T_Raw - T_{SETL})
T_Raw	= Raw Temperature reading converted from PTAT signal
T_{SETL}	= Raw PTAT reference value (See *Technical Note—ZSC31010, ZSC31015, and ZSSC3015 Calibration Sequence, DLL, and EXE* for details.*)*
SOT	= Second Order Term

Note: See section 3.6.2.7 for limitations when SOT applies to the bridge reading.

If the **SOT** applies to correcting the 2nd order behavior of **Tco**, then the formula for bridge correction is as follows:

$$BR = Gain\_B(1 + \Delta T * Tcg) * [BR\_Raw + Offset\_B + \Delta T(SOT * \Delta T + Tco)] \tag{3}$$

Note: See section 3.6.2.7 for limitations when SOT applies to Tco.

If the SOT applies to correcting the 2nd order behavior of Tcg, then the formula for bridge correction is as follows:

$$BR = Gain\_B[1 + \Delta T(SOT * \Delta T + Tcg)] * [BR\_Raw + Offset\_B + \Delta T * Tco] \tag{4}$$

The bandgap reference gives a very linear PTAT signal, so temperature correction can always simply be accomplished with a linear gain and offset term.

Corrected Temp Reading:

$$T = Gain\_T(T\_Raw + Offset\_T) \tag{5}$$

Where:

    T_Raw   = Raw Temperature reading converted from PTAT signal

    Offset_T   = Temperature sensor offset coefficient

    Gain_T   = Temperature gain coefficient

2.3.1. EEPROM

The EEPROM contains the calibration coefficients for gain and offset, etc., and the configuration bits, such as output mode, update rate, etc. When programming the EEPROM, an internal charge-pump voltage is used, so a high voltage supply is not needed. The EEPROM is implemented as a shift register. During an EEPROM read, the contents are shifted 8 bits before each transmission of one byte occurs.

The charge-pump is internally regulated to 12.5 V, and the programming time is typically 6 ms.

Note: EEPROM writing can only be performed at temperatures lower than 85°C.

2.3.2. One-Wire Interface—ZACwire™

The IC communicates via a One-Wire Serial Interface (OWI, ZACwire™). There are different commands available for the following:

- Reading the conversion result of the ADC (Get_BR_Raw, Get_T_Raw)
- Calibration commands
- Reading from the EEPROM (dump of entire contents)
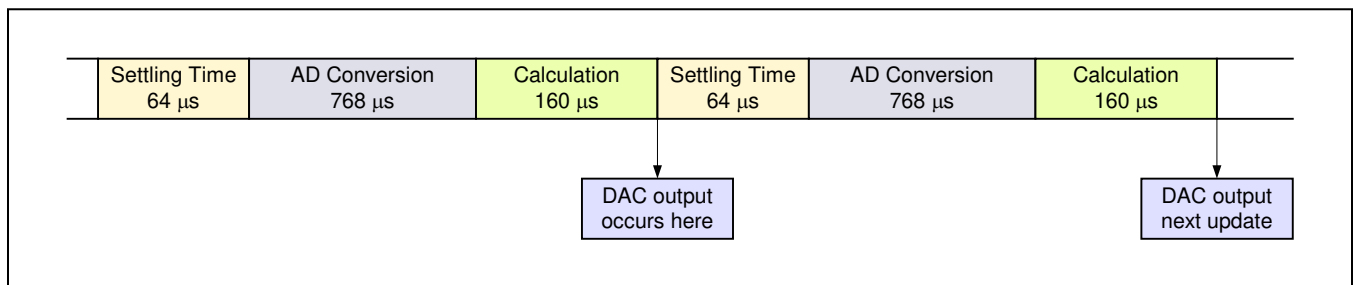- Writing to the EEPROM (trim setting, configuration, and coefficients)

2.4. Output Stage

2.4.1. Digital to Analog Converter (Output DAC)

An 11-bit DAC, based on sub-ranging resistor strings, is used for the digital-to-analog output conversion in the analog ratiometric and absolute analog voltage modes. Selection during calibration configures the system to operate in either of these modes. The design allows for excellent testability as well as low power consumption.

Figure 2.2 shows the data timing of the DAC output with the 1 kHz update rate setting.

Figure 2.2   DAC Output Timing for Highest Update Rate

Settling Time 64 μs	AD Conversion 768 μs	Calculation 160 μs	Settling Time 64 μs	AD Conversion 768 μs	Calculation 160 μs	
			DAC output occurs here			DAC output next update

2.4.2. Output Buffer

A rail-to-rail operational amplifier (OpAmp) configured as a unity gain buffer can drive resistive loads (whether pull-up or pull-down) as low as 2.5 kΩ and capacitances up to 15 nF. To limit the error due to amplifier offset voltage, an error compensation circuit is included which tracks and reduces the offset voltage to < 1 mV.

2.4.3. Voltage Reference Block

A linear regulator control circuit is included in the Voltage Reference Block to interface with an external JFET to allow operation in systems where the supply voltage exceeds 5.5 V. This circuit can also be used for over-voltage protection. The regulator set point has a coarse adjustment via an EEPROM bit (see section 2.3.1), which can adjust the set point around 5.0 V or 5.5 V. In addition, the 1 V trim setting (see below) can also act as a fine adjustment for the regulation set point.

Note: If using the external JFET for over-voltage protection purposes (i.e., 5 V at JFET drain and expecting 5 V at JFET source), there will be a voltage drop across the JFET; therefore ratiometricity will be compromised somewhat depending on the rds(on) of the chosen JFET. A Vishay J107 is the best choice, because it has only an 8 mV drop worst case. If using as regulation instead of over-voltage, an MMBF4392 also works well.

The Voltage Reference Block uses the absolute reference voltage provided by the Bandgap to produce two regulated on-chip voltage references. A 1 V reference is used for the output DAC high reference, when the part is configured for 0 to 1 V analog output. For this reason, the 1 V reference must be very accurate and includes trim, such that its value can be trimmed within +/-3 mV of 1.0 V. The 1 V reference is also used as the on-chip reference for the JFET regulator block, so the regulation set point of the JFET regulator can be fine-tuned, using the 1 V trim. The 5 V reference can be trimmed within +/-15 mV. Table 2.1 shows the order of trim codes with 0111_B for the lowest reference voltage, and 1000_B for the highest reference voltage.

Table 2.1   Order of Trim Codes

Order	1Vref/5Vref__trim3	1Vref/5Vref_trim2	1Vref/5Vref_trim1	1Vref/5Vref_trim0
Highest Reference Voltage	1	0	0	0
...	1	0	0	1
...	1	0	1	0
...	1	0	1	1
...	1	1	0	0
...	1	1	0	1
...	1	1	1	0
...	1	1	1	1
...	0	0	0	0
...	0	0	0	1
...	0	0	1	0
...	0	0	1	1
...	0	1	0	0
...	0	1	0	1
...	0	1	1	0
Lowest Reference Voltage	0	1	1	1

2.5.   Clock Generator / Power-On Reset (CLKPOR)

If the power supply exceeds 2.5 V (maximum), the reset signal de-asserts, and the clock generator starts operating at a frequency of approximately 512 kHz (+17% / -22%). The exact value only influences the conversion cycle time and the communication to the outside world, but not the accuracy of signal processing. In addition, to minimize the oscillator error as the V_{DD} voltage changes, an on-chip regulator is used to supply the oscillator block.

2.5.1. Trimming the Oscillator

Trimming is performed at wafer level, and it is strongly recommended that this is not to be changed during calibration, because ZACwire™ communication is no longer guaranteed at different oscillator frequencies.

Table 2.2   Oscillator Trimming

Trimming Bits	Delta Frequency (kHz)
100	+385
101	+235
110	+140
111	+65
000	Nominal
001	-40
010	-76
011	-110

Example: Programming $011_B \rightarrow$ the trimmed frequency = nominal value - 110 kHz.

3   Functional Description

3.1.   General Working Mode

The command/data transfer takes place via the one-wire Sig™ pin, using the ZACwire™ serial communication protocol. After power-on, the IC waits for 6 ms (i.e., the command window) for the Start_CM command. Without this command, the Normal Operation Mode (NOM) starts. In this mode, raw bridge values are converted, and the corrected values are presented on the output in analog or digital format (depending on the configuration stored in EEPROM).

Command Mode (CM) can only be entered during the 6 ms command window after power-on. If the IC receives the Start_CM command during the command window, it remains in the Command Mode. The CM allows changing to one of the other modes via command. After command Start_RM, the IC is in the Raw Mode (RM). Without correction, the raw values are transmitted to the digital output in a predefined order. The RM can only be stopped by power-off. Raw Mode is used by the calibration software for collection of raw bridge and temperature data, so the correction coefficients can be calculated.

Figure 3.1   General Working Mode
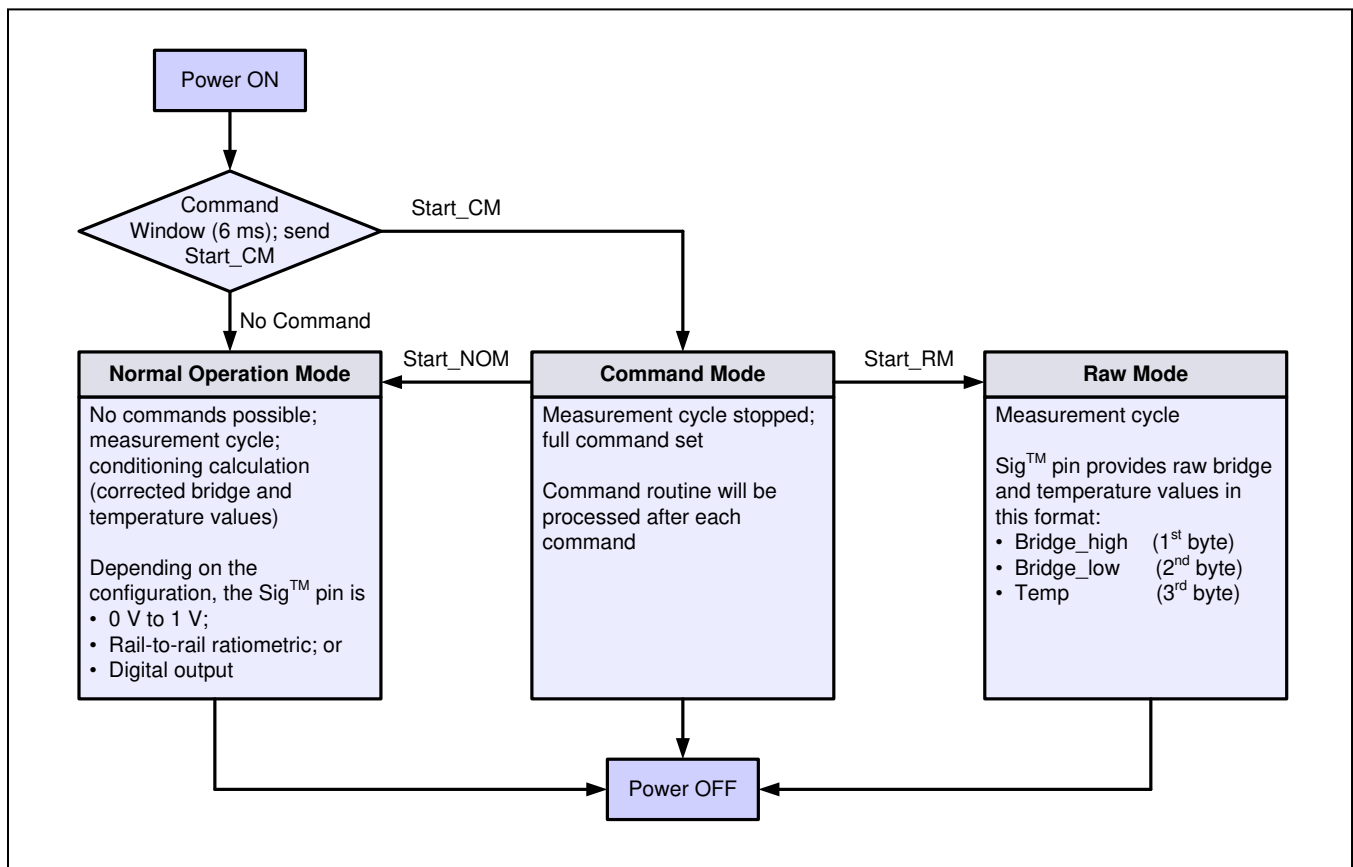
3.2.   ZACwire™ Communication Interface

3.2.1.   Properties and Parameters

Table 3.1   Pin Configuration and Latch-Up Conditions

No.	Parameter	Symbol	Min	Typ	Max	Unit	Comments
1	Pull-up resistor (on-chip)	$R_{ZAC,pu}$		30		kΩ	On-chip pull-up resistor switched on during Digital Output Mode and during CM Mode (first 6 ms after power up)
2	Pull-up resistor (external)	R_{ZAC,pu_ext}	150			Ω	If the master communicates via a push-pull stage, no pull-up resistor is needed; otherwise, a pull-up resistor with a value of at least 150 Ω must be connected.
3	ZACwire™ rise time	$T_{ZAC,rise}$			5	µs	Any user RC network included in Sig™ path must meet this rise time
4	ZACwire™ line resistance [1]	$R_{ZAC,line}$			3.9	kΩ	Also see section 1.3.6 in the specification tables.
5	ZACwire™ load capacitance [1]	$C_{ZAC,load}$	0	1	15	nF	Also see section 1.3.6 in the specification tables.
6	Voltage low level	$V_{ZAC,low}$		0	0.2	V_{DD}	Rail-to-rail CMOS driver
7	Voltage high level	$V_{ZAC,high}$	0.8	1		V_{DD}	Rail-to-rail CMOS driver
[1] The rise time must be $T_{ZAC,rise} = 2 * R_{ZAC,line} * C_{ZACload} \leq 5$ µs . If using a pull-up resistor instead of a line resistor, it must meet this specification.							

3.2.2. Bit Encoding

Figure 3.2   Manchester Duty Cycle
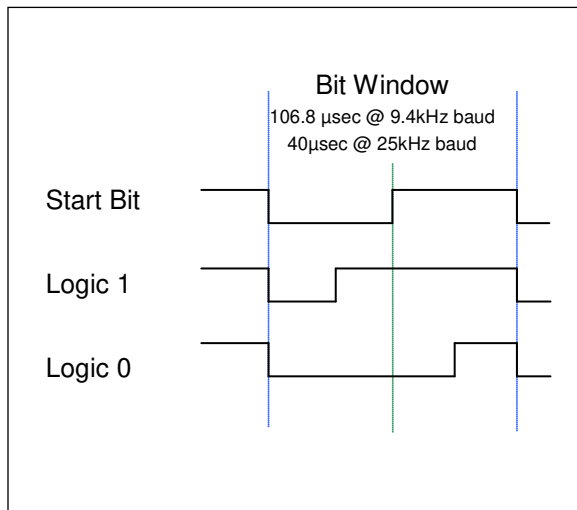
Start bit = 50% duty cycle used to set up strobe time

Logic 1 = 75% duty cycle

Logic 0 = 25% duty cycle

Stop Time

The ZACWire™ bus will be held high for 32 µs (nominal) between consecutive data packets regardless of baud rate.

3.2.3.   Write Operation from Master to ZSC31010

The calibration master sends a 19-bit packet frame to the ZSC31010.

Figure 3.3   19-Bit Write Frame
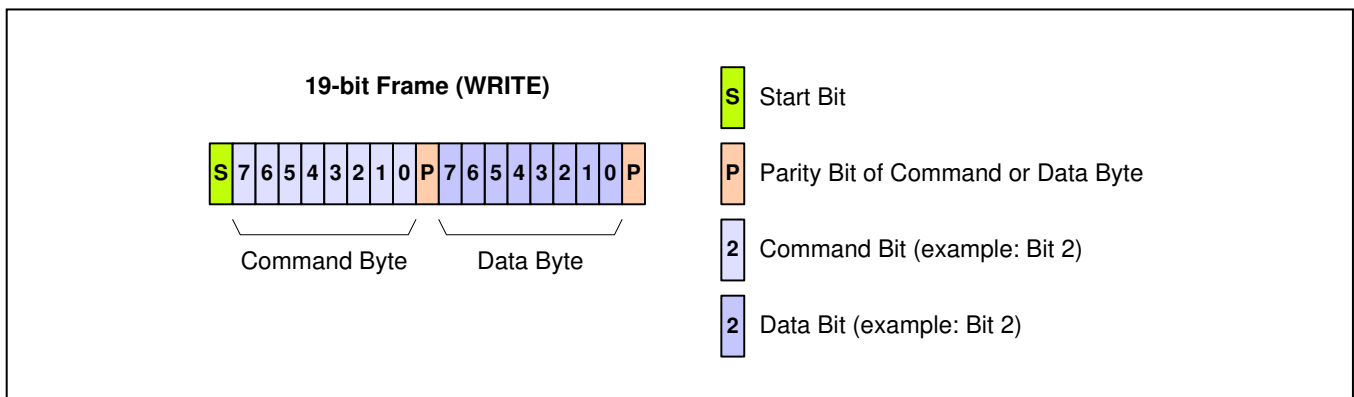
The incoming serial signal will be sampled at a 512 kHz clock rate. This protocol is very tolerant to clock skew and can easily tolerate baud rates in the 6 kHz to 48 kHz range.

3.2.4. ZSC31010 Read Operations

The incoming frame will be checked for proper parity on both, command and data bytes, as well as for any edge time-outs prior to a full frame being received.

Once a command/data pair is received, the ZSC31010 will perform that command. After the command has been successfully executed by the IC, the IC will acknowledge success by a transmission of an $A5_H$-byte back to the master. If the master does not receive an $A5_H$ transmission within 130 ms of issuing the command, it must assume the command was either improperly received or could not be executed.

Figure 3.4   Read Acknowledge
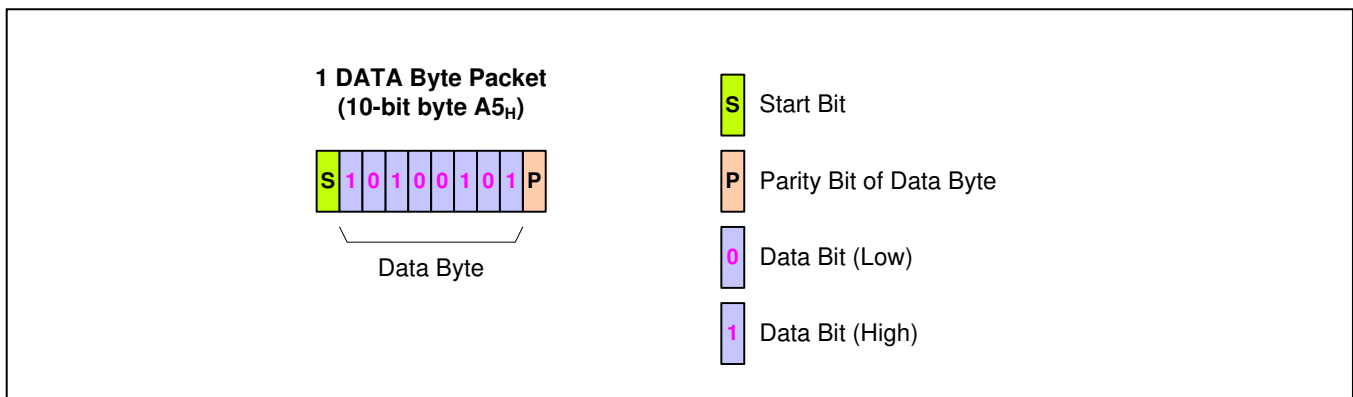
The ZSC31010 transmits 10-bit bytes (1 start bit, 8 data bits, 1 parity bit). During calibration and configuration, transmissions are normally either $A5_H$ or data. $A5_H$ indicates successful completion of a command. There are two different digital output modes configurable (digital output with temperature, and digital output with only bridge data). During Normal Operation Mode, if the part is configured for digital output of the bridge reading, it first transmits the high byte of bridge data, followed by the low byte. The bridge data is 14 bits in resolution, so the upper two bits of the high byte are always zero-padded. There is a 32 μs stop time when the bus is held high between bytes in a packet.

Figure 3.5   Digital Output (NOM) Bridge Readings
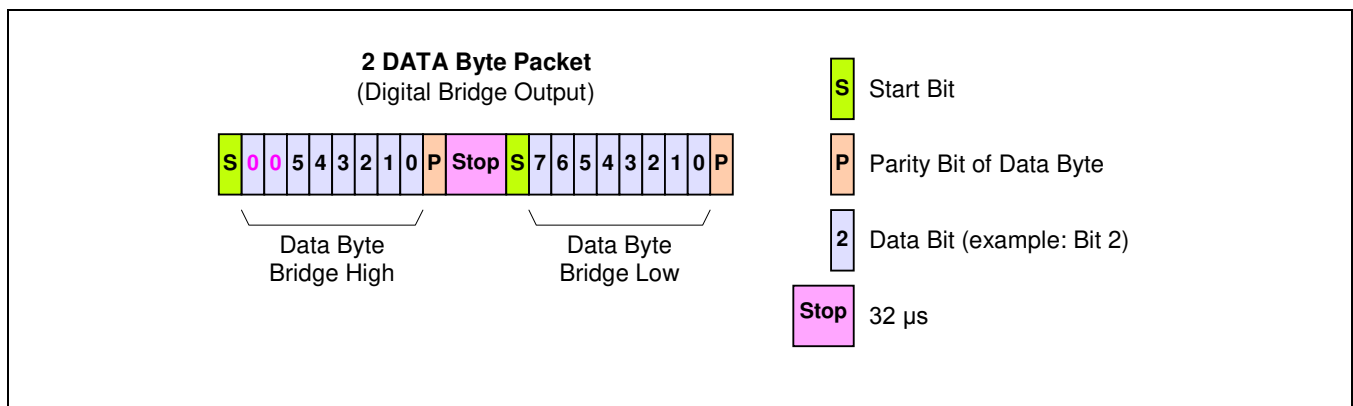
The second digital output mode is digital output bridge reading with temperature. It will be transmitted as a 3-data-byte packet. The temperature byte represents an 8-bit temperature quantity, spanning from -50 to 150°C.

Figure 3.6   Digital Output (NOM) Bridge Readings with Temperature

3 DATA Byte Packet
(Digital Bridge Output with Temperature)
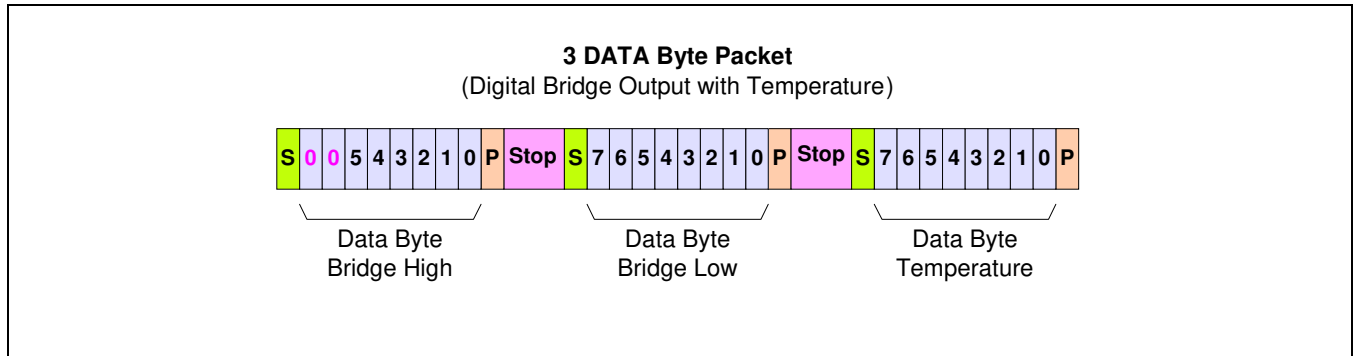
The EEPROM transmission occurs in a packet with 14 data bytes, as shown below.

Figure 3.7   Read EEPROM Contents

14 DATA Byte Packet
(Read EEPROM)
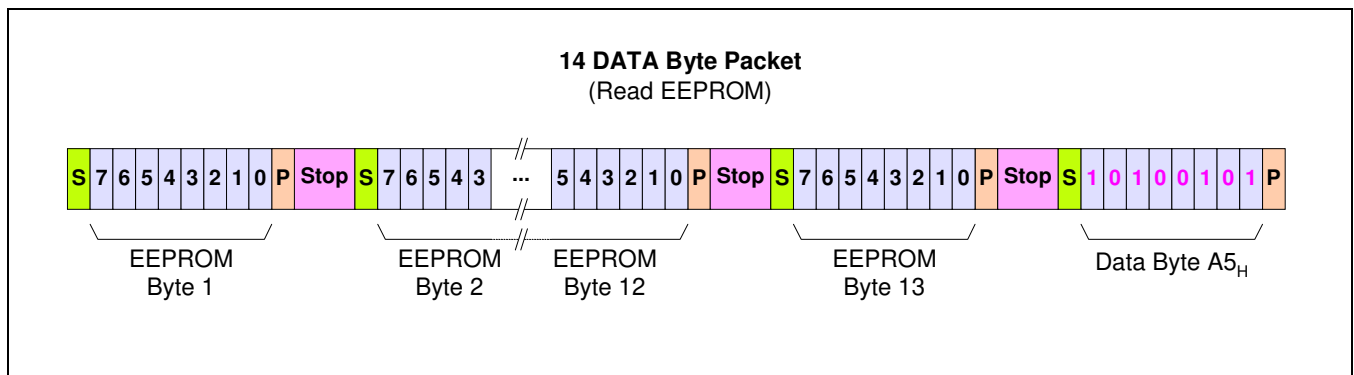
There is a variable idle time between packets, which varies with the update rate setting in the EEPROM.

Figure 3.8   Transmission of a Number of Data Packets

Packet Transmission
(This example shows 2 DATA packets)

Table 3.2 shows the idle time between packets versus the update rate. This idle time can vary by nominal +/-15% between parts, and over a temperature range of -50 to 150ºC.

Transmissions from the IC occur at one of two speeds depending on the update rate programmed in EEPROM. If the user chooses one of the two fastest update rates (1 ms or 5 ms) then the baud rate of the digital transmission will be 32 kHz (minimum 25 kHz). If, however, the user chooses one of the two slower update rates (25 ms or 125 ms), then the baud rate of the digital transmission will be 8 kHz (maximum 9.4 kHz).
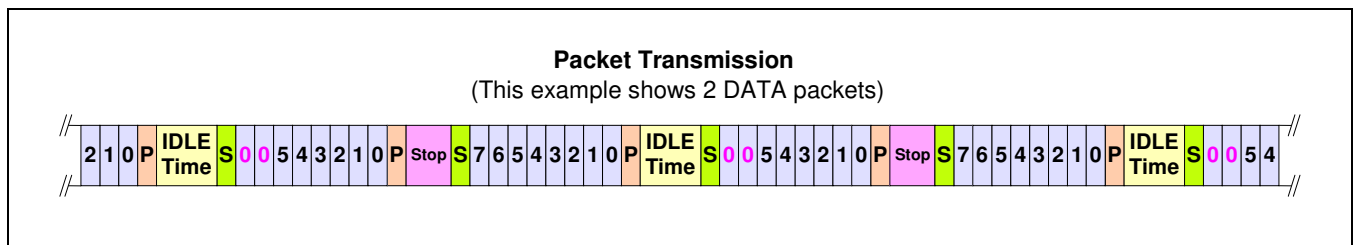
The total transmission time for both digital output configurations is shown in Table 3.2.

Table 3.2   Total Transmission Time for Different Update Rate Settings and Output Configuration

Update Rate	Baud Rate*	Idle Time	Transmission Time – Bridge Only Readings			Transmission Time – Bridge & Temperature Readings		
1 ms (1 kHz)	32 kHz	1.0 ms	20.5 bits	31.30 µs	1.64 ms	31.0 bits	31.30 µs	1.97 ms
5 ms (200 Hz)	32 kHz	4.85 ms	20.5 bits	31.30 µs	5.49 ms	31.0 bits	31.30 µs	5.82 ms
25 ms (40 Hz)	8 kHz	22.5 ms	20.5 bits	125.00 µs	25.06 ms	31.0 bits	125.00 µs	26.38 ms
125 ms (8 Hz)	8 kHz	118.0 ms	20.5 bits	125.00 µs	120.56 ms	31.0 bits	125.00 µs	121.88 ms
* Typical values. Minimum baud rate for 1 ms or 5 ms: 26kHz; maximum baud rate for 25 ms or 125 ms: 9.4kHz.								

The temperature raw reading is performed less often than a bridge reading, because the temperature changes more slowly.

Table 3.3 shows the timing for the special measurements (temperature and bridge measurement) in the different update rate modes.

Table 3.3   Special Measurement versus Update Rate

Update Rate Setting	Special Measurement
00	Every 128 bridge measurements
01	Every 64 bridge measurements
10	Every 16 bridge measurements
11	Every 8 bridge measurements

It is easy to program any standard microcontroller to communicate with the ZSC31010. IDT can provide sample code for a MicroChip® PIC microcontroller.

For update rates less than 1 kHz, the output is followed by a power-down, as shown below.

Figure 3.9   ZACwire™ Output Timing for Lower Update Rates

Calculation 160 µs	ZACwire™ Output	Power Down (determined by Update Rate)	Power-On Settling 128 µs	Settling Time 64 µs	ADC Conversion 768 µs	Calculation 160 µs	ZACwire™ Output
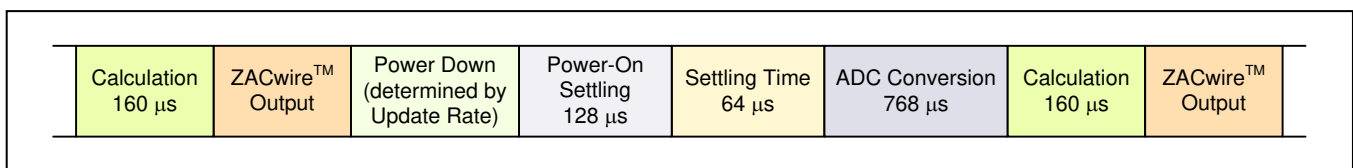
3.2.5. High Level Protocol

The ZSC31010 will listen for a command/data pair to be transmitted for the 6 ms after the de-assertion of its internal Power-On Reset (POR). If a transmission is not received within this time frame, then it will transition to Normal Operation Mode (NOM). In NOM, it will output bridge data in 0 to 1 V analog, rail-to-rail ratiometric analog output, or digital output, depending on how the part is currently configured.

If the ZSC31010 receives a Start CM command within the first 6 ms after the de-assertion of POR, then it will go into Command Mode (CM). In this mode, calibration/configuration commands will be executed. The ZSC31010 will acknowledge successful execution of commands by transmission of an A5$_H$. The calibrating/ configuring master will know that a command was not successfully executed if no response is received after 130 ms of issuing the command. Once in command interpreting/executing mode, the ZSC31010 will stay in this mode until power is removed, or a Start NOM (Start Normal Operation Mode) command is received. The Start CM command is used as an interlock mechanism, to prevent a spurious entry into command mode on power-up. The first command received within the 6 ms window of POR must be a Start CM command to enter into command interpreting mode. Any other commands will be ignored.

3.3. Command/Data Bytes Encoding

The 16-bit command/data stream sent to the ZSC31010 can be broken into 2 bytes, shown in Table 3.4. The most significant byte encodes the command byte. The least significant byte represents the data byte.

Table 3.4   Command/Data Bytes Encoding

Command Byte	Data Byte	Description
00$_H$	XX$_H$	Read EEPROM command via Sig™ pin; for more details, refer to section 3.7.
20$_H$	5X$_H$	Enter Test Mode (subset of Command Mode for test purposes only): Sig™ pin will assume the value of different internal test points depending on the most significant nibble of data sent. DAC Ramp Test Mode. Gain_B[13:3] contains the starting point, and the increment is (Offset_B/8). The increment will be added every 125 µsec.
30$_H$	*dd*$_H$	Trim/Configure: higher nibble of data byte determines what is trimmed/configured. Lower nibble is data to be programmed. See Table 3.5 for configuration details of data byte *dd*$_H$.
40H	00$_H$	Start NOM => Ends Command Mode, transition to Normal Operation Mode
	10$_H$	Start Raw Mode (RM) In this mode, if Gain_B = 800$_H$ and Gain_T = 80$_H$, then the digital output will simply be the raw values of the ADC for the Bridge reading and the PTAT conversion.
50$_H$	XX$_H$	Start_CM => Start the Command Mode; used to enter command interpret mode
60$_H$	*dd*$_H$	Program SOT (2nd order term)
70$_H$	*dd*$_H$	Program T$_{SETL}$
80$_H$	*dd*$_H$	Program Gain_B, upper 7 bits (set MSB of *dd*$_H$ to 0$_B$)
90$_H$	*dd*$_H$	Program Gain_B, lower 8 bits
A0$_H$	*dd*$_H$	Program Offset_B, upper 6 bits (set the two MSBs of *dd*$_H$ to 00$_B$)
B0$_H$	*dd*$_H$	Program Offset_B, lower 8 bits
C0$_H$	*dd*$_H$	Program Gain_T
D0$_H$	*dd*$_H$	Program Offset_T

Command Byte	Data Byte	Description
E0$_H$	dd_H	Program Tco
F0$_H$	dd_H	Program Tcg

Table 3.5   Programming Details for Command 30$_H$

3rd Nibble	4th Nibble	Description
0$_H$	$Xbbb_B$	Trim oscillator; only least significant 3 bits of data used ($Xbbb_B$).
1$_H$	$bbbb_B$	Trim 1 V reference; least significant 4 bits of data used ($bbbb_B$).
2$_H$	$XXbb_B$	Offset Mode; only least significant 2 bits of data used ($XXbb_B$).
3$_H$	$XXbb_B$	Set output mode; only least significant 2 bits of data used ($XXbb_B$).
4$_H$	$XXbb_B$	Set update rate; only least significant 2 bits of data used ($XXbb_B$).
5$_H$	$bbbb_B$	Configure JFET regulation
6$_H$	$bbbb_B$	Program the Tc_cfg register.
7$_H$	$bbbb_B$	Program bits [99:96] of EEPROM. (SOT_cfg, Pamp_Gain)

3.4.   Calibration Sequence

Although the ZSC31010 can function with many different types of resistive bridges, assume it is connected to a pressure bridge for the following calibration example.

In this case, calibration essentially involves collecting raw bridge and temperature data from the ZSC31010 for different known pressures and temperatures. This raw data can then be processed by the calibration master (the PC), and the calculated coefficients can then be written to the EEPROM of the ZSC31010.

IDT can provide software and hardware with samples to perform the calibration.

There are three main steps to calibration:

1. Assigning a unique identification to the ZSC31010. This identification is programmed into the EEPROM and can be used as an index into the database stored on the calibration PC. This database will contain all the raw values of bridge readings and temperature reading for that part, as well as the known pressure and temperature the bridge was exposed to. This unique identification can be stored in a combination of the following EEPROM registers: T$_{SETL}$, Tcg, Tco. These registers will be overwritten at the end of the calibration process, so this unique identification is not a permanent serial number.

2. Data collection. Data collection involves getting raw data from the bridge at different known pressures and temperatures. This data is then stored on the calibration PC using the unique identification of the IC as the index to the database.

3. Coefficient calculation and write. Once enough data points have been collected to calculate all the desired coefficients, then the coefficients can be calculated by the calibrating PC and written to the IC.