Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Brief Description

The ZSC31014 is a CMOS integrated circuit for highly accurate amplification and analog-to-digital conversion of differential and half-bridge input signals. The ZSC31014 can compensate the measured signal for offset, 1st and 2nd order span, and 1st and 2nd order temperature (Tco and Tcg). It is well suited for sensor-specific correction of bridge sensors. Digital compensation of signal offset, sensitivity, temperature drift, and non-linearity is accomplished via an internal digital signal processor running a correction algorithm with calibration coefficients stored in a non-volatile EEPROM.

The ZSC31014 is adjustable to nearly all piezoresistive bridge sensors. Measured and corrected bridge values are provided at digital output pins, which can be configured as I²C™* or SPI. The digital I²C™ interface can be used for a simple PC-controlled calibration procedure to program calibration coefficients into an on-chip EEPROM. The calibrated ZSC31014 and a specific sensor are mated digitally: fast, precise, and without the cost overhead associated with trimming by external devices or laser trimming.

The ZSC31014's integrated diagnostics functions are well suited for safety-critical applications.

Features

- High accuracy (±0.1% FSO @ -25 to +85°C; ±0.25% FSO @ -40 to +125°C)
- 2nd order charge-balancing analog-to-digital converter provides low noise, 14-bit data at sample rates exceeding 2kHz
- Fast power-up to data output response: 3ms at 4MHz
- Digital compensation of sensor offset, sensitivity, temperature drift, and non-linearity
- Eight programmable analog gain settings combine with a digital gain term; accommodates bridges with spans <1mV/V and high offset
- Internal temperature compensation for sensor correction and for corrected temperature output
- 48-bit customer ID field for module traceability

* I²C™ is a trademark of NXP.

Benefits

- Simple PC-controlled configuration and single-pass digital calibration via I²C™ interface – quick and precise; SPI option for measurement mode
- Eliminates need for external trimming components
- On-chip diagnostic features add safety to the application (e.g., EEPROM signature, bridge connection checks, bridge short detection).
- Low-power Sleep Mode lengthens battery life
- Enables multiple sensor networks

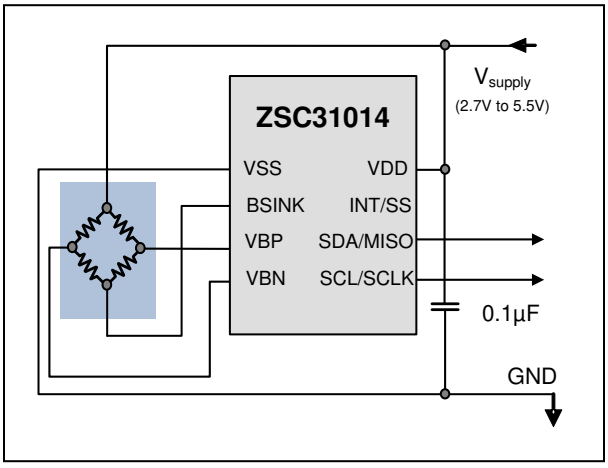
Available Support

- Evaluation Kit
- Application Notes
- Mass Calibration Solution

Physical Characteristics

- Wide supply voltage capability: 2.7V to 5.5V
- Current consumption as low as 70µA depending on programmed sample rate
- Low-power Sleep Mode (<2µA @ 25°C)
- Operation temperature: -40°C to +125°C
- Small SOP8 package

ZSC31014 Application: I²C™ Interface, Low-Power Bsink Option, Internal Temperature Correction



ZSC31014 Block Diagram

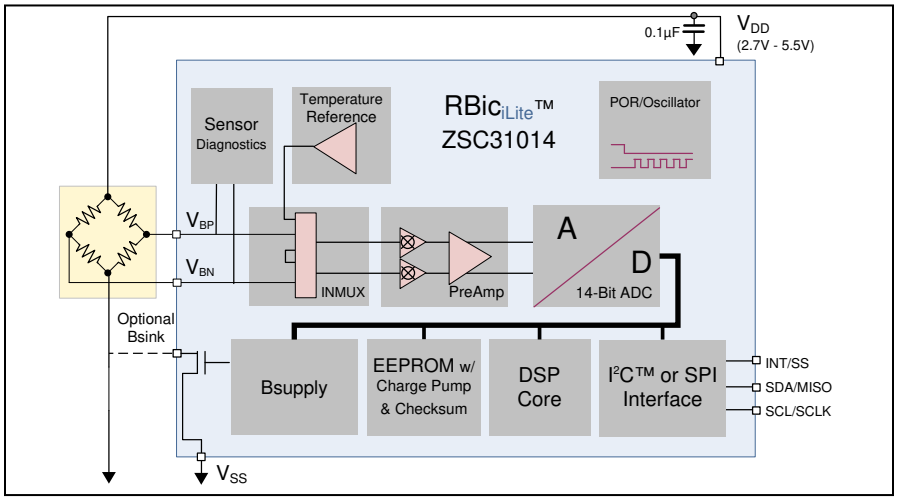
Applications:

Industrial: building automation, data loggers, pressure meters, leak detection monitoring

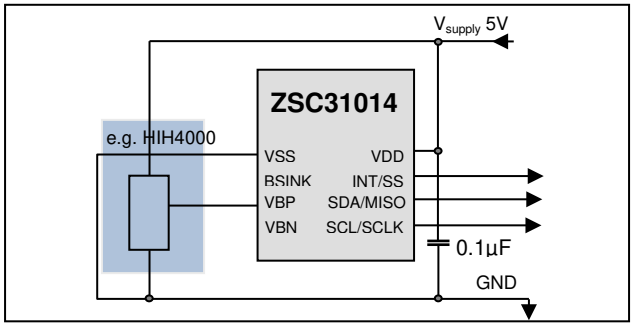
Medical: infusion pumps, blood pressure meters, air mattresses, apnea monitors

White Goods / Appliances: fluid level, refrigerant

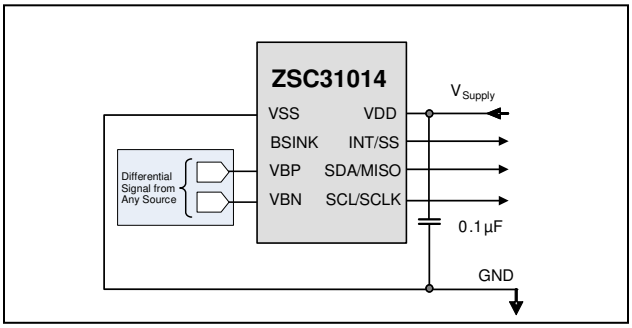
Consumer: body monitors, portable monitors, desktop weather stations, bathroom scales, toys/games



Application: *Half-Bridge Voltage Measurement*



Application: *Generic Differential A2D Converter*



Ordering Examples *(Refer to section 10 in the data sheet for additional options.)*

Sales Code	Description	Package
ZSC31014EAB	ZSC31014 Die — Temperature range: -40°C to +125°C	Unsawn on Wafer
ZSC31014EAC	ZSC31014 Die — Temperature range: -40°C to +125°C	Sawn on Wafer Frame
ZSC31014EAG1	ZSC31014 SOP8 (150 mil) — Temperature range: -40° to +125°C	Tube: add "-T" to sales code / Reel: add "-R"
ZSC31014KIT	ZSC31014 SSC Evaluation Kit: Communication Board, SSC Board, Sensor Replacement Board, USB Cable, 5 IC Samples (software can downloaded on www.IDT.com/ZSC31014)	

Corporate Headquarters
6024 Silver Creek Valley Road
San Jose, CA 95138
www.IDT.com

Sales
1-800-345-7015 or 408-284-8200
Fax: 408-284-2775
www.IDT.com/go/sales

Tech Support
www.IDT.com/go/support

Contents

List of Figures

List of Tables

1 IC Characteristics

1.1. Absolute Maximum Ratings

Table 1.1 ZSC31014 Maximum Ratings

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Analog Supply Voltage	V_{DD}	-0.3		6.0	V
Voltages at Digital and Analog I/O – In Pin	V_{INA}	-0.3		V_{DD}+0.3	V
Voltages at Digital and Analog I/O – Out Pin	V_{OUTA}	-0.3		V_{DD}+0.3	V
Storage Temperature Range (≥10 hours)	T_{STOR}	-50		150	°C
Storage Temperature Range (<10 hours)	$T_{STOR<10h}$	-50		170	°C

Note: Also see Table 6.1 regarding soldering temperature and storage conditions for the SOP-8 package.

1.2. Recommended Operating Conditions

Table 1.2 ZSC31014 Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Analog Supply Voltage to Gnd	V_{DD}	2.7		5.5	V
Ambient Temperature Range [1)]	T_{AMB}	-40		125	°C
CM Voltage Range [2)]	V_{IN}	1		V_{DD} -1.2	V
External Capacitance between V_{DD} and Gnd	C_{VDD}	100	220	470	nF
Pull-up on SDA and SCL	R_{PU}	1			kΩ
Bridge Resistance	R_{BR}	0.2		100	kΩ

1) If buying die, designers should use caution not to exceed maximum junction temperature by proper package selection.

2) Both BP and BN input voltage must be within the specified range. In Half-Bridge Mode, this requirement applies only to the BP input (gain 1.5 and 3). In this mode, BN is connected internally to VDD/2.

1.3. Electrical Parameters

Note: See important notes at the end of the table.

Table 1.3 ZSC31014 Electrical Parameters

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY						
Update Mode Supply Current (See section 1.4.1)	I_{DD}	At minimum update rate (1MHz clock)	70	120		µA
		At maximum update rate (4MHz clock). See section 3.1.1 for more details. Minimum current is achieved at slow update rates.		2000	2500	
Sleep Mode Supply Current (See section 1.4.2)	I_{sndby}	-40°C to +85°C		0.5	5	µA
		-40°C to +125°C		0.5	32	µA
Power-On-Reset Level	POR		1.8		2.5	V
ANALOG FRONT END (AFE)						
Leakage Current Pins VBP,VBN	I_{IN_LEAK}	Sensor connection and short checks must be disabled.			±20	nA
EEPROM						
Number of Erase/Write Cycles	n_{WRI_EEP}	At 85°C			100k	Cycles
Data Retention	t_{WRI_EEP}	At 100°C			10	Years
ANALOG-TO-DIGITAL CONVERTER (ADC)						
Resolution	r_{ADC}			14		Bits
Temperature Resolution					11	Bits
Integral Nonlinearity (INL) [1]	INL_{ADC}	Based on ideal slope	-4		+4	LSB
Differential Nonlinearity [2] (DNL)	DNL_{ADC}		-1		+1	LSB
I²C™ INTERFACE & SPI INTERFACE						
Input Low Level	V_{IN_low}	SDA/MISO and SCL/SCLK	0		0.2	V_{DD}
Input High Level	V_{IN_high}	SDA/MISO and SCL/SCLK	0.8		1	V_{DD}
Input leakage to V_{SS}	I_{il}	SDA/MISO, SCL/SCLK, and INT/SS with output disabled	-1.0		+1.0	µa
Input leakage to V_{DD}	I_{ih}	SDA/MISO and INT/SS with output disabled	-1.0		+1.0	µa
	I_{ih_PU}	SCL/SCLK with weak pull-up		-1.2	-5	µa
Output Sourcing Current	$I_{OH\_SDA/MISO}$	SDA/MISO @V_{OH} = V_{DD} -0.2v	-1.9	-3.1	-4.8	mA
	$I_{OH\_INT/SS}$	INT/SS @V_{OH}= V_{DD} -0.2v	-0.63	-1.2	-1.9	mA

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Sink Current	$I_{OL\_SDA/MISO}$	SDA/MISO @V_{OI} = 0.2v	2.3	3.9	6.2	mA
	$I_{OL\_INT/SS}$	INT/SS @V_{OI}= 0.2v	0.85	1.7	3.0	mA
Load Capacitance at SDA	C_{SDA}	@ 400kHz			200	pF
Pull-up Resistor	R_{I2C_PU}		500			Ω
Input Capacitance (each pin)	C_{I2C_IN}				10	pF
TOTAL SYSTEM						
Frequency Variation	f_{var}	All timing in the specification is subject to this variation.			±15	%
Start-Up-Time [3), 4), 5)] (Power-up to data ready)	t_{STA}	@ 4MHz(EEPROM locked) @ 4MHz(EEPROM unlocked)		2.8 7.3	3.2 8.4	ms
		@ 1MHz(EEPROM locked) @ 1MHz(EEPROM unlocked)		6.0 10.4	6.9 12	
Response Time [3), 4), 5)] (Time to data ready)	f_{meas}	@ 4MHz		0.5		ms
		@ 1MHz		1.6		
Overall Linearity Error [6), 7), 8)]	E_{LIND}	Within 5% to 95% of full-scale differential input.			±0.05	%FSO
Overall Ratiometricity Error [6), 9)]	RE_{out}	VDD ± 10%		±0.025	±0.1	%FSO
Overall Absolute Error [6), 10)]	AC_{out}	-25°C to +85°C, VDD ± 10%			±0.1	%FSO
		-40°C to +125°C, VDD ± 10%			±0.25	%FSO

1) Measured at highest PreAmp_Gain setting and -1/2 to 1/2 A2D_Offset setting.
2) Parameter not tested during production test but guaranteed by design.
3) In Update Rate Mode at fastest update rate.
4) See section 3.1 for more details.
5) Parameter indirectly tested during production test.
6) Bridge input to digital output.
7) For applications where Vdd <3.5V using A2D offsets 15/16, 7/8, 1/8, or 1/16, a slight overall linearity improvement of 0.015% FSO can be achieved.
8) FSO = percent full-scale output.
9) For high preamp gain (≥96) in conjunction with high clock frequency and normal integration (4MHz, longInt=0), the ratiometricity error can be ≤0.3%.
10) For applications requiring high preamp gain (≥96) in conjunction with a high clock frequency (4 MHz), calibration using three temperature points is required in order to achieve the specified “Overall Absolute Error.” If calibration is performed using only two temperature points, the specified maximum error values must be increased by a factor of 3. A calibration using only one temperature point is not recommended for applications with high preamp gain (≥96) in conjunction with a high clock frequency (4 MHz).

1.4. Current Consumption

1.4.1. Update Mode Current Consumption

Figure 1.1 Update Mode Current Consumption with Minimum Update Rate

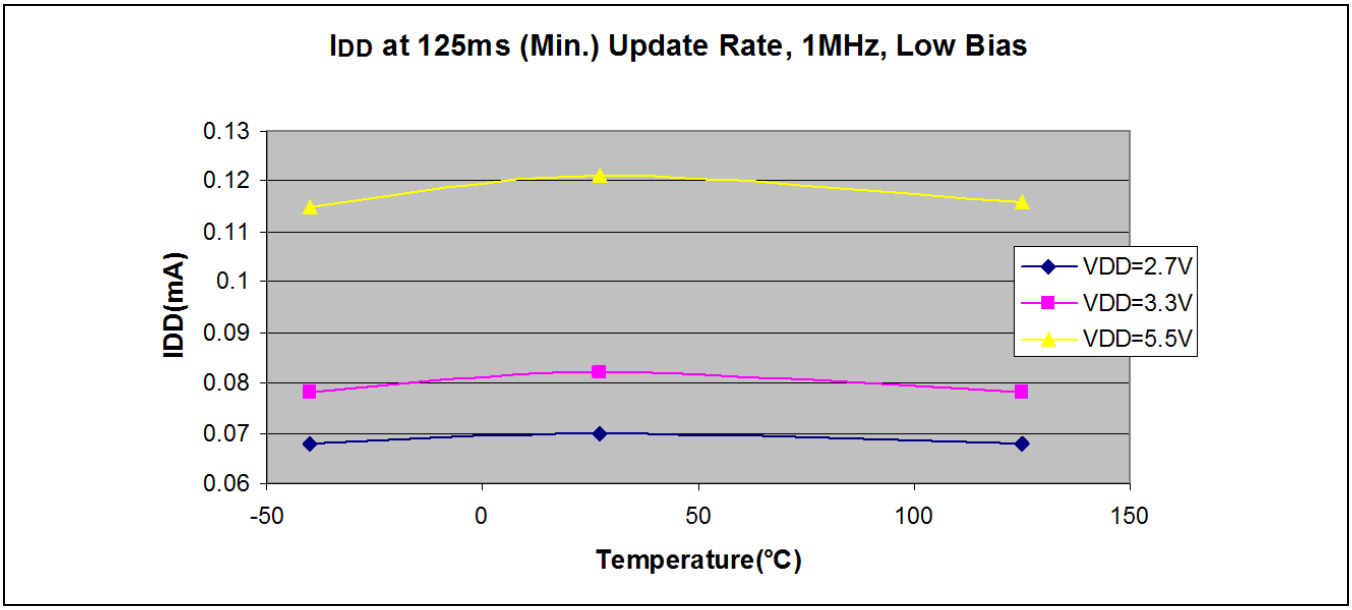
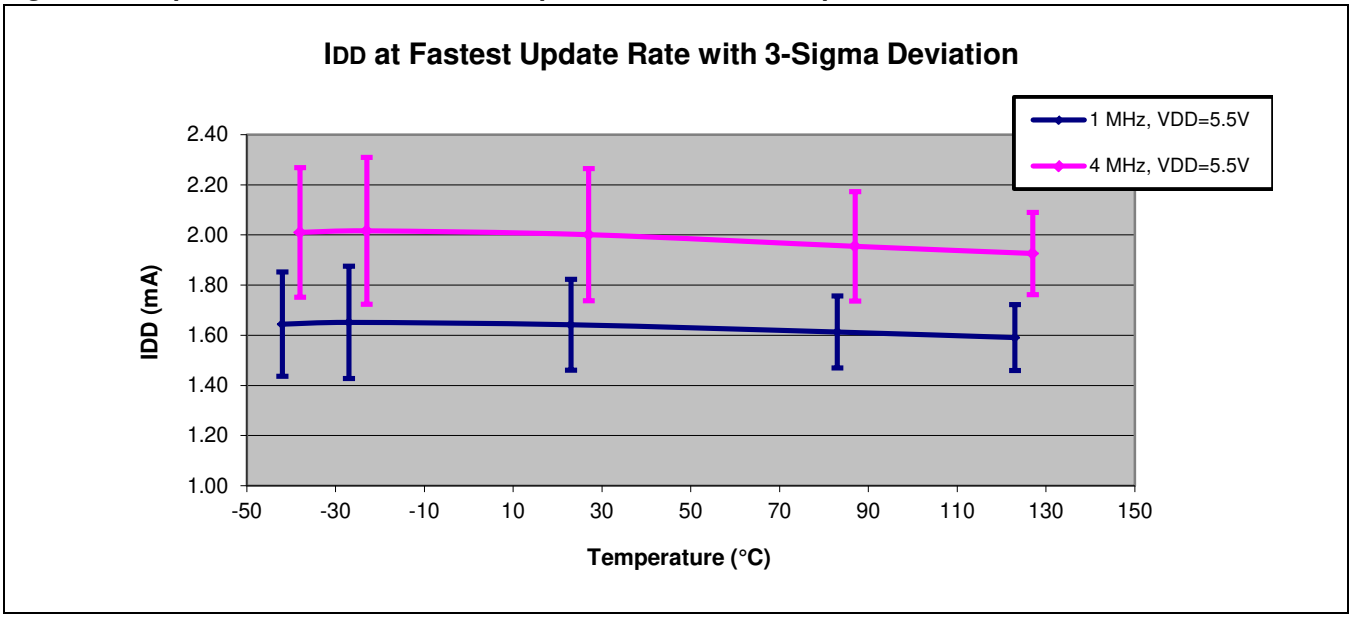
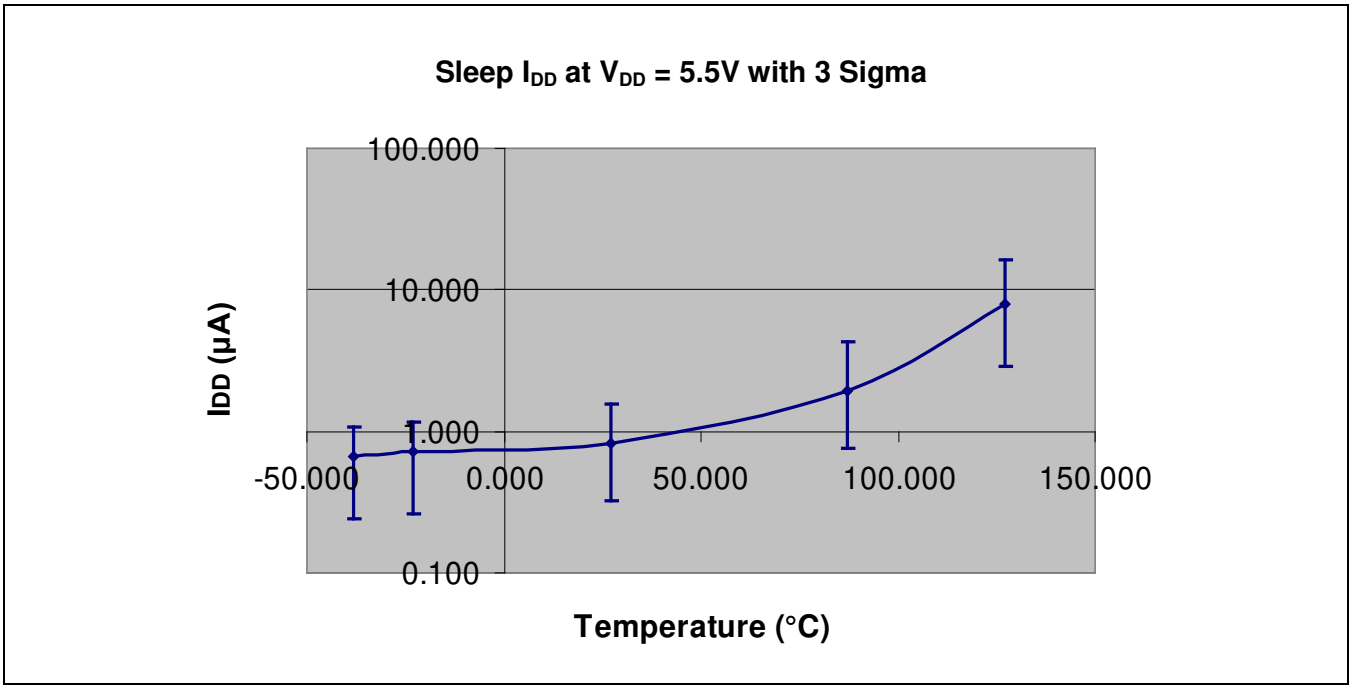


Figure 1.2 Update Mode Current Consumption with Maximum Update Rate



1.4.2. Sleep Mode Current Consumption

Figure 1.3 Sleep Mode Current Consumption



1.5. Analog Input versus Output Resolution

The ZSC31014 has a fully differential chopper-stabilized preamplifier with 8 programmable gain settings through a 14-bit analog-to-digital converter (ADC). The resolution of the output depends on the input span (bridge sensitivity) and the analog gain setting programmed. Analog gains available are 1.5, 3, 6, 12, 24, 48, 96, and 192. *

Table 1.4 gives the guaranteed minimum resolution for a given bridge sensitivity range for the eight analog gain settings. At higher analog gain settings, there will be higher output resolution, but the ability of the ASIC to handle large offsets decreases. This is expected because the offset is also amplified by the analog gain and can therefore saturate the ADC input.

* For previous silicon revision A, the available analog gain settings are 1, 3, 5, 15, 24, 40, 72, and 120. See *ZSC31014_AFE_Settings.xls* for table values for revision A.

Table 1.4 Minimum Guaranteed Resolution for the Analog Gain Settings

Analog Gain = 1.5				
Input Span (mV/V)			Allowed Offset (mV/V)	Min. Guaranteed Resolution (Bits)
Min	Typ	Max		
289	400	529	69	12.7
235	325	430	118	12.4
181	250	331	168	12.1
126	175	231	218	11.6
90	125	165	251	11.1
54	75	99	284	10.3
43	60	79	294	10.0

Analog Gain = 3				
Input Span (mV/V)			Allowed Offset (mV/V)	Min. Guaranteed Resolution (Bits)
Min	Typ	Max		
145	200	265	34	12.7
123	170	225	54	12.5
101	140	185	74	12.2
80	110	145	94	11.9
58	80	106	114	11.4
36	50	66	134	10.7
22	30	40	147	10.0

Analog Gain = 6				
Input Span (mV/V)			Allowed Offset (mV/V)	Min. Guaranteed Resolution (Bits)
Min	Typ	Max		
65	90	119	24	12.6
61	85	112	27	12.5
51	70	93	37	12.2
43	60	79	44	12.0
40	55	73	47	11.9
36	50	66	50	11.7
29	40	53	57	11.4

Analog Gain = 12				
Input Span (mV/V)			Allowed Offset (mV/V)	Min. Guaranteed Resolution (Bits)
Min	Typ	Max		
36	50	66	9	12.7
30	42	56	14	12.5
25	34	45	19	12.2
19	26	34	24	11.8
13	18	24	30	11.3
7	10	13	35	10.4
6	8	11	36	10.1

Analog Gain = 24				
Input Span (mV/V)			Allowed Offset (mV/V)	Min. Guaranteed Resolution (Bits)
Min	Typ	Max		
18.1	25.0	33.1	4.3	12.7
15.2	21.0	27.8	6.9	12.5
12.3	17.0	22.5	9.6	12.2
9.4	13.0	17.2	12.2	11.8
6.5	9.0	11.9	14.9	11.3
3.6	5.0	6.6	17.5	10.4
2.9	4.0	5.3	18.2	10.1

Analog Gain = 48				
Input Span (mV/V)			Allowed Offset (mV/V)	Min. Guaranteed Resolution (Bits)
Min	Typ	Max		
8.7	12.0	15.9	0.4	12.7
7.2	10.0	13.2	1.7	12.4
5.8	8.0	10.6	2.9	12.1
4.3	6.0	7.9	4.2	11.7
2.9	4.0	5.3	5.4	11.1
2.2	3.0	4.0	6.7	10.7
1.4	2.0	2.6	7.3	10.1

Analog Gain = 96				
Input Span (mV/V)			Allowed Offset (mV/V)	Min. Guaranteed Resolution (Bits)
Min	Typ	Max		
4.3	6.0	7.9	1.2	12.7
2.9	4.0	5.3	2.6	12.1
1.8	2.5	3.3	3.6	11.4
1.4	2.0	2.6	3.9	11.1
1.2	1.6	2.1	4.2	10.8
0.9	1.3	1.7	4.3	10.5
0.7	1.0	1.3	4.5	10.1

Analog Gain = 192				
Input Span (mV/V)			Allowed Offset (mV/V)	Min. Guaranteed Resolution (Bits)
Min	Typ	Max		
1.81	2.50	3.31	1.0	12.4
1.45	2.00	2.65	1.3	12.1
1.08	1.50	1.98	1.6	11.7
0.90	1.25	1.65	1.8	11.4
0.72	1.00	1.32	1.9	11.1
0.51	0.70	0.93	2.1	10.6
0.36	0.50	0.66	2.3	10.1

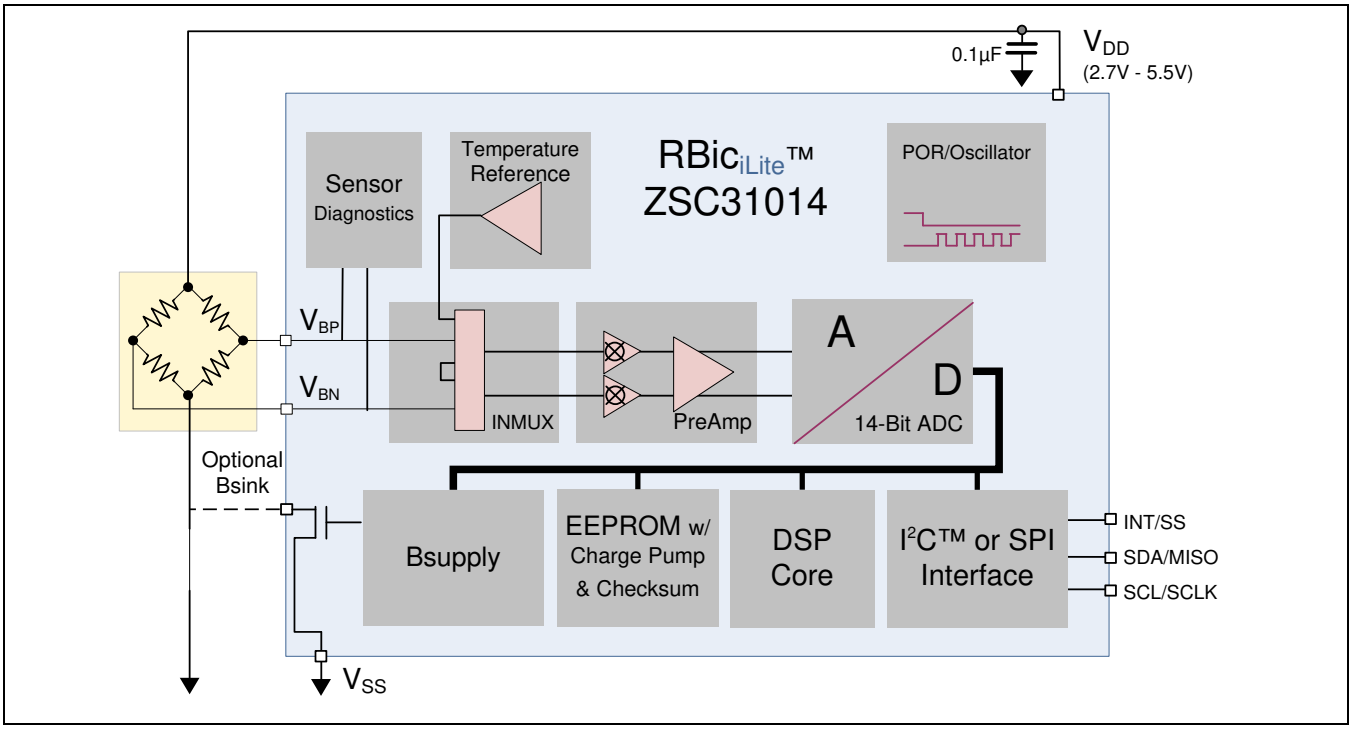
2 Circuit Description

2.1. Signal Flow and Block Diagram

The ZSC31014 uses a charge-balancing ADC that provides low noise 14-bit samples. The system clock can operate at 1MHz (lower power, better noise performance) or 4MHz (faster sample rates). The PreAmp nulls its offset over temperature and offers a wide range of selectable analog gain settings. The on-chip digital signal processor (DSP) core uses coefficients stored in EEPROM to precisely calibrate/condition the amplified differential input signal. Temperature can be measured from an internal temperature sensor, which can be calibrated and output as well as used to compensate for temperature effects of the sensor bridge.

Direct interfacing to µP controllers is facilitated via I²C™ digital protocol or optional SPI. I²C™ is used as the calibration interface and can be used in the final application. SPI is only supported for end applications.

Figure 2.1 ZSC31014 Block Diagram



2.2. Analog Front End

2.2.1. Preamplifier (PreAmp)

The preamplifier has a chopper-stabilized two-stage design. The first stage instrumentation-type amplifier has an internal auto-zero (AZ) function in order to prevent the second stage from being overdriven by the amplified offset. The overall chopper guarantees that the whole PreAmp has negligible offset.

There are eight analog gain settings selectable in EEPROM. The polarity of the gain can be changed by shifting the chopper phase between input and output by 180 degrees via the EEPROM setting Gain_Polarity. Changing the polarity can help prevent board layout crossings in cases where the sensor chip layout does not match the ZSC31014 pad/pin layout.

PreAmp_Gain for the bridge measurement is controlled by bits [6:4] in EEPROM Word $0F_{HEX}$ (B_Config register). PreAmp_Gain for temperature is set by bits [6:4] in Word 10_{HEX} (T_Config register). These 3 bits are referred to as [G2:G0]. See section 2.2.3 for recommended temperature measurements settings.

Table 2.1 Preamplifier Gain Control Signals [†]

G2	G1	G0	PreAmp_Gain
0	0	0	1.5
1	0	0	3
0	0	1	6
1	0	1	12
0	1	0	24
1	1	0	48
0	1	1	96
1	1	1	192

Gain Polarity for the bridge is controlled by bit [7] (Gain_Polarity) in the B_Config register.

Table 2.2 Gain Polarity Control Signal

Gain_Polarity	Overall Gain
0	(-1) ∗ GAIN
1	(+1) ∗ GAIN

[†] For previous silicon revision A, the available analog gain settings are 1 (G2:G0=000); 3 (G2:G0=100); 5 (G2:G0=001); 15 (G2:G0=101); 24 (G2:G0=010); 40 (G2:G0=011); 72 (G2:G0=110); and 120 (G2:G0=111).

Before a measurement conversion is started, the PreAmp has a phase called nulling. During the nulling phase, the PreAmp measures its internal offset so that it can be removed during the measurement. It is especially useful at higher gains where a small offset could cause the PreAmp to saturate. If bit[12] of the configuration register is set to one, then the nulling feature is disabled as shown in Table 2.3. At lower PreAmp gains, nulling can adversely affect the linearity and ratiometricity of the part, so the recommended setting for this bit is zero for gains of 6 or higher and one for all other gains.

Table 2.3 Disable Nulling Control Signal

Disable_Nulling	Effect
0	Nulling is on
1	Nulling is off

2.2.2. Analog-to-Digital Converter

A 14-bit 2nd order charge-balancing analog-to-digital converter (ADC, A2D) is used to convert signals coming from the PreAmp. By default, each conversion is split into a 9-bit coarse conversion and a 5-bit fine conversion. During the coarse conversion, the amplified signal is integrated (averaged). One coarse conversion covers exactly 4 chopper periods of the PreAmp. A configurable setting stored in EEPROM allows quadrupling the period of the coarse conversion. In Table 3.7, see the LongInt bit in EEPROM words B_Config ($0F_{HEX}$) and T_Config (10_{HEX}). When LongInt = 1, the conversion is performed as 11 bits coarse + 3 bits fine. The advantage of this mode is more noise suppression; however, sampling rates will fall significantly because A2D conversion periods are quadrupled.

An auto-zero (AZ) measurement is performed periodically and subtracted from all ADC results used in calculations. This compensates for any drift of offset vs. temperature. The ADC uses switched capacitor technique and complete full-differential architecture to increase its stability and noise immunity.

Part of the switched capacitor network is a 4-bit digital-to-analog conversion (DAC) function, which allows adding or subtracting a defined offset value resulting in an A2D_Offset shift. This allows for a rough compensation of the bridge offset, which allows a higher PreAmp_Gain to be used and consequently more end resolution of the measured signal. Table 2.4 shows the A2D_Offset adjustment. Using this function, the ADC input range can be shifted in order to optimize the coverage of the sensor signal and sensor offset values as large as the sensor span can be processed without losing resolution.

The A2D_Offset setting for the bridge is controlled by bits [3:0] in Word $0F_{HEX}$ (B_Config). These 4 bits are referred to as [Z3:Z0]. Note: To collect uncalibrated raw bridge values from the ADC, the Offset_B coefficient must be programmed as shown in Table 2.4. Note: The ADC offset for the internal temperature measurement is trimmed at production test to avoid saturation and the setting, which is stored in bits [3:0] in word 10_{HEX} (T_Config), should not be changed (see Table 3.7).

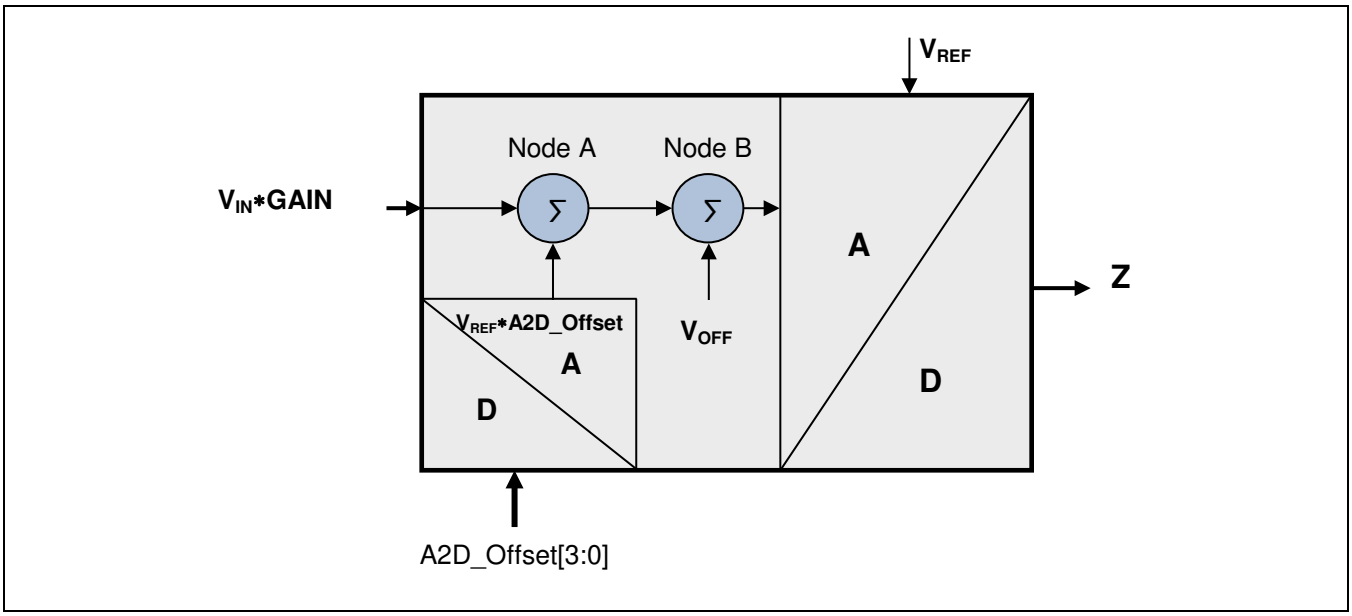
Table 2.4 A2D_Offset Signals

A2D_Offset[3:0]	Auto-Zero Output Count of A2D (+/- 250 Codes)	A2D Input Range [VREF]	A2D_Offset	Offset_B[15:0]
F_{HEX}	15360	-15/16 to 1/16	15/16	$1C00_{HEX}$
E_{HEX}	14336	-7/8 to 1/8	7/8	1800_{HEX}
D_{HEX}	13312	-13/16 to 3/16	13/16	1400_{HEX}
C_{HEX}	12288	-3/4 to 1/4	3/4	1000_{HEX}
B_{HEX}	11264	-11/16 to 5/16	11/16	$0C00_{HEX}$
A_{HEX}	10240	-5/8 to 3/8	5/8	0800_{HEX}
9_{HEX}	9216	-9/16 to 7/16	9/16	0400_{HEX}
8_{HEX}	8192	-1/2 to 1/2	1/2	0000_{HEX}
7_{HEX}	7168	-7/16 to 9/16	7/16	$FC00_{HEX}$
6_{HEX}	6144	-3/8 to 5/8	3/8	$F800_{HEX}$
5_{HEX}	5120	-5/16 to 11/16	5/16	$F400_{HEX}$
4_{HEX}	4096	-1/4 to 3/4	1/4	$F000_{HEX}$
3_{HEX}	3072	-3/16 to 13/16	3/16	$EC00_{HEX}$
2_{HEX}	2048	-1/8 to 7/8	1/8	$E800_{HEX}$
1_{HEX}	1024	-1/16 to 15/16	1/16	$E400_{HEX}$
0_{HEX} 1)	0	0 to 16/16	0	$E000_{HEX}$

1) A setting of 0000_{BIN} for the A2D offset can only be used for internal temperature measurements, which are factory-trimmed (do not change default setting). If it is used for bridge measurements, it could lead to the auto-zero saturating, which results in poor performance of the IC.

Figure 2.2 shows a functional diagram of the ADC. The A/D block at the right side is assumed to be an ideal differential ADC. The summing node B models the offset voltage, which is caused by the tolerance of process parameters and other influences including temperature and changes of power supply. The summing node A adds a voltage, which is controlled by the digital input A2D_Offset. This internal digital-to-analog converter (DAC, D2A) uses binary-weighted capacitors, which are part of the switched capacitor network of the ADC. This DAC function allows optimal adjustment of the input voltage range of the ADC to the amplified output voltage range of the sensor. All signals in this diagram are shown as single-ended for simplicity in understanding the concept; all signals are actually differential. An auto-zero reading is accomplished by short-circuiting the differential ADC input.

Figure 2.2 Functional Diagram of the ADC



Digital representation of the input voltage as a signed number requires calculating the difference Z_{SENSOR} - $Z_{AUTOZERO}$.

$$Z_{SENSOR} = 2^{14} * (GAIN * V_{IN} / V_{DD} + A2D\_Offset + V_{OFF} / V_{REF}) \quad (1)$$

$$Z_{AUTOZERO} = 2^{14} * (A2D\_Offset + V_{OFF} / V_{REF}) \quad (2)$$

where

GAIN PreAmp_Gain (B_Config bits [6:4] for bridge measurement; fixed value 6 for temperature measurement) (See Table 2.1)

A2D_Offset Zero Shift of ADC (B_Config or T_Config bits [3:0]) (See Table 2.4)

V_{REF} ~ V_{DD} Supply Voltage to ZSC31014

V_{IN} Input Voltage = (V_{BP}-V_{BN}) in differential mode;
= (V_{BP}-V_{DD}/2) in half-bridge mode

V_{OFF} Small random offset voltage that varies part-to-part and with temperature. The periodic auto-zero cycle will subtract this error.

The digital output Z as a function of the analog input of the analog front-end (including the PreAmp) can be described as

$$Z = Z_{SENSOR} - Z_{AUTOZERO}$$

$$Z = 2^{14} * (GAIN * V_{IN} / V_{REF}) \quad (3)$$

With $V_{REF} = V_{DD} - V_{BSink}$ (see section 2.2.4) where V_{BSink} is the voltage at the BSINK pin.

2.2.3. Temperature Measurement

The temperature signal comes from an internal measurement of the die temperature. The temperature signal is generated from a bridge-type sensor using resistors with different TC values. Table 2.5 shows the characteristic parameters. This temperature signal can be corrected with offset, span, and 2nd order non-linearity coefficients. The corrected temperature can then be read on the digital output I²C™ or SPI with either an 8 or 11 bit resolution. The raw temperature reading can also be used to compensate the sensor bridge reading. 1st order Tco and Tcg, and 2nd order Tco and Tcg coefficients are available to correct sensor bridge offset and span variations with temperature.

Table 2.5 Parameters of the Internal Temperature Sensor Bridge

Parameter	Min	Typ	Max	Units
Sensitivity	0.28	0.38	0.5	mV/V/K
Offset voltage	-75		65	mV/V
Nonlinearity (-20 to 80°C) first order fit			2	°C
Nonlinearity (-20 to 80°C) second-order fit			0.25	°C
Bridge resistance	15	20	25	kΩ

NOTE: The T_CONFIG register description is given in section 2.2.5. Most fields within this EEPROM register are programmed to default settings on the production test and should not be changed. Only the LongInt field (bit 8) setting is user-selectable if desired. Other settings for the remaining T_Config bits might cause temperature measurements to saturate. Section 2.2.5 gives the details of how PreAmp_Gain and A2D_Offset Mode are configured for temperature measurements.

ZSC31014 on-chip temperature sensor is calibrated by IDT using three temperature points: -40°C, room temperature (RT), and +125°C, which provides a 2nd-order fit. The error of the conditioned temperature output data at delivery is specified as ≤ 2.5 Kelvin over the full operational temperature range of -40 to +125°C.

2.2.4. Bridge Supply (Bsink)

The ZSC31014 provides a Bsink (bridge sink) pin to drive the bottom of the sensor bridge. Internal to the ZSC31014, Bsink is driven by a large NMOS pull-down ($R_{DS(ON)}$≈20Ω). There will be some IR drop across this device, but the Bsink node also forms the bottom reference of the ADC. Therefore, any ratiometricity error this IR drop would normally cause is cancelled out.

Bsink is turned on 190µs/50µs (depending on 1MHz or 4MHz clock setting) prior to the start of a conversion to allow settling time for the bridge and the internal front-end (PreAmp and ADC) path. The entire conversion is then performed, and Bsink is then turned off. This can achieve significant power savings when used in conjunction with slower update rates. For example, a 2.5kΩ bridge would consume 2mA with a constant 5V bias. However, if used with the Bsink feature at an update rate of 6.35ms, the same bridge would draw on average only 112µA since it would be biased on only 5.6% of the time. Savings at slower update rates can be even more significant.

2.2.5. Analog Front-End Configuration

As shown in Figure 2.3, the analog front-end (AFE) has much flexibility/configurability in how its measurement is performed. The preferred settings for the AFE configuration are typically different for a bridge reading than for a temperature reading. The EEPROM contains two words for configuring the AFE for each measurement: B_Config ($0F_{HEX}$) and T_Config (10_{HEX}).

Figure 2.3 Format for AFE Configuration Registers B_Config and T_Config

Reserved [2:0]			Disable Nulling	PreAmp_Mux [1:0]		Bsink	Longint	Gain_Polarity	PreAmp_Gain [2:0]			A2D_Offset [3:0]			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

The B_Config register is loaded from EEPROM and written to the AFE configuration register just before a measurement of the bridge begins. The T_Config register is loaded from EEPROM and written to the AFE configuration register immediately before a temperature measurement begins. For more details, refer to Table 3.7, EEPROM words $0F_{HEX}$ (B_Config) and 10_{HEX} (T_Config), in section 3.6. Note: for T_Config, only bit 8 (LongInt) is user-configurable. All other settings are factory programmed and should not be changed.

2.3. Digital Signal Processor

A digital signal processor (DSP) is used for processing the converted differential signal as well as performing temperature correction and computing the temperature value for digital output.

2.3.1. Digital Core

The digital core reads correction coefficients from EEPROM and can correct for the following:

1. Signal offset (Offset_B term)
2. Signal gain (Gain_B term)
3. Temperature coefficient of the bridge offset 1st order (Tco term)
4. Temperature coefficient of the bridge gain 1st order (Tcg term)
5. Second-order non-linearity of signal (SOT_bridge term)
6. Second-order non-linearity of Tco (SOT_tco term)
7. Second-order non-linearity of Tcg (SOT_tcg term)

See sections 3.7 and 3.8 for a full discussion of calibration and correction math.

2.3.2. Normal Operation Mode

Two operation modes are available for normal operation: Update Rate Mode (continuous conversion at a selectable update rate) or Sleep Mode (low power). (See section 3.1.) Both modes can operate in either I²C™ digital output or SPI digital output. These selections are made in configuration registers of the EEPROM.

2.3.3. EEPROM

The EEPROM array contains the calibration coefficients for gain and offset, etc., and the configuration bits, such as output mode, update rate, etc. When programming the EEPROM, an internal charge pump voltage is used; therefore a high voltage supply is not needed. (See section 3.5 for instructions on programming the EEPROM.)

Important: After the ZMDI_Config_1 or ZMDI_Config_2 EEPROM word has been changed, the IC must be power cycled for the changes to be loaded.

The EEPROM array is arranged as twenty 16-bit words. Three words are dedicated to the customer serial number for module traceability. The integrity of the contents of the EEPROM array is ensured by a 16-bit signature word which is checked after each power-on of the device. The signature word is automatically updated whenever the Start_NOM command (starts Normal Operating Mode; see section 3.5) is executed after EEPROM contents have been changed.

After calibration is completed and all coefficients are written to EEPROM, the user can lock the EEPROM so that no further writes can occur (see section 3.6 regarding EEP_Lock, bits [15:13] of EEPROM word 02_{HEX}).

IMPORTANT: Care must be taken when performing this function. After the command to lock EEPROM, the next command *must* be Start_NOM so that the EEPROM checksum is calculated and written. If the part is power cycled instead, the lock will take effect, and the checksum will be wrong. In this case, the part will always output a diagnostic state, and since the EEPROM is permanently locked, it can never be recovered.

2.3.4. Digital Interface – I²C™

The IC can communicate via an addressable two-wire (I²C™) interface. Commands are available for the following:

- Sending calibration commands in Command Mode
- Starting measurements in Sleep Mode
- Reading data

The ZSC31014 uses an I²C™-compatible communication protocol[‡] with support for the bit rates listed in Table 2.6.

Table 2.6 Supported I²C™ Bit Rates

Clock Setting	Bit Rates
4MHz	400kHz or 100kHz
1MHz	100kHz

See section 2.3.6 for clock setting details.

[‡] For more details, refer to http://www.standardics.nxp.com or other websites for this specification.

I²C™ is the protocol used during calibration (Command Mode). The ZSC31014 I²C™ slave address (00_{HEX} to $7F_{HEX}$) is selected by bits [9:3] of EEPROM word 02_{HEX}. If the communication lock pattern Comm_lock (bits [5:3], EEPROM word 02_{HEX}) is programmed to 011, the device will respond only to this address. Otherwise, the device will respond to all I²C™ addresses. The factory setting for I²C™ slave address is 28_{HEX} with Comm_lock set.

When programmed as an I²C™ device, the INT/SS pin operates as an interrupt. The INT pin rises when new output data is ready and falls when the next I²C™ communication occurs. It is most useful if the part is configured in Sleep Mode to indicate to the system that a new conversion is ready.

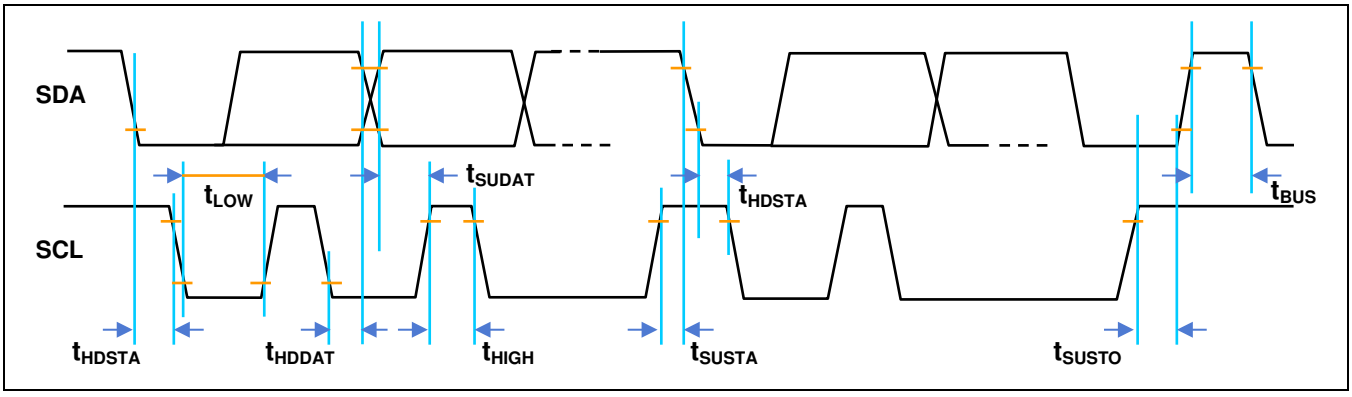
See Figure 2.4 for the I²C™ timing diagram and Table 2.7 for definitions of the parameters shown in the timing diagram.

Table 2.7 I²C™ Parameters

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
SCL clock frequency	f_{SCL}	100		400	kHz
Start condition hold time relative to SCL edge	t_{HDSTA}	0.1			µs
Minimum SCL clock low width [1)]	t_{LOW}	0.6			µs
Minimum SCL clock high width [1)]	t_{HIGH}	0.6			µs
Start condition setup time relative to SCL edge	t_{SUSTA}	0.1			µs
Data hold time on SDA relative to SCL edge	t_{HDDAT}	0			µs
Data setup time on SDA relative to SCL edge	t_{SUDAT}	0.1			µs
Stop condition setup time on SCL	t_{SUSTO}	0.1			µs
Bus free time between stop condition and start condition	t_{BUS}	2			µs

1) Combined low and high widths must equal or exceed minimum SCLK period.

Figure 2.4 I²C™ Timing Diagram



(See section 3.1 for data transmission details.)

Note: There are three differences in the ZSC31014 protocol compared with the original I²C™ protocol:

- Sending a start-stop condition without any transitions on the CLK line (no clock pulses in between) creates a communication error for the next communication, even if the next start condition is correct and the clock pulse is applied. An additional start condition must be sent, which results in restoration of proper communication.
- The restart condition—a falling SDA edge during data transmission when the CLK clock line is still high—creates the same situation. The next communication fails, and an additional start condition must be sent for correct communication.
- A falling SDA edge is not allowed between the start condition and the first rising SCL edge. If using an I²C™ address with the first bit 0, SDA must be held low from the start condition through the first bit.

2.3.5. Digital Interface – SPI

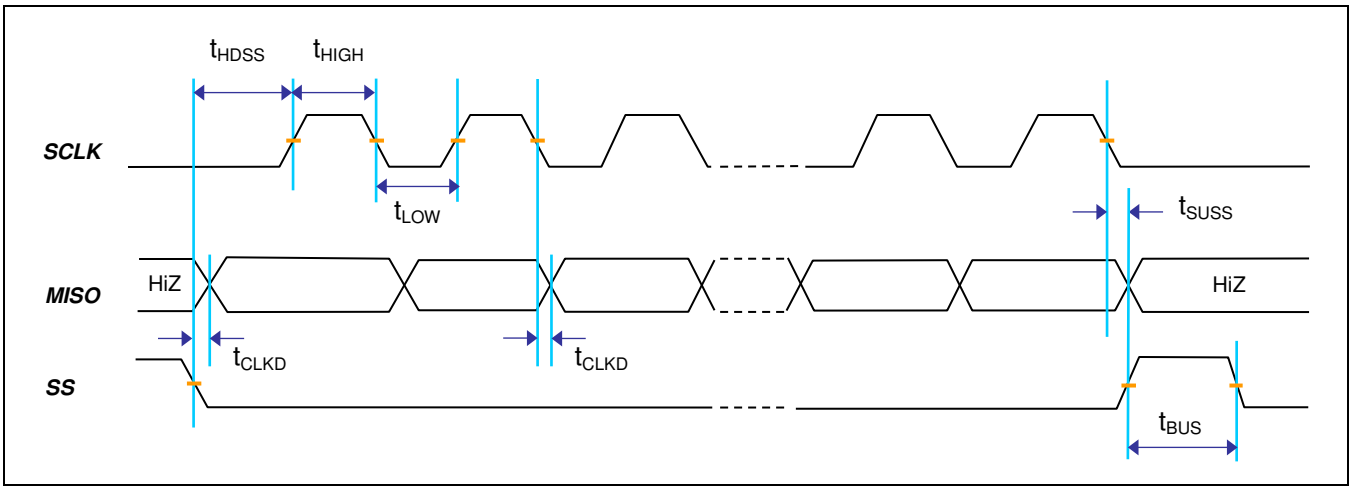
SPI is available only as half duplex (read-only from the ZSC31014). SPI cannot be used in the calibration environment (Command Mode) because it does not support receiving commands. SPI speeds of up to 200kHz can be supported in 1MHz Mode, and up to 800kHz can be supported in 4MHz Mode. See Figure 2.5 for the SPI timing diagram and Table 2.8 for definitions of the parameters shown in the timing diagram.

Table 2.8 SPI Parameters

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
SCLK clock frequency (4MHz clock)	f_{SCL}	50		800	kHz
SCLK clock frequency (1MHz clock)	f_{SCL}	50		200	kHz
SS drop to first clock edge	t_{HDSS}	2.5			µs
Minimum SCLK clock low width [1)]	t_{LOW}	0.6			µs
Minimum SCLK clock high width [1)]	t_{HIGH}	0.6			µs
Clock edge to data transition	t_{CLKD}	0		0.1	µs
Rise of SS relative to last clock edge	t_{SUSS}	0.1			µs
Bus free time between rise and fall of SS	t_{BUS}	2			µs

1) Combined low and high widths must equal or exceed minimum SCLK period.

Figure 2.5 SPI Bus Data Output Timing



(See section 3.1 for data transmission details.)

2.3.6. Clock Generator / Power-On Reset (CLKPOR)

The ZSC31014 has an internal 4MHz temperature-compensated oscillator that provides the time base for all operations. This oscillator feeds into a 4:1 post scalar that can optionally form the clock source for the device. Using ClkSpeed (bit 3 of EEPROM word 01_{HEX}; see section 3.6) the user can select a 4MHz clock or a 1MHz digital core clock for the ZSC31014. If the fast response times and sampling periods provided by the 4MHz clock are not needed, then choosing the 1MHz clock will result in better noise performance.

If the power supply exceeds the power-on reset level (see Table 1.3), the reset signal de-asserts and the clock generator starts working at the selected frequency (approximately 1MHz or 4MHz). The exact value only influences the conversion cycle time. To minimize the oscillator error as the V_{DD} voltage changes, an on-chip regulator supplies the oscillator block.

2.4. Diagnostic Features

The ZSC31014 offers a full suite of diagnostic features to ensure robust system operation in the most “mission-critical” applications. The diagnostic states are indicated by a transmission of the status of the 2 MSBs of the bridge high byte data.

Table 2.9 2 MSB of Data Packet Encoding

Status Bits (2 MSBs of Output Packet)	**Definition**
00	Normal operation, good data packet
01	Device in Command Mode
10	Stale data: Data that has already been fetched since the last measurement cycle. **Note**: If a data fetch is performed before or during the first measurement after power-on reset, then “stale” will be returned, but this data is actually invalid because the first measurement has not been completed.
11	Diagnostic condition exists

When the two MSBs are 11, one of the following faults listed below is indicated.

- Invalid EEPROM signature
- Loss of bridge positive or negative
- Bridge input short
- Loss of bridge source
- Loss of bridge sink

All diagnostics are detected in the next measurement cycle and reported in the subsequent data fetch. Once a diagnostic is reported, the diagnostic status bits will not change unless both the cause of the diagnostic is fixed and a power-on-reset is performed.

2.4.1. EEPROM Integrity

The contents of the EEPROM are protected by a 16-bit signature generated by a multiple input shift register (MISR). This signature is generated and stored in EEPROM (word 12_{HEX}) upon leaving Command Mode if an EEPROM write has occurred. This signature is re-generated and checked for a match after Power-On-Reset prior to entering Normal Operation Mode. If the generated signature fails to match, the part will output a diagnostic state on the output. The customer ID fields (words 00_{HEX}, $0E_{HEX}$, and 13_{HEX}) are not included in the signature.

2.4.2. Sensor Connection Check

Four dedicated comparators constantly check the range of the bridge inputs (BP/BN) to ensure they are within the envelope of 0.15∗VDD to 0.85∗VDD during all conversions. The two sensor inputs have switched ohmic paths to ground and if not driven, would discharge during the fine conversion phase. If any of the connections to the bridge break, this mechanism will detect it and put the ASIC in a diagnostic state. This diagnostic feature can be enabled/disabled with bit 0 of Diag_cfg (bits [2:1] of EEPROM word 02_{HEX}).

2.4.3. Sensor Short Check

If a short occurs between BP/BN (bridge inputs), it would normally produce a mid-range output signal and therefore would not be detected as a fault. If enabled via bit 1 of Diag_cfg (bits [2:1] of EEPROM word 02_{HEX}), the sensor short diagnostic detects BP/BN shorts. After the measurement cycle of the bridge, it will deliberately pull the BP bridge input to ground for 8µsec with a 1MHz clock or 2µsec with a 4MHz clock. At the end of this 8µsec/2µsec window, it will check to see if the BN input “followed” it down below the 15%VDD comparator check point. If so, a short must exist between BP/BN, and the part will output a diagnostic state. The bridge will have a minimum recovery time of 100 µsec for a 1MHz clock or 25 µsec for a 4MHz clock prior to the next measurement.