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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Brief Description

The ZSC31015 is adjustable to nearly all piezo-resistive bridge sensors. Measured and corrected bridge values are provided at the SIG™ pin, which can be configured as an analog voltage output or as a one-wire serial digital output.

The digital one-wire interface (OWI) can be used for a simple PC-controlled calibration procedure to program a set of calibration coefficients into an on-chip EEPROM. The calibrated ZSC31015 and a specific sensor are mated digitally: fast, precise, and without the cost overhead associated with trimming by external devices or laser. Integrated diagnostics functions make the ZSC31015 particularly well suited for automotive applications.*

Features

- Digital compensation of sensor offset, sensitivity, temperature drift, and non-linearity
- Programmable analog gain and digital gain; accommodates bridges with spans < 1mV/V and high offset
- Many diagnostic features on chip (e.g., EEPROM signature, bridge connection checks, bridge short detection, power loss detection)
- Independently programmable high and low clipping levels
- 24-bit customer ID field for module traceability
- Internal temperature compensation reference (no external components)
- Option for external temperature compensation with addition of single diode
- Output options: rail-to-rail ratiometric analog voltage (12-bit resolution), absolute analog voltage, digital one-wire interface
- Fast power-up to data out response; output available 5ms after power-up
- Current consumption depends on programmed sample rate: 1mA down to 250µA (typical)
- Fast response time: 1ms (typical)
- High voltage protection up to 30V with external JFET

Benefits

- No external trimming components required
- Simple PC-controlled configuration and calibration via one-wire interface
- High accuracy: ±0.1% FSO @ -25 to 85°C; ±0.25% FSO @ -50 to 150°C
- Single-pass calibration – quick and precise

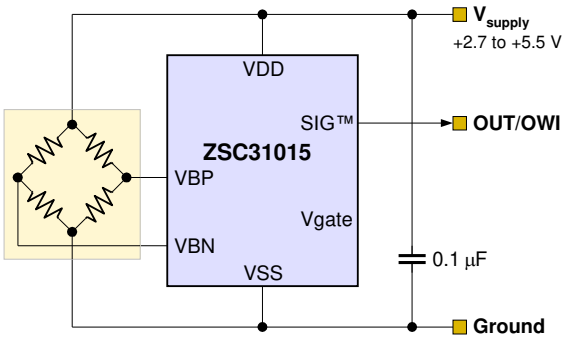
Available Support

- Evaluation Kit available
- Mass Calibration System available
- Support for industrial mass calibration available
- Quick circuit customization possible for large production volumes

Physical Characteristics

- Wide operation temperature: –50°C to +150°C
- Supply voltage 2.7 to 5.5V; with external JFET, 5.5 to 30V
- Small SOP8 package

ZSC31015 Application Circuit



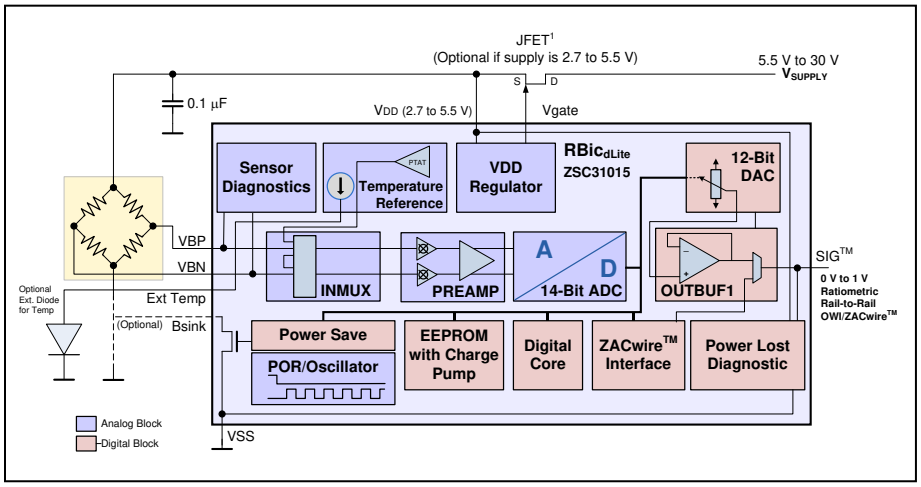
* Not AEC-Q100-qualified.

ZSC31015 Block Diagram

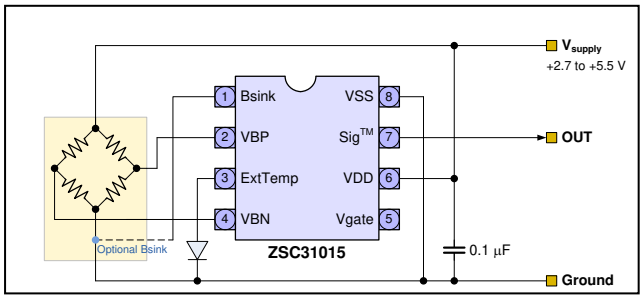
Highly Versatile Applications in Many Markets Including

- *Industrial*
- *Building Automation*
- *Office Automation*
- *White Goods*
- *Automotive **
- *Portable Devices*
- *Your Innovative Designs*

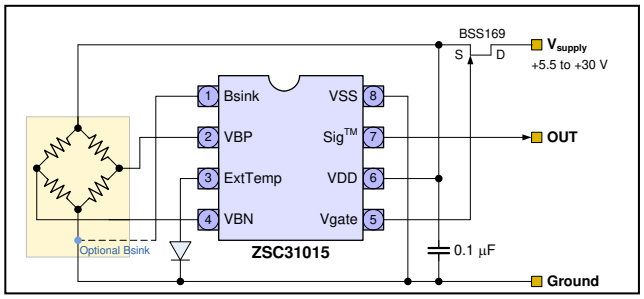
* Not AEC-Q100-qualified.



Rail-to-Rail Ratiometric Voltage Output Applications



Absolute Analog Voltage Output Applications



Ordering Examples *(See section 11 of the data sheet for additional temperature range options.)*

Sales Code	Description	Package
ZSC31015EEB	ZSC31015 Die — Temperature range: -50°C to +150°C	Unsawn on Wafer
ZSC31015EEC	ZSC31015 Die — Temperature range: -50°C to +150°C	Sawn on Wafer Frame
ZSC31015EEG1	ZSC31015 SOP8 (150 mil) — Temperature range: -50°C to +150°C	Tube: add "-T" to sales code. Reel: add "-R"
ZSC31015KIT	ZSC31015 ZACwire™ SSC Evaluation Kit: Communication Board, SSC Board, Sensor Replacement Board, USB Cable, 5 IC Samples (SOP8 150mil) (ZACwire™ SSC Evaluation Software can be downloaded from www.IDT.com/ZSC31015)	Kit

Corporate Headquarters

6024 Silver Creek Valley Road
San Jose, CA 95138
www.IDT.com

Sales

1-800-345-7015 or 408-284-8200
Fax: 408-284-2775
www.IDT.com/go/sales

Tech Support

www.IDT.com/go/support

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1 Electrical Characteristics

1.1. Absolute Maximum Ratings

Note: The absolute maximum ratings are stress ratings only. The device might not function or be operable above the operating conditions given in section 1.2. Stresses exceeding the absolute maximum ratings might also damage the device. In addition, extended exposure to stresses above the recommended operating conditions might affect device reliability. IDT does not recommend designing to the "Absolute Maximum Ratings."

Parameter	Symbol	Min	Max	Unit
Analog Supply Voltage	V_{DD}	-0.3	6.0	V
Voltages at Analog I/O – In Pin	V_{INA}	-0.3	VDD+0.3	V
Voltages at Analog I/O – Out Pin	V_{OUTA}	-0.3	VDD+0.3	V
Storage Temperature Range (≥10 hours)	T_{STOR}	-50	150	°C
Storage Temperature Range (<10 hours)	$T_{STOR<10h}$	-50	170	°C

Note: Also see Table 6.1 regarding soldering temperature and storage conditions.

1.2. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Analog Supply Voltage to Ground	V_{DD}	2.7	5.0	5.5	V
Analog Supply Voltage (with external JFET Regulator)	V_{SUPP}	5.5	7	30	V
Common Mode Voltage	V_{CM}	1		V_{DD} – 1.3	V
Ambient Temperature Range [1), 2)]	T_{AMB}	-50		150	°C
External Capacitance between V_{DD} and Ground	C_{VDD}	100	220	470	nF
Output Load Resistance to V_{DD} [3)]	$R_{L,OUT}$	5			kΩ
Output Load Resistance to VSS [3),4)]	$R_{L,OUT}$	5			kΩ
Output Load Capacitance [5)]	$C_{L,OUT}$	1	10	15	nF
Bridge Resistance [6),7)]	R_{BR}	0.3		100	kΩ
Power-On Rise Time	t_{PON}			100	ms

1) Note that the maximum EEPROM programming temperature is 85°C.
2) If buying die, designers should use caution not to exceed maximum junction temperature by proper package selection.
3) Only needed for Analog Output Mode; not needed for Digital Output Mode. When a pull-down resistor is used as the load resistor, the power loss detection diagnostic for loss of VSS cannot be assured at R_L=5k; R_L=10k is recommended for this configuration.
4) Note: for unlocked devices or during calibration, the minimum value of output load resistance to VSS is 20kΩ.
5) Using the output for digital calibration, $C_{L,OUT}$ is limited by the maximum rise time $t_{ZAC,rise}$. See section 1.3.8.
6) Note: Minimum bridge resistance is a factor if using the Bsink feature. The rds(on) of the Bsink transistor is 8 to 10Ω when operating at V_{DD}=5V. This does give rise to a ratiometricity inaccuracy that becomes greater with low bridge resistances.
7) Note: Minimum bridge resistance is important if using certain diagnostic features. It must be at least 0.3kΩ at V_{DD}=2.7V and at least 0.6kΩ at V_{DD}=5V for the Sensor Short Check to function properly. For details, see section 2.6.3.

1.3. Electrical Parameters

See important table notes at the end of the table. Note: For parameters marked with an asterisk, there is no verification in mass production; the parameter is guaranteed by design and/or quality observation.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
1.3.1. Supply/Regulation Characteristics						
Supply Voltage	V_{DD}		2.7	5.0	5.5	V
Supply Current (varies with update rate and output mode)	I_{DD}	At minimum update rate		0.25		mA
		At maximum update rate		1.0	1.4	
Temperature Coefficient – PTAT Source *	T_{CPTAT}			20	100	ppm/K
Power Supply Rejection Ratio *	PSRR		60			dB
Power-On Reset Level	POR		1.4		2.6	V
1.3.2. Parameters for Analog Front-End (AFE)						
Leakage Current Pin VBP,VBN	I_{IN_LEAK}	Sensor connection and short check must be disabled.			±10	nA
1.3.3. Parameters for EEPROM						
Number Write Cycles	n_{WRI_EEP}	At 150°C			100	Cycles
		At 85°C			100k	Cycles
Data Retention	t_{WRI_EEP}	At 100°C			10	Years
1.3.4. Parameters for A/D Converter						
ADC Resolution	r_{ADC}				14	Bit
Integral Nonlinearity (INL) [1)]	INL_{ADC}	Based on ideal slope	-4		+4	LSB
Differential Nonlinearity (DNL) *	DNL_{ADC}		-1		+1	LSB
1.3.5. Parameters for Analog Output (DAC and Buffer)						
Max. Output Current	I_{OUT}	Max. current maintaining accuracy	2.2			mA
Resolution	Res	Referenced to V_{DD}			12	Bit
Absolute Error	E_{ABS}	DAC input to output			±0.2%	V_{DD}
Differential Nonlinearity *	DNL	No missing codes	-0.9		+3.0	LSB_{12Bit}
Upper Output Voltage Limit	V_{OUT}	R_L = 5 kΩ	95%			V_{DD}
Lower Output Voltage Limit	V_{OUT}	With 5kΩ pull down, 0 to1V output			16.5mV	mV
Output Short Circuit Protection Limit	I_{SC}	Depends on operating conditions. Short circuit protection must be enabled via Diag_cfg (EEPROM word [102:100]). See section 2.4.2.	3		40	mA
Analog Output Noise Peak-to-Peak	$V_{NOISE,PP}$	Shorted input			5 ±1LSB	mV

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
1.3.6. Diagnostics						
Upper diagnostic output level	$V_{DIA,H}$		97.5%			V_{DD}
Lower diagnostic output level	$V_{DIA,L}$				2.5%	V_{DD}
Minimum load resistor for power loss [2)]	R_{L,OUT_PS}	Pull-up or pull-down in Analog Output Mode	5			kΩ
1.3.7. External Temperature Measurement						
External Temperature (ExtTemp) Signal Input Range	V_{TSE}		150		800	mV
Required External Temperature Diode Sensitivity	ST_{TSE}		1.9		3.25	mV/K
Temperature Span with External Temperature Diode	T_{TSE_SP}		-50		150	°C
1.3.8. Parameters for ZACwire™ Serial Interface						
ZACwire™ Line Resistance *	$R_{ZAC,load}$	The rise time must be $t_{ZAC,rise} = 2 * R_{ZAC,load} * C_{ZACload} \leq 5\mu s$. If using a pull-up resistor instead of a line resistor, it must meet this specification. The absolute maximum for $C_{ZACload}$ is 15nF.			3.9	kΩ
ZACwire™ Load Capacitance *	$C_{ZAC,load}$		0	1	15	nF
Voltage Level Low *	$V_{ZAC,low}$			0	0.2	V_{DD}
Voltage Level High *	$V_{ZAC,low}$		0.8	1		V_{DD}
1.3.9. Parameters for System Response						
Start-Up-Time	t_{STA}	Power-up to output Update_rate = 1 kHz (1 ms)			8	ms
Response Time – Analog Output	t_{RESP-A}	Update_rate = 1 kHz (1 ms)		1	2	ms
Response and Transmission Time for Digital Output	$t_{RES, DIG}$	Varies with update rate. Value given at fastest rate.		1.6		ms
Sampling Rate	f_S	Update_rate = 1 kHz (1 ms)		1000		Hz
Overall Linearity Error– Digital	E_{LIND}	Bridge input to output		0.025	0.04	%
Overall Linearity Error – Analog	E_{LINA}	Bridge input to output		0.1	0.2	%
Overall Ratiometricity Error	RE_{out}	±10%VDD, Not using Bsink feature			0.035	%

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Overall Accuracy – Digital (only IC, without sensor bridge)	AC_{outD}	-25°C to 85°C			±0.1%	%FSO
		-50°C to 150°C			±0.25%	
Overall Accuracy – Analog [3), 4)] (only IC, without sensor bridge)	AC_{outA}	-25°C to 85°C			±0.25%	%FSO
		-40°C to 125°C			±0.35%	
		-50°C to 150°C			±0.5%	

1) Note: This is ± 4 LSBs for the 14-bit A-to-D conversion. This results in absolute accuracy to 12-bits on the A-to-D result. Non-linearity is typically better at temperatures less than 125°C.
2) When using a pull-down resistor as the load resistor, the power loss detection diagnostic for loss of VSS cannot be assured at R_L=5kΩ; R_L=10kΩ is recommended for this configuration.
3) Not included is the quantization noise of the DAC. The 12-bit DAC has a quantization noise of ± ½ LSB = 0.61mV (@ 5V VDD) = 0.0125%.
4) Analog output range 2.5% to 95%

1.4. Analog Inputs versus Output Resolution

The ZSC31015 has a fully differential chopper-stabilized pre-amplifier with four programmable gain settings. The output of the pre-amplifier feeds into a 14-bit charge-balanced ADC. Span, offset, temperature, and non-linearity correction are performed in the digital domain. Then the resulting corrected bridge value can be output in analog form through a 12-bit DAC or as a 16-bit serial digital packet. The resolution of the output depends on the input span (bridge sensitivity) and the analog gain setting programmed. Digital gains can vary from [0,32). Analog gains available are 6, 24, 48, and 96.

Note: At higher analog gain settings, there will be higher output resolution, but the ability of the ZSC31015 to handle large offsets decreases. This is expected because the offset is also amplified by the analog gain and can therefore saturate the ADC input.

The following tables outline the guaranteed minimum resolution for a given bridge sensitivity range.

Table 1.1 ADC Resolution Characteristics for an Analog Gain of 6

Analog Gain 6				
Input Span [mV/V]			Allowed Offset (+/- % of Span) [1]	Minimum Guaranteed Resolution [Bits]
Min	Typ	Max		
57.8	80.0	105.8	38%	12.4
50.6	70.0	92.6	53%	12.2
43.4	60.0	79.4	73%	12.0
36.1	50.0	66.1	101%	11.7
28.9	40.0	52.9	142%	11.4
21.7	30.0	39.7	212%	11.4

1) In addition to Tco, Tcg.

Table 1.2 ADC Resolution Characteristics for an Analog Gain of 24

Analog Gain 24				
Input Span [mV/V]			Allowed Offset (+/- % of Span) [1]	Minimum Guaranteed Resolution [Bits]
Min	Typ	Max		
18.1	25.0	33.1	17%	12.7
14.5	20.0	26.5	38%	12.4
7.2	10.0	13.2	142%	11.4
3.6	5.0	6.6	351%	10.4
1.8	2.5	3.3	767%	9.4
0.9	1.2	1.6	1670%	8.4

1) In addition to Tco, Tcg.

Important Note: The yellow shadowed fields indicate that for these input spans with the selected analog gain setting, the quantization noise is higher than 0.1% FSO.

Table 1.3 ADC Resolution Characteristics for an Analog Gain of 48

Analog Gain 48				
Input Span [mV/V]			Allowed Offset (+/- % of Span) [1]	Minimum Guaranteed Resolution [Bits]
Min	Typ	Max		
10.8	15.0	19.8	3%	13.0
7.2	10.0	13.2	38%	12.4
4.3	6.0	7.9	107%	11.7
2.9	4.0	5.3	194%	11.1
1.8	2.5	3.3	351%	10.4
1.0	1.4	1.85	678%	9.6
0.72	1.0	1.32	976%	9.1

1) In addition to Tco, Tcg.

Important Note: The yellow shadowed fields indicate that for these input spans with the selected analog gain setting, the quantization noise is higher than 0.1% FSO.

Table 1.4 ADC Resolution Characteristics for an Analog Gain of 96

Analog Gain 96				
Input Span [mV/V]			Allowed Offset (+/- % of Span) [1]	Minimum Guaranteed Resolution [Bits]
Min	Typ	Max		
4.3	6.0	7.9	21%	12.7
2.9	4.0	5.3	64%	12.1
1.8	2.5	3.3	142%	11.4
1.0	1.4	1.85	306%	10.6
0.72	1.0	1.32	455%	10.1

1) In addition to Tco, Tcg.

2 Circuit Description

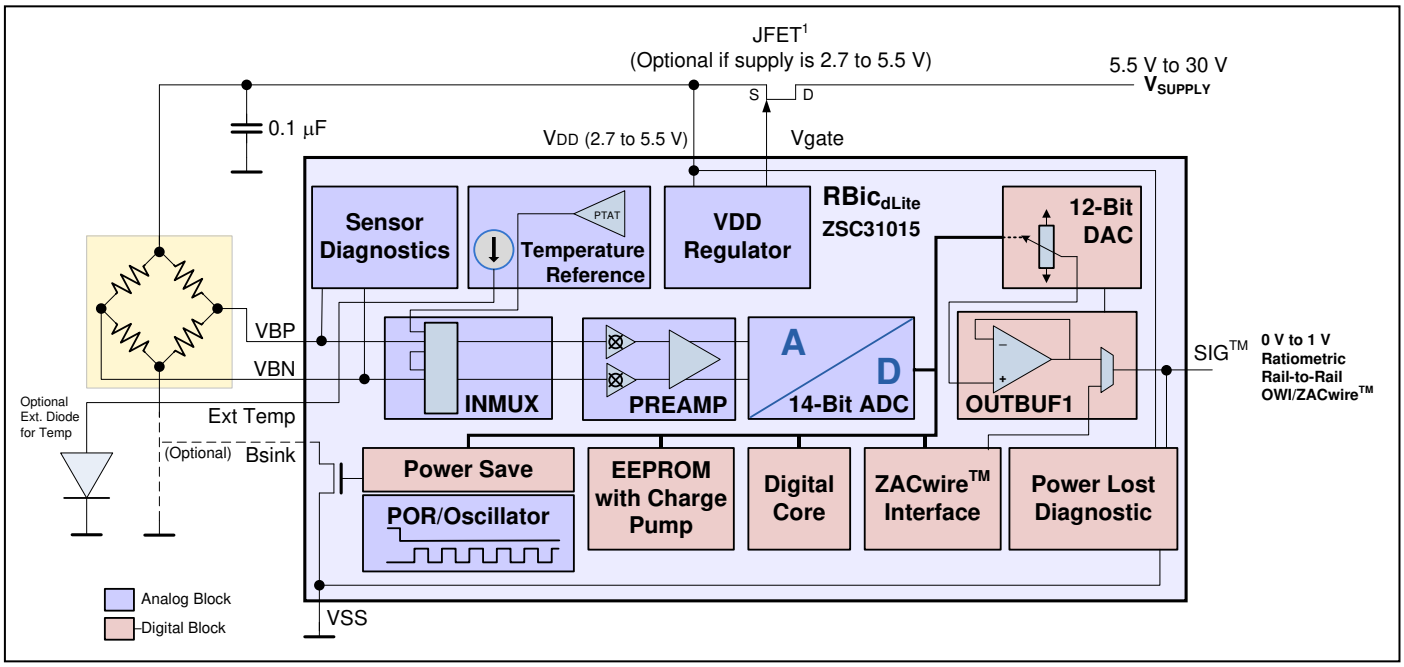
2.1. Signal Flow and Block Diagram

The ZSC31015 resistive bridge sensor interface ICs were specifically designed as cost-effective solutions for sensing in building automation, automotive *, industrial, office automation and white goods applications. The ZSC31015 employs IDT's high precision bandgap with proportional-to-absolute-temperature (PTAT) output; low-power 14-bit analog-to-digital converter (ADC, A2D, A-to-D); and an on-chip DSP core with EEPROM to precisely calibrate the bridge output signal.

Three selectable outputs, two analog and one digital, offer the ultimate in versatility across many applications. The ZSC31015 rail-to-rail ratiometric analog V_{out} signal (0V to ~5 V V_{out} @ V_{DD}=5V) suits most building automation and automotive requirements (12-bit resolution). Typical office automation and white goods applications require the 0 to ~1V V_{out} signal, which in the ZSC31015 is referenced to the internal bandgap. The ZSC31015 is capable of running in high-voltage (5.5 to 30V) systems when combined with an external JFET.

Direct interfacing to µP controllers is facilitated via IDT's single-wire serial ZACwire™ digital interface.

Figure 2.1 ZSC31015 Block Diagram



* Not AEC-Q100-qualified.

2.2. Analog Front End

2.2.1. Bandgap/PTAT and PTAT Amplifier

The highly linear Bandgap/PTAT section provides the PTAT signal to the ADC, which allows accurate temperature conversion. In addition, the ultra-low ppm Bandgap provides a stable voltage reference over temperature for the operation of the rest of the IC. If the bridge is not near the ZSC31015, an external diode can be used for temperature measurement/compensation.

The temperature signal (internal PTAT or external diode) is amplified through a path in the Pre-Amp and fed to the ADC for conversion. The most significant 12-bits of this converted result are used for temperature measurement and temperature correction of bridge readings. When temperature is output in Digital Mode, only the most significant 8 bits are given.

When external temperature is selected, add a diode from the ExtTemp pin to ground. The diode is biased with approximately 50µA during temperature measurement cycles. The voltage level on ExtTemp is amplified through the Pre-Amp and converted by the ADC. Ensure that the ExtTemp signal is in the range of 150mV to 800mV to prevent saturation of the ADC. If the selected diode has a sensitivity in the range of 1.9mV/°C to 3.25mV/°C, a corrected temperature output (in Digital Mode) can be achieved for a 200°C temperature span (-50°C to 150°C).

2.2.2. Bridge Supply

The voltage-driven bridge is usually connected to V_{DD} and ground. As a power savings feature, the ZSC31015 also includes a switched transistor to interrupt the bridge current via pin 1 (Bsink). The transistor switching is synchronized to the analog-to-digital conversion and released after finishing the conversion. To utilize this feature, the low supply of the bridge should be connected to Bsink instead of ground.

Depending on the programmable update rate, the average current consumption (including bridge current) can be reduced to approximately 20%, 5%, or 1%. Note: this feature has no power savings benefit if using the fastest update rate mode.

2.2.3. PREAMP Block

The differential signal from the bridge is amplified through a chopper-stabilized instrumentation amplifier with very high input impedance designed for low noise and low drift. This pre-amp provides gain for the differential signal and re-centers its DC to $V_{DD}/2$. The output of the Pre-Amp block is fed into the ADC. The calibration sequence performed by the digital core includes an auto-zero sequence to null any drift in the Pre-Amp state over temperature.

The Pre-Amp can be set to a gain of 6, 24, 48, or 96 through an EEPROM setting.

The inputs to the Pre-Amp from (VBN/VBP pins) can be reversed via an EEPROM configuration bit.

2.2.4. Analog-to-Digital Converter (ADC)

A 14-bit/1ms 2nd order charge-balancing ADC is used to convert signals coming from the pre-amplifier. The converter, designed in full differential switched capacitor technique, is used for converting the various signals in the digital domain.

This principle offers the following advantages:

- High noise immunity because of the differential signal path and integrating behavior
- Independence from clock frequency drift and clock jitter
- Fast conversion time due to second-order mode

Four selectable values for the zero point of the input voltage allow conversion to adapt to the sensor's offset parameter. With the Reverse Input Polarity Mode and the negative digital gain options, this results in seven possible zero point adjustments (not eight because the -1/2,1/2 offset setting is the same regardless of gain polarity).

The conversion rate varies with the programmed update rate. The fastest conversation rate is 1k samples/s and the response time is then 1ms. Based on a best fit, the Integral Nonlinearity (INL) is less than 4 LSB_{14Bit}.

2.3. Digital Signal Processor

A digital signal processor (DSP) is used for processing the converted bridge data as well as performing temperature correction and computing the temperature value for output on the digital channel.

The digital core reads correction coefficients from EEPROM and can correct for the following:

- Bridge Offset
- Bridge Gain
- Variation of Bridge Offset over Temperature (Tco)
- Variation of Bridge Gain over Temperature (Tcg)
- A single second order effect (SOT) (Second Order Term)

The EEPROM contains a single SOT that can be applied to correct one and only one of the following:

- 2nd order behavior of bridge measurement
- 2nd order behavior of Tco
- 2nd order behavior of Tcg

If the SOT applies to correcting the bridge reading, then the correction formula for the bridge reading is represented as a two-step process as follows:

$$ZB = Gain\_B(1 + \Delta T * Tcg) * (BR\_Raw - Offset\_B + \Delta T * Tco) \quad (1)$$

$$BR = ZB(1.25 + SOT * ZB) \quad (2)$$

Where:

BR	=	Corrected Bridge reading that is output as digital or analog on the SIG™ pin
ZB	=	Intermediate result in the calculations
BR_Raw	=	Raw Bridge reading from ADC
T_Raw	=	Raw Temp reading converted from PTAT signal or external diode
Gain_B	=	Bridge Gain term
Offset_B	=	Bridge Offset term
Tcg	=	Temperature Coefficient Gain
Tco	=	Temperature Coefficient Offset
ΔT	=	(**T_Raw – T_{SETL}**)
T_{SETL}	=	T_Raw reading at which low calibration was performed (typically 25°C)
SOT	=	Second-Order Term

Note For solving equation (1) the following condition must be met:

$$BR\_Raw \geq BR / Gain\_B$$

If this condition is not met, the analog Pre-Amp Gain must be set to a smaller value because a negative Offset_B is not supported.

If the **SOT** applies to correcting the 2nd order behavior of **Tco**, then the formula for bridge correction is as follows:

$$BR = Gain\_B(1 + \Delta T * Tcg) * [BR\_Raw - Offset\_B + \Delta T(SOT * \Delta T + Tco)] \quad (3)$$

If the SOT applies to correcting the 2nd order behavior of Tcg, then the formula for bridge correction is as follows:

$$BR = Gain\_B[1 + \Delta T(SOT * \Delta T + Tcg)] * [BR\_Raw - Offset\_B + \Delta T * Tco] \quad (4)$$

The bandgap reference gives a very linear PTAT signal, so temperature correction can always simply be accomplished with a linear gain and offset term.

Corrected Temperature Reading:

$$T = Gain\_T(T\_Raw + Offset\_T) \quad (5)$$

Where:

T_Raw = Raw Temperature reading converted from PTAT signal or external diode

Offset_T = Offset Coefficient for Temperature

Gain_T = Gain Coefficient for Temperature

2.3.1. EEPROM

The EEPROM contains the calibration coefficients for gain and offset, etc., and the configuration bits, such as output mode, update rate, etc. The ZSC31015 also offers three user-programmable storage bytes for module traceability. When programming the EEPROM, an internal charge pump voltage is used; therefore a high voltage supply is not needed. The EEPROM is implemented as a shift register. During an EEPROM read, the contents are shifted 8 bits before each transmission of one byte occurs. The charge pump is internally regulated to 12.5 V, and the programming time is 6ms.

See section 2.6.1 regarding EEPROM signatures for verifying EEPROM integrity.

Note: EEPROM writing can only be performed at temperatures lower than 85ºC.

2.3.2. One-Wire Interface – ZACwire™

The IC communicates via a one-wire serial interface. There are different commands available for the following:

- Reading the conversion result of the ADC (Get_BR_Raw, Get_T_Raw)
- Calibration commands
- Reading from the EEPROM (“dump” of entire contents)
- Writing to the EEPROM (trim setting, configuration, and coefficients)

2.4. Output Stage

2.4.1. Digital to Analog Converter (Output DAC) with Programmable Clipping Limits

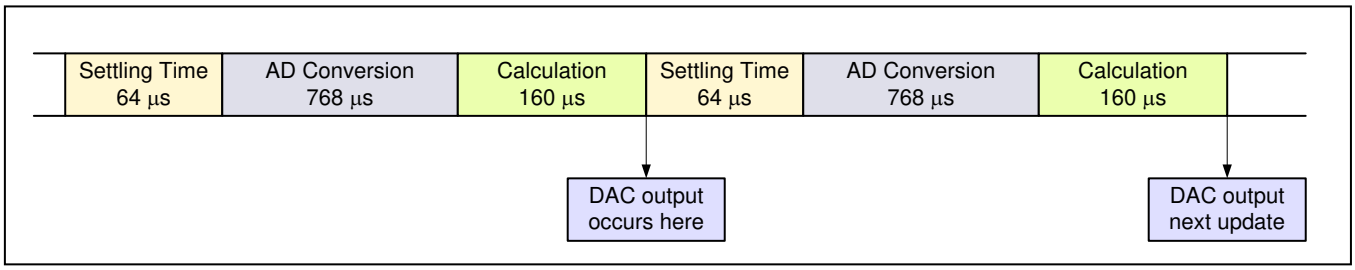
A 12-bit DAC based on sub-ranging resistor strings is used for the digital-to-analog output conversion in the analog ratiometric and absolute analog voltage modes. Options during calibration configure the system to operate in either of these modes. The design allows for excellent testability as well as low power consumption. The DAC allows programming a lower and upper clipping limit (Low_Clip_Lim and Up_Clip_Lim bit fields respectively; see section 3.5) for the output signal (analog and digital). The internal 14-bit calculated bridge value is compared against the 14-bit value formed by {11,Up_Clip_Lim[6:0],11111} for the upper limit and against {00,Low_Clip_Lim[6:0],00000} for the lower limit. If the calculated bridge value is higher than the upper limit or less than the lower limit, the analog output value is clipped to this value; otherwise it is output as is.

Example for the upper clipping level: If the Up_Clip_Lim[6:0] = 0000000, then the 14-bit value used for the clipping threshold is 11000000011111. This is 75.19% of full scale. Since there are 7 bits of upper clipping limit, there are 127 possible values between 75.19% and 100%. Therefore the resolution of the clipping limits 0.195%.

Example for the lower clipping level: If the Low_Clip_Lim[6:0] = 1111111, then the 14-bit value used for the clipping threshold is 00111111100000. This is 24.8% of full scale. Since there are 7 bits of lower clipping limit, there are 127 possible values between 0 and 24.8%. Therefore the resolution of the lower clipping limit is 0.195%.

Figure 2.2 shows the data timing of the DAC output for the update rate setting 00.

Figure 2.2 DAC Output Timing for Highest Update Rate



2.4.2. Output Buffer

A rail-to-rail op amp configured as a unity gain buffer can drive resistive loads (whether pull-up or pull-down) as low as 5kΩ and capacitances up to 15nF (for pure analog output). In addition, to limit the error due to amplifier offset voltage, an error compensation circuit is included which tracks and reduces offset voltage to < 1mV. The output of the ZSC31015 output can be permanently shorted to VDD or VSS without damaging the device. The output driver contains a current-limiting block that detects a hard short and limits the current to a safe level. The short circuit protection current can vary from a minimum of 3mA to a maximum of 40mA depending on operating conditions. Output short circuit protection can be enabled via Diag_cfg (EEPROM [102:100]). Enabling this protection is recommended when using the analog output.

2.4.3. Voltage Reference Block

A linear regulator control circuit is included in the Voltage Reference Block to interface with an external JFET to allow operation in systems where the supply voltage exceeds 5.5V. This circuit can also be used for over-voltage protection. The regulator set point has a coarse adjustment controlled by the JFET_cfg EEPROM bits that can adjust the set point around 5.0 or 5.5V. (See Table 3.5 for bit locations and section 2.3.1 regarding writing to the EEPROM.). The 1V trim setting (see below) can also act as a fine adjust for the regulation set point. The 5V reference can be trimmed within +/-15mV.

Note: If using the external JFET for over-voltage protection purposes (i.e., 5V at JFET drain and expecting 5V at JFET source), there will be a voltage drop across the JFET; therefore ratiometricity will be slightly compromised depending on the rds(on) of the chosen JFET. A Vishay J107 is the best choice because it has only an 8mV drop worst case. If using as regulation instead of over-voltage protection, a MMBF4392 or BSS169 also works well.

The Voltage Reference Block uses the absolute reference voltage provided by the bandgap to produce two regulated on-chip voltage references. A 1V reference is used for the output DAC high reference when the part is configured in 0-1V Analog Output Mode. For this reason, the 1V reference must be very accurate and includes trim so that its value can be trimmed within +/- 3mV of 1.00V. The 1V reference is also used as the on-chip reference for the JFET regulator block. The regulation set point of the JFET regulator can be fine-tuned using the 1V trim.

The reference trim setting is selected with the 1V_Trim/JFET_Trim bits in EEPROM. See Table 3.5 for bit locations. Table 2.1 shows the order of trim codes with 0111 for the lowest reference voltage and 1000 for the highest reference voltage.

Important: Optimal reference trim is determined during wafer-level testing and final package testing. Back-up copies of these bits are stored in bits in the CUST_ID0 bits for applications requiring accurate references. In this case, see section 5 for important notes and instructions for verifying the integrity of the 1V_Trim/JFET_Trim bits and if necessary, restoring the value from the CUST_ID0 bits before calibration.

Table 2.1 1V Reference Trim (1V vs. Trim for Nominal Process Run)

Order	1Vref/ 5Vref_trim3	1Vref/ 5Vref_trim2	1Vref/ 5Vref_trim1	1Vref/ 5Vref_trim0
Highest Reference Voltage	1	0	0	0
…	1	0	0	1
…	1	0	1	0
…	1	0	1	1
…	1	1	0	0
…	1	1	0	1
…	1	1	1	0
…	1	1	1	1
…	0	0	0	0
…	0	0	0	1
…	0	0	1	0
…	0	0	1	1
…	0	1	0	0
…	0	1	0	1
…	0	1	1	0
Lowest Reference Voltage	0	1	1	1

2.5. Clock Generator / Power-On Reset (CLKPOR)

If the power supply exceeds 2.5V (maximum), the reset signal de-asserts and the clock generator starts working at a frequency of approximately 512kHz (±20%). The exact value only influences the conversion cycle time and communication to the outside world but not the accuracy of signal processing. In addition, to minimize the oscillator error as the V_{DD} voltage changes, an on-chip regulator is used to supply the oscillator block.

2.5.1. Trimming the Oscillator

Settings for the Osc_Trim bits in EEPROM fine-tune the oscillator frequency. See Table 3.5 for bit locations and Table 2.2 for possible settings. The default value is 0_{HEX} to ensure communication on start-up.

Important: Optimal oscillator trimming is determined during wafer-level testing and final package testing, and this part-specific factory value, which can be copied to Osc_Trim, is stored in bits in the CUST_ID1 and CUST_ID2 EEPROM bits for applications requiring optimal response time. In this case, see section 5 for important notes and instructions for copying these optimal values to the Osc_Trim bits before calibration. It is strongly recommended that only the default value or the factory trim value be used because ZACwire™ communication is not guaranteed at different oscillator frequencies.

Table 2.2 Oscillator Trimming

Osc_Trim Bits	Delta Frequency (kHz)
100	+385
101	+235
110	+140
111	+65
000	Nominal
001	-40
010	-76
011	-110

Example: Programming $011_B \rightarrow$ the trimmed frequency = nominal value – 110 kHz.

2.6. Diagnostic Features

The ZSC31015 offers a full suite of diagnostic features to ensure robust system operation in the most “mission-critical” applications. If the part is programmed in Analog Output Mode, then diagnostic states are indicated by an output below 2.5% of VDD or above 97.5% of VDD. If the part is programmed in Digital Output Mode, then diagnostic states will be indicated by a transmission with a generated parity error.

Table 2.3 gives a summary of the diagnostic features, which are explained in detail in the following sections. EEPROM settings that control diagnostic functions are given in section 3.5.

Table 2.3 Summary of Diagnostic Features

Detected Fault	Analog Diagnostic Level	ZACwire™ Diagnostic	Delay in Detection
EEPROM signature	Lower	Generates parity error	10ms after power-on
Loss of bridge positive	Upper	Generates parity error	2ms
Loss of bridge negative	Upper	Generates parity error	2ms
Open bridge connection	Upper	Generates parity error	2ms
Bridge input short	Upper	Generates parity error	2ms
ExtTemp pin open	Lower	Generates parity error	300ms
ExtTemp pin shorted to PWR/GND	Lower	Generates parity error	300ms
ExtTemp pin shorted to BP/BN[†]	Upper	Generates parity error	3ms
Loss of VDD	Lower	Transmissions stop	Dependent on R_L and C_L
Loss of VSS	Upper	Transmissions stop	Dependent on R_L and C_L

2.6.1. EEPROM Integrity

The contents of the EEPROM are protected by an 8-bit LFSR signature (linear feedback shift register). This signature is regenerated and stored in EEPROM every time EEPROM contents are changed. This signature is generated and checked for a match after Power-On-Reset prior to entering Normal Operation Mode. If the generated signature fails to match, the part will output a diagnostic state on the output.

In addition to an extensive temporal and code interlock mechanism used to prevent false writes to the EEPROM, the ZSC31015 offers an EEPROM lock mechanism for high-security applications. When EEPROM bits 105:103 are programmed with “011” or “110,” this 3-bit field will permanently disable the VPP charge pump and will not allow further writes to the EEPROM. See Table 2.3 in section 2.6 for more information.

2.6.2. Sensor Connection Check

Four dedicated comparators permanently check the range of the bridge inputs (BP/BN) to ensure they are within the envelope of 0.8V to 0.85∗VDD during all conversions. The two sensor inputs have a switched ohmic path to ground and if left floating, would be discharged. If any of the wires connecting the bridge break, this mechanism will detect it and put the ZSC31015 in a diagnostic state. This same diagnostic feature can also detect a short between BP/BN and the ExtTemp signal if an external diode is being used for temperature measurement. See Table 2.3 in section 2.6 for more information.

[†] A short from ExtTemp to BP/BN might not be detected in some circuit configurations.

2.6.3. Sensor Short Check

If a short occurs between BP/BN (bridge inputs), it would normally produce an in-range output signal and therefore would not be detected as a fault. This diagnostic mode, if enabled, will deliberately look for such a short. After the measurement cycle of the bridge, it will deliberately pull the BP bridge input to ground for 4µsec. At the end of this 4µsec window, it will check to see if the BN input "followed" it down below the 0.8V comparator checkpoint. If so, a short must exist between BP/BN, and the part will output a diagnostic state. The bridge will have a minimum of 480µsec recovery time prior to the next measurement. See Table 2.3 in section 2.6 for more information.

The bridge resistance must be taken into account if the Sensor Short diagnostic feature is used. At V_{DD}= 2.7V, the minimum bridge resistance is 0.3KΩ, and at V_{DD} = 5V, the minimum bridge resistance is 0.6KΩ.

2.6.4. Power Loss Detection

If the power or GND connection to the module containing the sensor bridge and the ZSC31015 is lost, the ZSC31015 will output a diagnostic state if a pull-up or pull-down terminating resistor greater than or equal to 5kΩ is connected in the final application. This diagnostic mode only works when the part is configured in Analog Output Mode. See Table 2.3 in section 2.6 for more information.

2.6.5. ExtTemp Connection Checks

When external temperature is selected and connection checking is enabled, the part performs range checking on the converted temperature value. If the internal ADC reading of the temperature is less than 1/32 of full scale or greater than 63/64 of full scale then a diagnostic state is asserted. If the ExtTemp pin is shorted to ground, the ADC reads less than 1/32. Because 100µA is sourced onto the ExtTemp pin during conversions, it naturally pulls up during these times. If the ExtTemp pin is open, it produces an ADC reading greater than 63/64 of full scale. Both these bad connection conditions would be detected and result in a diagnostic output. If internal temperature is selected or sensor connection check is not enabled, then this diagnostic check is not enabled. See Table 2.3 in section 2.6 for more information.

3 Functional Description

3.1. General Working Mode

The command/data transfer takes place via the one-wire SIG™ pin using the ZACwire™ serial communication protocol.

After power-on, the ZSC31015 waits for 3ms (= Command window) for the Start_CM command.

Without this command, the Normal Operation Mode (NOM) starts. In this mode, raw bridge values are converted, and the corrected values are presented on the output in analog or digital format (depending on the configuration stored in EEPROM).

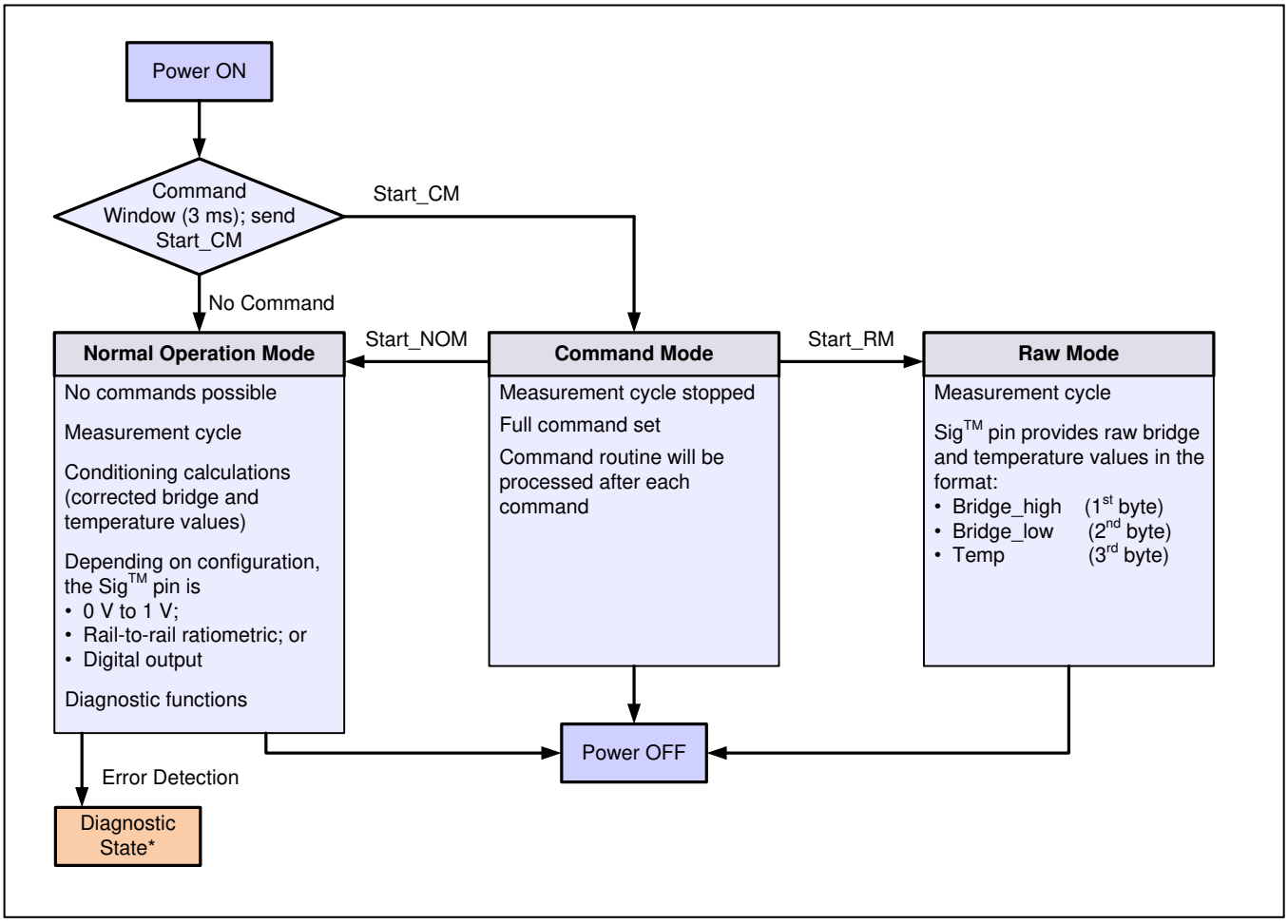
Command Mode (CM) can only be entered during the 3ms command window after power-on. If the ZSC31015 receives the Start_CM command during the command window, it remains in the Command Mode. The CM allows changing to one of the other modes via command. After the command Start_RW, the ZSC31015 is in the Raw Mode (RM). Without correction, the raw values are transmitted to the digital output in a predefined order. The RM can only be stopped by a power-off. RM is used by the calibration software for collection of raw bridge and temperature data so the correction coefficients can be calculated.

If diagnostic features are enabled and a diagnostic fault is detected, diagnostic states are indicated as follows depending on the programmed mode:

- In Analog Output Mode,
  diagnostic states are indicated by an output below 2.5% of VDD or above 97.5% of VDD.
- In Digital Output Mode,
  diagnostic states will be indicated by a transmission with a generated parity error.

For more details see section 2.6.

Figure 3.1 General Working Mode



* See section 2.6.

3.2. ZACwire™ Communication Interface

3.2.1. Properties and Parameters

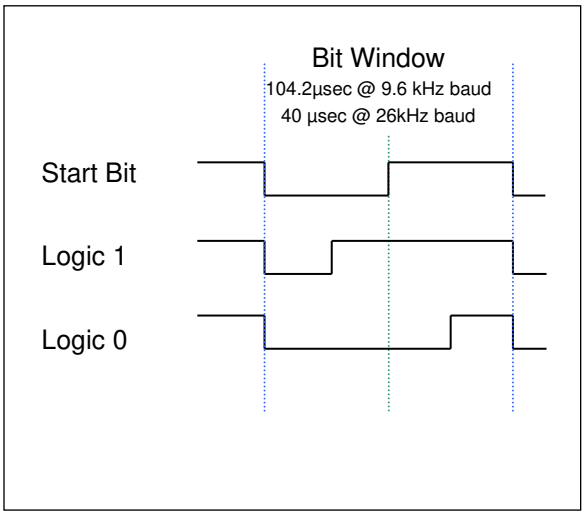
Table 3.1 Pin Configuration and Latch-Up Conditions

No.	Parameter	Symbol	Min	Typ	Max	Unit	Comments
1	Pull-up resistor (on-chip)	$R_{ZAC,pu}$		30		kΩ	On-chip pull-up resistor switched on during Digital Output Mode and during CM Mode (first 3 ms after power up).
2	Pull-up resistor (external)	R_{ZAC,pu_ext}	150			Ω	If the master communicates via a push-pull stage, no pull-up resistor is needed; otherwise, a pull-up resistor with a value of at least 150 Ω must be connected.
3	ZACwire™ rise time	$t_{ZAC,rise}$			5	µs	Any user RC network included in the Sig™ path must meet this rise time.
4	ZACwire™ line resistance [1)]	$R_{ZACload}$			3.9	kΩ	Also see section 1.3.8.
5	ZACwire™ load capacitance [1)]	$C_{ZAC,load}$	0	1	15	nF	Also see section 1.3.8.
6	Voltage low level	$V_{ZAC,low}$		0	0.2	V_{DD}	Rail-to-rail CMOS driver.
7	Voltage high level	$V_{ZAC,high}$	0.8	1		V_{DD}	Rail-to-rail CMOS driver.

1) The rise time must be $t_{ZAC,rise} = 2 * R_{ZACload} * C_{ZACload} \leq 5$ µs . If using a pull-up resistor instead of a line resistor, it must meet this specification. The absolute maximum for $C_{ZACload}$ is 15nF.

3.2.2. Bit Encoding

Figure 3.2 Manchester Duty Cycle



Start bit = 50% duty cycle used to set up strobe time

Logic 1 = 75% duty cycle

Logic 0 = 25% duty cycle

Stop Time

The ZACWire™ bus will be held high for 32µs (nominal) between consecutive data packets regardless of baud rate.