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Brief Description

ZSC31050 is a CMOS integrated circuit for highly accurate amplification and sensor-specific correction of bridge sensor and temperature sensor signals. The device provides digital compensation of sensor offset, sensitivity, temperature drift, and nonlinearity via a 16-bit RISC microcontroller running a polynomial correction algorithm.

The ZSC31050 accommodates virtually any bridge sensor type (e.g., piezo-resistive, ceramic thick-film, or steel membrane based). In addition, it can interface to a separate temperature sensor. The bi-directional digital interfaces (I²C, SPI, and ZACwire™) can be used for a simple PC-controlled one-pass calibration procedure to program a set of calibration coefficients into an on-chip EEPROM. A specific sensor and a ZSC31050 can be mated digitally: fast, precise, and without the cost overhead associated with trimming by external devices or laser. The ZACwire™ interface enables an end-of-line calibration of the sensor module.

Typical applications for the ZSC31050 include industrial, medical, and consumer products. It is specifically engineered for most resistive bridge sensors; e.g., sensors for measuring pressure, force, torque, acceleration, angle, position, and revolution.

Benefits

- No external trimming components required
- PC-controlled configuration and calibration via digital bus interface – simple, low cost
- High accuracy (±0.1% FSO @ –25 to 85°C; ±0.25% FSO @ –40 to 125°C) *

Available Support

- Evaluation kit available
- Support for industrial mass calibration available
- Quick circuit customization possible for large production volumes

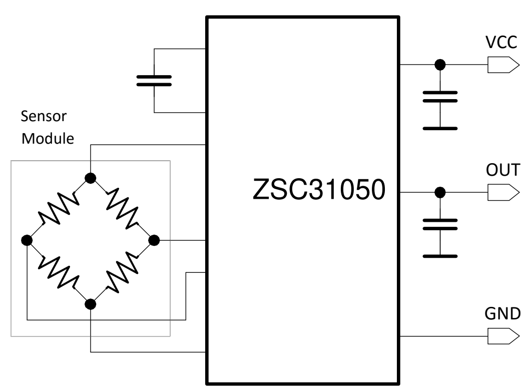
Features

- Digital compensation of sensor offset, sensitivity, temperature drift, and nonlinearity
- Accommodates nearly all resistive bridge sensor types (signal spans from 1mV/V up to 275mV/V)
- Digital one-pass calibration: quick and precise
- Selectable compensation temperature source: bridge, thermistor, or internal or external diode
- Output options: voltage (0 to 5V), current (4 to 20mA), PWM, I²C, SPI, ZACwire™ (one-wire interface), alarm
- Adjustable output resolution (up to 15 bits) versus sampling rate (up to 3.9kHz)
- Current consumption: 2.5mA (typical)
- Selectable bridge excitation: ratiometric voltage, constant voltage, or constant current
- Input channel for separate temperature sensor
- Sensor connection and common mode check (sensor aging detection)
- AEC-Q100 qualification (temperature grade 0)

Physical Characteristics

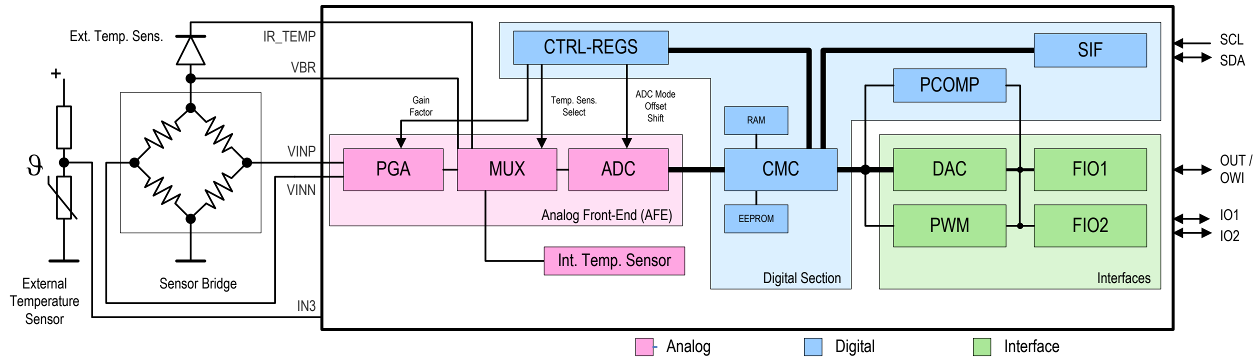
- Operation temperature -40°C to +125°C (-40°C to +150°C de-rated, depending on product version)
- Supply voltage: 2.7V to 5.5V;
  with external JFET: 5V to 48 V
- Available in 16-SSOP package or as die

Basic Circuit Diagram



* Digital output signal.

ZSC31050 Block Diagram



Typical Applications:

Consumer Goods
- Weight scales
- Flow meters
- Strain gauges
- Load meters
- HVAC

Industrial Applications
- 4-20mA transmitters
- Intelligent sensor networks
- Process automation
- Factory automation

Portable Devices
- Altimeters
- Blood pressure monitors

Automotive Sensors *
- Oil pressure
- Temperature sensing
- Strain gauges

* AEC-Q100 qualified

Ordering Information *(See section 8 in the data sheet for additional options.)*

Product Sales Code	Description	Package
ZSC31050FEB	ZSC31050 Die — Temperature range: -40°C to +150°C	Unsawn on Wafer
ZSC31050FEC	ZSC31050 Die — Temperature range: -40°C to +150°C	Sawn on Wafer Frame
ZSC31050FEG1	ZSC31050 16-SSOP — Temperature range: -40°C to +150°C	Add "-T" for tube or "-R" for reel to sales code
ZSC31050KITV3P1	ZSC31050 SSC Evaluation Kit V3.1: ZSC31050 Evaluation Board, SSC Communication Board, SSC Sensor Replacement Board, five ZSC31050 16-SSOP samples. Software is downloadable.	
ZSC31050MCSV1P1	Modular Mass Calibration System (MSC) V1.1 for ZSC31050: Four Mass Calibration Boards; SSC Communication Board; four ZSC31050 Mass Calibration Reference Boards, each with a ZSC31050 sample mounted; 30m 10-wire flat cable; 100 connectors. Software is downloadable.	

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1. Electrical Characteristics

1.1 Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. The ZSC31050 might not function or be operable above the recommended operating conditions. Stresses exceeding the absolute maximum ratings might also damage the device. In addition, extended exposure to stresses above the recommended operating conditions might affect device reliability. IDT does not recommend designing to the "Absolute Maximum Ratings."

No.	Parameter	Symbol	Conditions	Min	Max	Unit
1.1.1	Digital supply voltage	VDD_{MAX}	To VSS	-0.3	6.5	V DC
1.1.2	Analog supply voltage	$VDDA_{MAX}$	To VSS	-0.3	6.5	V DC
1.1.3	Voltage at all analog and digital I/O pins except FBP, SDA, SCL (see 1.1.4, 1.1.5, and 1.1.6)	$V_{A\_I/O}$, $V_{D\_I/O}$		-0.3	VDDA+0.3	V DC
1.1.4	Voltage at FBP pin	V_{FBP_MAX}	4mA to 20mA – Interface	-1.2	VDDA+0.3	V DC
1.1.5	Voltage at SDA pin	V_{SDA_MAX}	I²C mode only	-0.3	5.5	V DC
1.1.6	Voltage at SCL pin	V_{SCL_MAX}	I²C mode only	-0.3	5.5	V DC
1.1.7	Storage temperature	T_{STG}		-45	150	°C

1.2 Operating Conditions

Unless otherwise noted, voltages are relative to VSS and analog-to-digital conversion = 2nd order, resolution = 13 bits, gain ≥ 210, $f_{clk} \leq 2.25$MHz.

For specifications marked with an asterisk (*), there is no measurement in mass production—the parameter is guaranteed by design and/or quality observations.

Note: See important notes at the end of the table.

No.	Parameter	Symbol	Conditions	Min	Typical	Max	Unit
1.2.1	1.2.1.1 TQE ambient temperature range for part numbers ZSC31050x***E***xx	T_{AMB_TQE}	Operation life time < 1000h @ 125°C to 150°C	-40		150	°C
	1.2.1.2 TQA ambient temperature range for part numbers ZSC31050x***A***xx	T_{AMB_TQA}		-40		125	°C
	1.2.1.3 TQI ambient temperature range for part numbers ZSC31050x***I***xx	T_{AMB_TQI}		-25		85	°C
1.2.2	Ambient temperature EEPROM programming	T_{AMB_EEP}		-25		85	°C
1.2.3	EEPROM programming cycles					100	
1.2.4	Data retention (EEPROM)		Average temp. < 85°C	15			years

No.	Parameter	Symbol	Conditions	Min	Typical	Max	Unit
1.2.5	Analog supply voltage	VDDA	Ratiometric mode	2.7		5.5	V DC
1.2.6	Analog supply voltage advanced performance	$VDDA_{ADV}$	Ratiometric mode	4.5		5.5	V DC
1.2.7	Digital supply voltage	VDD	Externally powered			1.05	VDDA
				2.7			V DC
1.2.8	External supply voltage	V_{SUPP}	Voltage Regulator Mode with external JFET [a]	VDDA + 2V			V DC
1.2.9	Common mode input range[b]	V_{IN_CM}	Depends on gain adjust; refer to section 2.3.1	0.21		0.76	V_{ADC_REF}
1.2.10	Input voltage FBP pin	V_{IN_FBP}		-1		VDDA	V DC
1.2.11	Sensor bridge resistance [c] (over full temperature range)	R_{BR}		3.0		25.0	kΩ
		R_{BR_CL}	Current loop interface, 4 to 20mA	5.0		25.0	kΩ
1.2.12	Reference resistor for bridge current source *	R_{BR_REF}	Bridge current $I_{BR} = VDDA / (16 \cdot R_{BR\_REF})$	0.07			R_{BR}
1.2.13	Stabilization capacitor *	C_{VDDA}	External capacitor between VDDA and VSS	50	100	470	nF
1.2.14	VDD stabilization capacitor*, [d]	C_{VDD}	Between VDD and VSS, external	0	100	470	nF
1.2.15	Maximum load capacitance allowed at OUT [e]	C_{L_OUT}	Output Voltage Mode			50	nF
1.2.16	Minimum load resistance allowed	R_{L_OUT}	Output Voltage Mode	2			kΩ
1.2.17	Maximum load capacitance allowed at VGATE	C_{L_VGATE}	Total capacitance relative to all potentials			10	nF

[a] Maximum depends on the breakdown voltage of the external JFET; refer to the application recommendations in the *ZSC31050 Application Note—0-10V Output*.

[b] V_{ADC_REF}: reference voltage of the analog-to-digital converter (VBR or VDDA).

[c] No minimum limitation with an external connection between VDDA and VBR.

[d] Lower stabilization capacitors can increase noise level at the output.

[e] If the maximum is used, take into consideration the special requirements of the ZACwire™ interface stated in the *ZSC31050 Functional Description,* section 4.3.

1.3 Inherent Characteristics

For specifications marked with an asterisk (*), there is no measurement in mass production—the parameter is guaranteed by design and/or quality observations.

No.	Parameter	Symbol	Conditions	Min	Typ	Max	Unit
1.3.1	Selectable input span, bridge sensor measurement	V_{IN_SP}	Refer to section 2.3.1.	2		280	mV/V
1.3.2	Analog offset comp range (6 bit setting)			-20		20	Counts
			Maximum bias current [a]	-25		25	Counts
1.3.3	Analog-to-digital conversion (ADC) resolution	r_{ADC}	3-bit setting [b]	9		15	Bits
1.3.4	ADC input range	Range		10		90	%VDDA
1.3.5	Digital-to-analog conversion (DAC) resolution	r_{DAC}	At analog output		11		Bits
1.3.6	PWM resolution	r_{PWM}		9		12	Bits
1.3.7	Bias current for external temperature diodes	I_{TS}		8	18	40	µA
1.3.8	Sensitivity internal temperature diode [c]	ST_{T_SI}	Raw values without conditioning	2800	3200	3600	ppm FS/K
1.3.9	Clock frequency*	f_{CLK}	Guaranteed adjustment range	1	2	4	MHz

[a] Set configuration word ADJREF:BCUR (bits 4-6) to 111 (for details, see the *ZSC31050 Functional Description)*.

[b] 15-bit resolution is not applicable for 1st order ADC and not recommended for sensors with high nonlinearity behavior.

[c] FS = Full scale.

1.3.1 Cycle Rate versus ADC Resolution

The following specifications are guaranteed by design and/or quality observations.

Important note: Combining first-order configuration of the ADC with 15-bit resolution is not allowed.

ADC Order (O_{ADC})	Resolution r_{ADC}	Conversion Cycle f_{CYC}	
		f_{CLK}=2MHz	f_{CLK}=2.25MHz
	[Bit]	[Hz]	[Hz]
1	9	1302	1465
	10	781	879
	11	434	488
	12	230	259
	13	115	129
	14	59	67
2	11	3906	4395
	12	3906	4395
	13	1953	2197
	14	1953	2197
	15	977	1099

1.3.2 PWM Frequency

The following specifications are not measured in mass production; they are guaranteed by design and/or quality observations.

PWM Resolution r_{PWM} [Bit]	PWM Frequency in Hz at 2MHz Clock [a]				PWM Frequency in Hz at 2.25MHz Clock [b]			
	Clock Divider				Clock Divider			
	1	0.5	0.25	0.125	1	0.5	0.25	0.125
9	3906	1953	977	488	4395	2197	1099	549
10	1953	977	488	244	2197	1099	549	275
11	977	488	244	122	1099	549	275	137
12	488	244	122	61	549	275	137	69

[a] Internal RC oscillator: coarse adjustment to 1MHz, 2MHz, and 4MHz, fine-tuning +/- 25%; external clock is also possible.

[b] Internal RC oscillator: coarse adjustment to 1.125MHz, 2.25MHz, and 4.5MHz, fine-tuning +/- 25%; external clock is also possible.

1.4 Electrical Parameters

Unless otherwise noted, voltages are relative to VSS and analog-to-digital conversion = 2nd order, resolution = 13 bits, gain ≥210, f_{clk}≤2.25MHz.

Note: See important notes at the end of the table.

No.	Parameter	Symbol	Conditions	Min	Typ	Max	Unit
1.4.1	**Supply/Regulation**						
1.4.1.1	Supply current	I_{SUPP}	Without bridge and load current, bias adjustment ≤ 4, f_{CLK} ≤ 2.4MHz		2.5	4	mA
1.4.1.2	Supply current for current loop	I_{SUPP_CL}	Without bridge current, f_{CLK} ≤ 1.2MHz, bias [a] adjustment ≤ 1		2.0	2.75	mA
1.4.1.3	Temperature coefficient voltage reference *	TC_{REF}		-200	±50	200	ppm/K
1.4.2	**Analog Front End**						
1.4.2.1	Parasitic differential input offset current *	I_{IN_OFF}	Temperature range = T_{AMB_TQI} (-40 to 85°C)	-2 to -10		2 to 10	nA
1.4.3	**DAC and Analog Output (OUT Pin)**						
1.4.3.1	Output signal range [b]	V_{OUT_SR}	Voltage Mode, R_{LOAD} > 2KΩ $VDDA_{ADV}$ Temperature range = T_{AMB_TQI}	0.025		0.975	VDDA
1.4.3.2	Output DNL	DNL_{OUT}	$VDDA_{ADV}$ Temperature range = T_{AMB_TQI}			0.95	LSB
1.4.3.3	Output INL [c]	INL_{OUT}				4	LSB
1.4.3.4	Output slew rate *	SR_{OUT}	Voltage Mode Load capacitance < 20nF Using conditions of 1.4.3.1	0.1			V/µs
1.4.3.5	Short circuit current *	I_{OUT_max}		5	10	20	mA
1.4.3.6	Addressable output signal range *	V_{OUT_ADR}	2048 steps	0		1	VDDA
1.4.4	**PWM Output (OUT Pin, IO1 Pin)**						
1.4.4.1	PWM high voltage	V_{PWM_H}	Load resistance > 10kΩ	0.9			VDDA
1.4.4.2	PWM low voltage	V_{PWM_L}	Load resistance > 10kΩ			0.1	VDDA
1.4.4.3	PWM output slew rate *	SR_{PWM}	Load capacitance < 1nF	15			V/µs
1.4.5	**Temperature Sensors (IR_TEMP Pin)**						
1.4.5.1	Sensitivity external diode / resistor measurement	ST_{TS_E}	At r_{ADC} = 13 bits	75		210	µV/LSB

No.	Parameter	Symbol	Conditions	Min	Typ	Max	Unit
1.4.6	**Digital Outputs (IO1, IO2, OUT Pins in Digital Mode)**						
1.4.6.1	Output high level	V_{DOUT_H}	Load resistance > 1 kΩ	0.9			VDDA
1.4.6.2	Output low level	V_{DOUT_L}	Load resistance > 1 kΩ			0.1	VDDA
1.4.6.3	Output current *	I_{DOUT}		4			mA
1.4.7	**System Response**						
1.4.7.1	Startup time [d]	t_{STA}	Power-on to 1st measurement result at output	2		5	ms
1.4.7.2	Response time *	t_{RESP}	66% change in input signal; refer to Table 3 for f_{CON}	1.66	2.66	3.66	$1/f_{CON}$
1.4.7.3	Overall accuracy (deviation from ideal line including INL, gain, and offset errors) *, [e]	AC_{OUT}	T_{AMB_TQI} (-25 to 85 °C) & $VDDA_{ADV}$			0.10	%
			T_{AMB_TQA} (-40 to 125 °C) & $VDDA_{ADV}$			0.25	%
			T_{AMB_TQE} (-40 to 150 °C) & $VDDA_{ADV}$			0.50	%
1.4.7.4	Analog output noise: peak-to-peak *	$V_{NOISE,\ PP}$	Shorted inputs, gain ≤ 210 bandwidth ≤ 10kHz			10	mV
1.4.7.5	Analog output noise: RMS *	$V_{NOISE,\ RMS}$	Shorted inputs, gain ≤ 210 bandwidth ≤ 10kHz			3	mV
1.4.7.6	Ratiometricity error	RE_{OUT_5V}	±5% respectively 1000ppm ±10% (5V)			500	ppm
		RE_{OUT_3V}	±5% respectively 200ppm ±10% (3V)			1000	ppm

[a] Recommended bias adjustment ≤ 4; note the application recommendations and power consumption adjustment constraints given in the *ZSC31050 Application Note—Current Loop*.

[b] De-rated performance in lower part of supply voltage range (2.7 to 3.3V): 2.5 to 5 %VDDA and 95 to 97.5%VDDA.

[c] Output linearity and accuracy can be enhanced by an additional analog output stage calibration.

[d] OWI, start window disabled (depending on resolution and configuration, start routine begins approximately 0.8ms after power-on).

[e] Accuracy better than 0.5% requires offset and gain calibration for the analog output stage; parameter only for ratiometric output. The current loop application is verified and validated for 5V operation only and external supply > 7V (upper limit is dependent on the external components used). Accuracy and temperature range should be validated based on the schematic design used. Refer to the *ZSC31050 Application Note—Current Loop* for more information.

* For specifications marked with an asterisk (*), there is no measurement in mass production—the parameter is guaranteed by design and/or quality observations.

1.5 Interface Characteristics

No.	Parameter	Symbol	Conditions	Min	Typ	Max	Unit
1.5.1	**Multiport Serial Interfaces (I²C, SPI)**						
1.5.1.1	Input high level [a]	$V_{I2C\_IN\_H}$		0.7		1	VDDA
				-		5.5	V DC
1.5.1.2	Input low level	$V_{I2C\_IN\_L}$		0		0.3	VDDA
1.5.1.3	Output low level	$V_{I2C\_OUT\_L}$				0.1	VDDA
1.5.1.4	Load capacitance at the SDA pin	C_{SDA}				400	pF
1.5.1.5	Clock frequency at the SCL pin [b]	f_{SCL}	$f_{CLK} \geq 2MHz$			400	kHz
1.5.1.6	Pull-up resistor	R_{I2C_PU}		500			Ω
1.5.1.7	Input capacitance (each pin)	C_{I2C_IN}	Also valid for SPI.			10	pF
1.5.2	**One-Wire Serial Interface (ZACwire™)**						
1.5.2.1	OWI start window	t_{OWI_start}			20		ms
1.5.2.2	Pull-up resistance master	R_{OWI_PU}		330			Ω
1.5.2.3	OWI load capacitance	C_{OWI_LOAD}	$20\mu s < t_{OWI\_BIT} < 100\mu s$			0.08	t_{OWI_BIT} / R_{OWI_PU}
1.5.2.4	Voltage level low	V_{OWI_L}				0.2	VDDA
1.5.2.5	Voltage level high	V_{OWI_H}		0.75			VDDA

[a] The maximum value in V DC is independent from VDDA in I²C Mode.

[b] Internal clock frequency f_{CLK} must be at least 5 times higher than the communication clock frequency.

2. Circuit Description

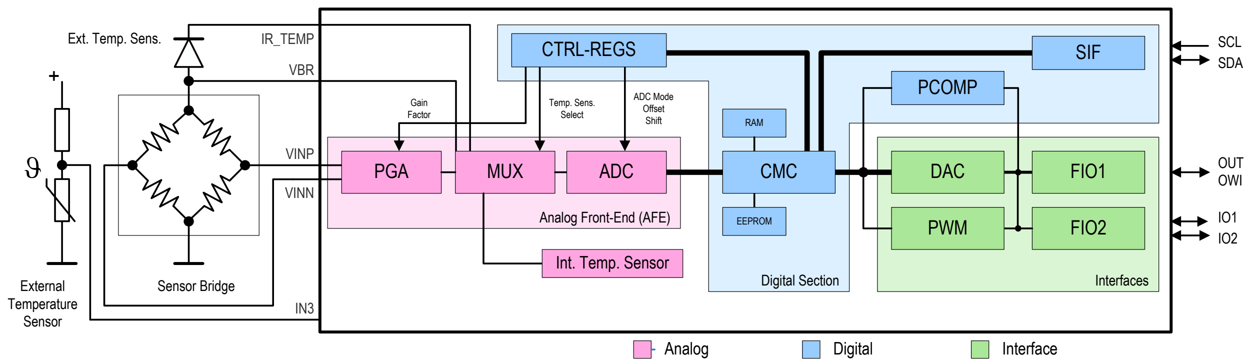
Note: This data sheet provides specifications and a general overview of ZSC31050 operation. For details of operation, including configuration settings and related EEPROM registers, refer to the *ZSC31050 Functional Description*.

2.1 Signal Flow

The ZSC31050's signal path includes both analog (shown in pink in Figure 1) and digital (blue) sections. The analog path is differential; i.e., the differential bridge sensor signal is handled internally via two signal lines that are symmetrical around a common mode potential (analog ground = VDDA/2), which improves noise rejection.

Therefore it is possible to amplify positive and negative input signals, which are located in the common mode range of the signal input.

Figure 1. Block Diagram of the ZSC31050



PGA	Programmable Gain Amplifier
MUX	Multiplexer
ADC	Analog-to-Digital Converter
CMC	Calibration Microcontroller
DAC	Digital-to-Analog Converter
FIO1	Flexible I/O 1: Analog Out (voltage/current), PWM2, ZACwire™ (one-wire-interface)
FIO2	Flexible I/O 2: PWM1, SPI Data Out, SPI Slave Select, Alarm1, Alarm2
SIF	Serial interface: I²C Data I/O, SPI Data In, Clock
PCOMP	Programmable Comparator
EEPROM	Nonvolatile Memory for Calibration Parameters and Configuration
TS	On-Chip Temperature Sensor (pn-junction)
ROM	Memory for Correction Formula and Algorithm
PWM	PWM Module

The differential signal from the bridge sensor is pre-amplified by the programmable gain amplifier (PGA). The multiplexer (MUX) transmits the signals from the bridge sensor, external diode, or separate temperature sensor to the ADC in a specific sequence (the internal pn-junction (TS) can be used instead of the external temperature diode). Next, the ADC converts these signals into digital values.

The digital signal correction takes place in the calibration microcontroller (CMC). It is based on a special correction formula located in the ROM and sensor-specific coefficients (stored in the EEPROM during calibration). Depending on the programmed output configuration, the corrected sensor signal is output as an analog value, a PWM signal, or a digital value in the format of SPI, I²C, or ZACwire™. The output signal is provided at two flexible I/O modules (FIO) and at the serial interface (SIF). The configuration data and the correction parameters can be programmed into the EEPROM via the digital interfaces.

The modular circuit concept used in the design of the ZSC31050 allows fast customization of the IC for high-volume applications if needed. Circuit blocks and functions can be added or removed, which can reduce the die size (see section 7 for more details).

2.2 Application Modes

For each application, a configuration set must be established (generally prior to calibration) by programming the on-chip EEPROM regarding to the following modes:

- **Sensor channel**
  - Sensor mode: ratiometric voltage or current supply mode.
  - Input range: the gain of the analog front end must be chosen with respect to the maximum sensor signal span, which also requires adjusting the zero point of the ADC.
  - Additional offset compensation, the Extended Zero-Point Compensation (XZC), must be enabled if required; e.g., if the sensor offset voltage is close to or larger than the sensor span.
  - Resolution/response time: The ADC must be configured for resolution and conversion settings (1st or 2nd order). These settings influence the sampling rate, signal integration time, and, as a result, the noise immunity.
  - Polarity of the sensor bridge inputs: this allows inverting the sensor bridge inputs

- **Analog output**
  - Choice of output type (voltage value, current loop, or PWM) for output register 1.
  - Optional additional output register 2: PWM via IO1 pin or alarm out module via IO1 or IO2 pin.

- **Digital communication:** The protocol and its parameters must be selected.

- **Temperature**
  - The temperature sensor type for the temperature correction must be chosen (only main channel (T1) is usable for correction).
  - Optional: a secondary temperature sensor (T2) can be chosen as a second sensor output.

- **Supply voltage:** For non-ratiometric output, the voltage regulation must be configured.

Note: Not all possible combinations of settings are allowed (see section 2.5).

The calibration procedure must include establishing the coefficients for calibration calculation and the following steps depending on configuration:

- Adjustment of the extended offset compensation
- Zero compensation of temperature measurement
- Adjustment of the bridge current
- Settings for the reference voltage if using the reference voltage
- Settings for the thresholds and delays for the alarms if using the alarms

2.3 Analog Front-End (AFE)

The analog front-end consists of the programmable gain amplifier (PGA), the multiplexer (MUX), and the analog-to-digital converter (ADC).

2.3.1 Programmable Gain Amplifier (PGA)

The following tables show the adjustable gains, the sensor signal spans that can be processed, and the common mode range allowed.

Table 1. Adjustable Gains, Resulting Sensor Signal Spans, and Common Mode Ranges

No.	PGA Gain a_{IN}	Gain Amp1	Gain Amp2	Gain Amp3	Max. Span V_{IN_SP} in mV/V	Input Range V_{IN_CM} in % VDDA‡
1	420	30	7	2	2	43 to 57
2	280	30	4.66	2	3	40 to 59
3	210	15	7	2	4	43 to 57
4	140	15	4.66	2	6	40 to 59
5	105	15	3.5	2	8	38 to 62
6	70	7.5	4.66	2	12	40 to 59
7	52.5	7.5	3.5	2	16	38 to 62
8	35	3.75	4.66	2	24	40 to 59
9	26.3	3.75	3.5	2	32	38 to 62
10	14	1	7	2	50	43 to 57
11	9.3	1	4.66	2	80	40 to 59
12	7	1	3.5	2	100	38 to 62
13	2.8	1	1.4	2	280	21 to 76

2.3.2 Extended Zero Point Compensation (XZC)

The ZSC31050 supports two methods of sensor offset cancellation (zero shift):

- Digital offset correction
- XZC – an analog cancellation for large offset values (up to approximately 300% of span)

The digital sensor offset correction is processed at the digital signal correction/conditioning by the CMC. The XZC analog sensor offset pre-compensation is needed for compensation of large offset values, which would overdrive the analog signal path due to uncompensated amplification. For analog sensor offset pre-compensation, a compensation voltage is added in the analog pre-gaining signal path (coarse offset removal). The analog offset compensation in the AFE can be adjusted by six EEPROM bits as described in the *ZSC31050 Functional Description*. It allows an analog zero-point shift of up to 300% of the segment of the signal span that can be processed.

‡ Bridge in voltage mode; refer to the *ZSC31050 Functional Description* for the usable input signal / common mode range at the bridge in current mode.

The zero-point shift Z_{XZC} of the temperature measurements can also be adjusted by six EEPROM bits (recommended Z_{XZC}= -20 to +20). It is calculated by equation (1):

$$\frac{V_{XZC}}{VDD_{BR}} = \frac{k \cdot Z_{XZC}}{20 \cdot a_{IN}} \qquad (1)$$

Where

V_{XZC} = Extended zero compensation voltage

VDD_{BR} = Bridge voltage

k = Calculation factor

a_{IN} = Input gain

Table 2. Extended Zero Point Compensation (XZC) Range

PGA Gain a_{IN}	Max. Span V_{IN_SP} (mV/V)	Calculation Factor k	Offset Shift per Step (% Full Span)	Approx. Maximum Offset Shift (mV/V)	Approx. Maximum Shift (% V_{IN_SP}) (@ ± 20 Steps)
420	2	3.0	15%	+/- 7	330
280	3	1.833	9%	+/- 6	200
210	4	3.0	15%	+/- 14	330
140	6	1.833	9%	+/- 12	200
105	8	1.25	6%	+/- 12	140
70	12	1.833	9%	+/- 24	200
52.5	16	1.25	6%	+/- 22	140
35	24	1.833	9%	+/-48	200
26.3	32	1.25	6%	+/- 45	140
14	50	3.0	15%	+/- 180	330
9.3	80	1.833	9%	+/- 160	200
7	100	1.25	6%	+/- 140	140
2.8	280	0.2	1%	+/- 60	22

Note: Z_{XZC} can be adjusted in the range of –31 to 31; however, parameters are guaranteed only for -20 to 20.

2.3.3 Measurement Cycle Performed by Multiplexer

Depending on EEPROM settings, the multiplexer selects the following inputs in a set sequence as shown in Figure 2.

Refer to the *ZSC31050 Functional Description* for EEPROM details.

- Internal offset of the input channel (auto-zero) measured by short circuiting the input
- Bridge temperature signal measured by external and internal diode (pn-junction)
- Bridge temperature signal measured by bridge resistors
- Temperature measured by external thermistor
- Pre-amplified bridge sensor signal

The complete measurement cycle is controlled by the CMC. The cycle diagram at the right shows its principle structure.

The EEPROM adjustable parameters are

- Measurement count n (bits 9:7 in configuration word CFGCYC): n =<1, 2, 4, 8, 16, 32, 64, 128>
- Temperature 2 measurement enable, T2E=<0, 1>

After power-on, the start routine is called. It includes the bridge sensor and auto-zero measurement. It also measures the main temperature channel and its auto-zero if enabled.

Figure 2. Measurement Cycle ZSC31050

→ Start Routine

n	*Bridge sensor measurement*
1	Temp 1 auto-zero
n	*Bridge sensor measurement*
1	Temp 1 measurement
n	*Bridge sensor measurement*
1	Bridge sensor auto-zero
n ⋆ T2E	*Bridge sensor measurement*
T2E	Temp 2 auto-zero
n ⋆ T2E	*Bridge sensor measurement*
T2E	Temp 2 measurement
n	*Bridge sensor measurement*
1	Common mode voltage

2.3.4 Analog-to-Digital Converter

The ADC is a charge-balancing converter using full differential switched capacitor technique. It can be used as a first or second order converter:

In the **first order** mode, the ADC is inherently monotone and insensitive against short and long term instability of the clock frequency. The conversion cycle time depends on the desired resolution and can be roughly calculated by equation (2):

$$t_{CYC\_1} = 2^{r_{ADC}} [\mu s] \qquad (2)$$

The available ADC resolutions are r_{ADC} = <9, 10, 11, 12, 13, 14>.

In the **second order** mode, two conversions are stacked with the advantage of a much shorter conversion cycle time but with the drawback of a lower noise immunity caused by the shorter signal integration period. The conversion cycle time in this mode is roughly calculated by equation (3):

$$t_{CYC\_2} = 2^{\left(\frac{r_{ADC}+3}{2}\right)} [\mu s] \qquad (3)$$

The available ADC resolutions are r_{ADC} = <11, 12, 13, 14, 15>.

The result of the AD conversion is a relative counter result corresponding to equation (4):

$$Z_{ADC} = 2^{r_{ADC}} \cdot \left(\frac{V_{ADC\_DIFF} + V_{ADC\_OFF}}{V_{ADC\_REF}} + 1 - RS_{ADC} \right) \qquad (4)$$

Z_{ADC} Number of counts; i.e., the result of the conversion)

V_{ADC_DIFF} Differential input voltage of ADC: (a_{IN} * V_{IN_DIFF})

V_{ADC_REF} Reference voltage of ADC: (VBR or VDDA)

V_{ADC_OFF} Residual offset voltage of analog front-end to ADC

RS_{ADC} Digital ADC range shift (RS_{ADC} = $^1/_2$, $^3/_4$, $^7/_8$, $^{15}/_{16}$, controlled by EEPROM setting)

A sensor input signal can be shifted via the RS_{ADC} value into the optimal input range of the ADC.

The potential at the VBR pin is used as the ADC's reference voltage V_{ADC_REF} in "V_{ADC_REF} = VBR" mode. The mode is determined by the CFGAPP:ADCREF configuration register in EPPROM as described in the *ZSC31050 Functional Description*. Sensor bridges with no ratiometric behavior (e.g., temperature-compensated bridges) that are supplied by a constant current, require the VDDA potential as V_{ADC_REF} and this can be adjusted in the configuration. If this mode is enabled, XZC cannot be used (adjustment=0), but it must be enabled (refer to the calculation spreadsheet *ZSC31050_Bridge_Current_Excitation_Rev*.xls* for details).

Note: The AD conversion time (sample rate) is only part of the complete signal conditioning cycle.

Table 3. Output Resolution versus Sample Rate

ADC Order (O_{ADC})	Maximum Output Resolution				Sample Rate f_{CON}	
	r_{ADC} § (Bit)	Digital OUT (Bit)	Analog OUT (Bit)	r_{PWM} (Bit)	f_{CLK}=2MHz (Hz)	f_{CLK} =2.25MHz (Hz)
1	9	9	9	9	1302	1465
	10	10	10	10	781	879
	11	11	11	11	434	488
	12	12	11	12	230	259
	13	13	11	12	115	129
	14	14	11	12	59	67
2	10	10	10	10	3906	4395
	11	11	11	11	3906	4395
	12	12	11	12	3906	4395
	13	13	11	12	1953	2197
	14	14	11	12	1953	2197
	15	15	11	12	977	1099

§ ADC resolution should be 1 to 2 bits higher than applied output resolution

2.4 System Control

The system control is started by the internal power-on reset (POR) using the internal clock generator or an external clock. It has the following features:

- Control of the I/O functions and the measurement cycle using the EEPROM-stored configuration settings.
- 16-bit correction calculation for each measurement signal using the EEPROM-stored calibration coefficients and ROM-based algorithms.
- Error checking: To increase safety, the EEPROM data are verified via an EEPROM signature during the initialization procedure and the registers of the CMC are continuously observed with a parity check. If an error is detected, the error flag of the CMC is set and the outputs are driven to a diagnostic value. See section 2.7.

Note: Conditioning options include up to third-order sensor input correction (de-rated). The available adjustment ranges depend on the specific calibration parameters; basically, offset compensation and linear correction are only limited by the loss of resolution the compensation will cause. The second-order correction is possible up to approximately 20% of the full-scale difference from a straight line; third-order is possible up to approximately 10% (ADC resolution = 13 bits). The temperature calibration includes first and second order correction, which should be sufficient in almost all applications. ADC resolution also affects calibration options – each additional bit of resolution reduces the calibration range by approximately 50%.

2.5 Output Stage

The ZSC31050 provides the following I/O pins: OUT, IO1, IO2, and SDA. The signal formats listed in Table 4 can be output via these pins: analog (voltage or current), PWM, data (SPI/I²C), alarm. The following values can be provided at the I/O pins: bridge sensor signal, temperature signal 1, temperature signal 2, and alarms.

Note: *The alarm signals (Alarm 1 and Alarm 2) only apply to the bridge sensor signal; they cannot be used as an alarm for the temperature signal.*

Because some pins are dual-purpose, there are restrictions on the possible combinations for outputs and interface connections. Table 4 gives an overview of valid combinations. For some combinations in the SPI Mode, pin assignments depend on whether the ZSC31050 is in the Command Mode (CM) or the Normal Operation Mode (NOM) as indicated in the “Mode” column (refer to the *ZSC31050 Functional Description* for more details).

Note: *In the SPI Mode, the IO2 pin is used as the Slave Select, so no Alarm 2 can be output in this mode.*

Table 4. Output Configurations Overview

Configuration Number	SIF		I/O Pins Used				Mode
	I²C	SPI	OUT	IO1	IO2	SDA	
1	✓					Data I/O	
2	✓			ALARM1		Data I/O	
3	✓				ALARM2	Data I/O	
4	✓			ALARM1	ALARM2	Data I/O	
5	✓			PWM1		Data I/O	
6	✓			PWM1	ALARM2	Data I/O	
7	✓		Analog			Data I/O	
8	✓		Analog	ALARM1		Data I/O	
9	✓		Analog		ALARM2	Data I/O	
10	✓		Analog	ALARM1	ALARM2	Data I/O	
11	✓		Analog	PWM1		Data I/O	

Configuration Number	SIF		I/O Pins Used				Mode
	I^2C	SPI	OUT	IO1	IO2	SDA	
12	✓		Analog	PWM1	ALARM2	Data I/O	
13	✓		PWM2			Data I/O	
14	✓		PWM2	ALARM1		Data I/O	
15	✓		PWM2		ALARM2	Data I/O	
16	✓		PWM2	ALARM1	ALARM2	Data I/O	
17	✓		PWM2	PWM1		Data I/O	
18	✓		PWM2	PWM1	ALARM2	Data I/O	
19		✓		Data out (SDO)	Slave select	Data in	
20		✓		Data out (SDO)	Slave select	Data in	CM
				ALARM1	-	-	NOM
21		✓		Data out	Slave select	Data in	CM
				PWM1	-	-	NOM
22		✓	Analog	Data out	Slave select	Data in	
23		✓	Analog	Data out	Slave select	Data in	CM
				ALARM1	-	-	NOM
24		✓	Analog	Data out	Slave select	Data in	CM
				PWM1	-	-	NOM
25		✓	PWM2	Data out	Slave select	Data in	
26		✓	PWM2	Data out	Slave select	Data in	CM
				ALARM1	-	-	NOM
27		✓	PWM2	Data out	Slave select	Data in	CM
				PWM1	-	-	NOM

2.5.1 Analog Output

For analog output, three 15-bit registers store the compensated measurement results for the bridge sensor signal and temperature measurements 1 and 2. Each register can be independently switched to either the digital-to-analog converter module (DAC) or the PWM module (see Figure 1) and then output via the FIO1 or FIO2 output module connected to the OUT or IO1 pin respectively according to Table 5. Refer to the *ZSC31050 Functional Description* for details.

Table 5. Analog Output Configuration

Output Module	OUT	IO1
Voltage (DAC)	✓	
PWM	✓	✓

The voltage output module consists of an 11-bit resistor string DAC with a buffered output and a subsequent inverting amplifier with a class AB rail-to-rail operational amplifier. The two internal feedback networks are connected to the FBN and FBP pins. This structure offers wide flexibility for the output configuration; for example, voltage output and 4mA to 20mA current loop output. Accidentally short-circuiting the analog output to VSS or VDDA does not damage the ZSC31050.

The PWM module outputs the analog measurement value via a stream of pulses with a duty cycle that is determined by the analog value. The PWM frequency depends on the resolution and clock divider settings. The maximum analog output resolution is 12 bits; however the maximum PWM frequency is 4kHz (9 bits). If both PWM2 and SPI protocol are activated (configuration numbers 25, 26, and 27 in Table 4), the output IO1 pin is shared between the PWM output and the SPI SDO output of the serial interface, and SPI interface communication (Command Mode) interrupts the PWM output.

2.5.2 Comparator Module (ALARM Output)

The comparator module consists of two comparator channels that can be connected to IO1 and IO2. Each can be independently programmed for threshold, hysteresis, switching direction, and on/off delay. A window comparator mode is also available.

2.5.3 Serial Digital Interface

The ZSC31050 includes a serial digital interface that is able to communicate in three different communication protocols: I^2C, SPI, and ZACwire™ (one-wire communication). In SPI mode, the IO2 pin operates as the slave-select input, and the IO1 pin is the data output (SDO).

Initializing Communication

After power-on for approximately 20ms (the start window), the ZSC31050 interface is in the ZACwire™ mode, which allows communication via the one-wire interface (the OUT pin).

If a proper communication request is detected during the start window, the interface stays in the ZACwire™ mode (the Command Mode). This state can be left by set commands or a new power-on.

If no request is received during the start window, then the serial interface switches to communication via either I^2C or SPI mode depending on EEPROM settings. The OUT pin can be used as an analog output or as a PWM output depending on EEPROM settings. The start window can be disabled (or enabled) by a special EEPROM setting.

For a detailed description of the serial interfaces, see the *ZSC31050 Functional Description*.

2.6 Voltage Regulator

For 3V to 5V (±10%) ratiometric output applications, the external supply voltage can be used for sensor element biasing. If an absolute analog output is required, then the internal voltage regulator with an external power regulation element (JFET) can be used. The regulation is bandgap-reference-based and designed for an external supply voltage V_{SUPP} in the range of 7V to 48V DC. The internal supply and sensor bridge voltage can be varied between 3V and 5.5V in four steps with the voltage regulator as determined by a configuration word in EEPROM.

2.7 Watchdog and Error Detection

The ZSC31050 detects various possible errors. A detected error is signaled by changing to a diagnostic mode. In this case, the analog output is set to the high or low level (maximum or minimum possible output value) depending on the error and the output registers of the digital serial interface are set to a correlated error code.

A watchdog continuously monitors the operation of the CMC and the progress of the measurement loop.

A continuous check of the sensor bridge for broken wires is done by two comparators monitoring the input voltage of each input [(VSSA + 0.5V) to (VDDA – 0.5V)]. The common mode voltage of the sensor is continuously monitored to detect sensor aging.

Different functions and blocks in the digital section are continuously monitored, including the RAM, ROM, EEPROM, and register contents.

See section 1.3.4 in the *ZSC31050 Functional Description* for a detailed description of all monitored blocks and methods of indicating errors.

3. Application Circuit Examples

Figure 3. Application Example 1

Typical ratiometric measurement with voltage output, temperature compensation via external diode, internal VDD regulator, and active sensor connection check (bridge must not be at VDDA)

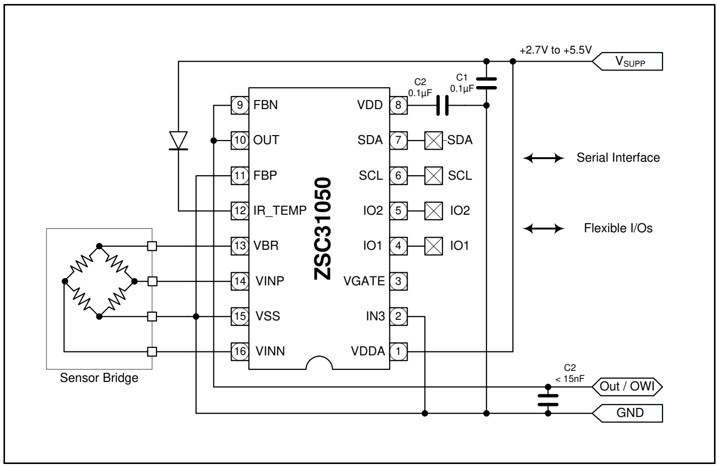


Figure 4. Application Example 2

0V to 10V output configuration with supply regulator (external JFET), temperature compensation via internal diode, and bridge in voltage mode

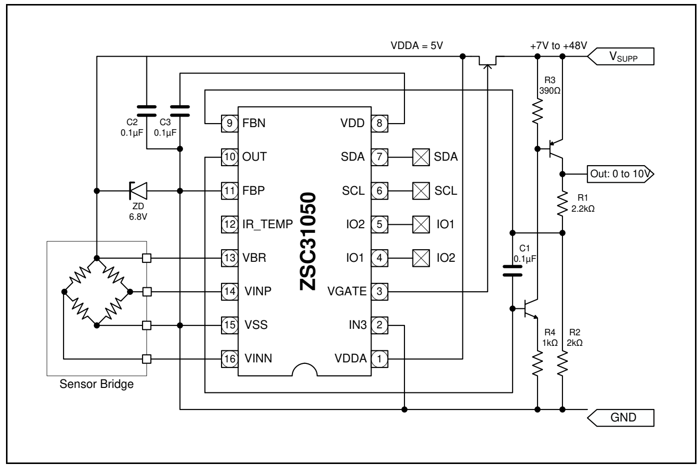


Figure 5. Application Example 3

Absolute voltage output, supply regulator (external JFET), constant current excitation of the sensor bridge, temperature compensation by bridge voltage drop measurement, internal VDD regulator without external capacitor

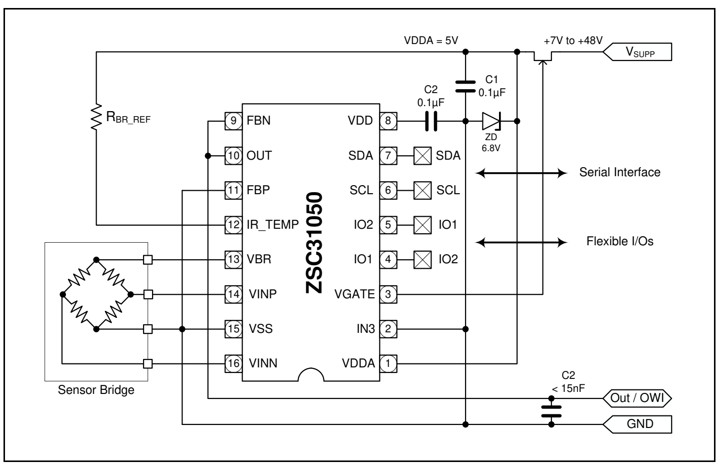


Figure 6. Application Example 4

Ratiometric bridge differential signal measurement, 3–wire connection for end-of-line calibration at OUT pin (ZACwire™), additional temperature measurement with external thermistor, and PWM output at IO1 pin

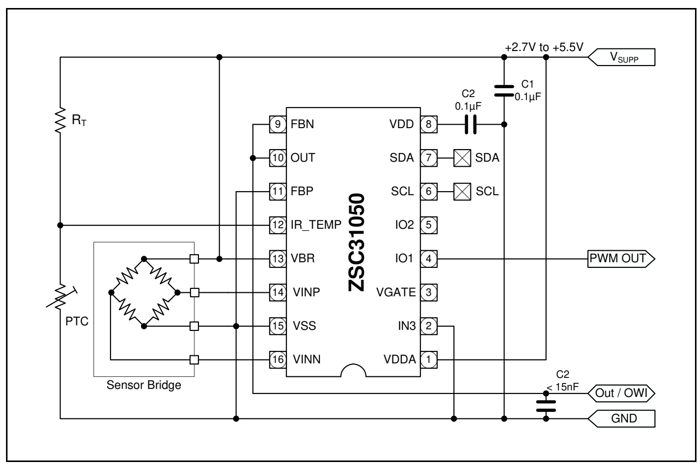
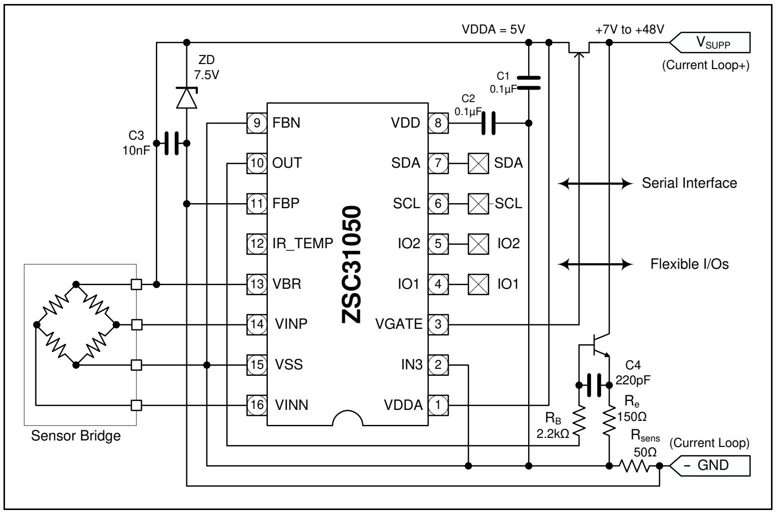


Figure 7. Application Example 5

Two-wire 4mA to 20mA configuration (7 to 48 V), temperature compensation via internal diode



Note: It is possible to combine or separate connectivity of different application examples. For VDD generation, IDT recommends using the internal supply voltage regulator with an external capacitor. Refer the *ZSC31050 Application Note—Current Loop* for use of supply voltage regulation features (non-ratiometric mode) and current loop output mode.

4. ESD/Latch-Up-Protection

All pins have an ESD protection of >2000V, except the VINN, VINP, and FBP pins, which have an ESD protection >1200V. All pins have a latch-up protection of ±100mA or +8V/ –4V (relative to VSS/VSSA). Refer to section 5 for details and restrictions. ESD protection referenced to the Human Body Model is tested with devices in 16-SSOP packages during product qualification. The ESD test follows the Human Body Model with 1.5kOhm/100pF based on MIL 883, method 3015.7.

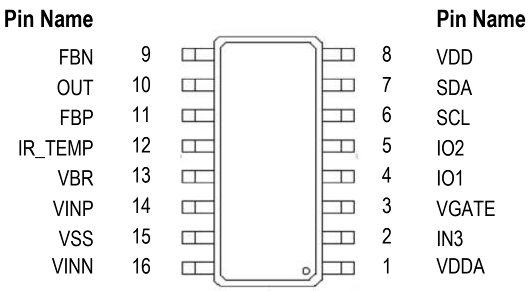
5. Pin Configuration and Package

Table 6. Pin Configuration

Pin	Name	Description	Remarks	Latch-up Related Application Circuit Restrictions and/or Remarks
1	VDDA	Positive analog supply voltage	Supply	
2	IN3	Resistive temperature sensor IN and external clock IN	Analog IN	Freely accessible by application (vulnerable to latch-up if specifications in section 4 are exceeded)
3	VGATE	Gate voltage for external regulator FET	Analog OUT	Only connection to external JFET
4	IO1	SPI data out or ALARM1 or PWM1 Output	Digital IO	Freely accessible by application
5	IO2	SPI slave select or ALARM2	Digital IO	Freely accessible by application
6	SCL	I^2C clock or SPI clock	Digital IN, pull-up	Freely accessible by application
7	SDA	Data I/O for I^2C or data IN for SPI	Digital I/O, pull-up	Freely accessible by application
8	VDD	Positive digital supply voltage	Supply	Only capacitor to VSS is allowed; otherwise no application access
9	FBN	Negative feedback connection output stage	Analog I/O	Freely accessible by application
10	OUT	Analog output or PWM2 output or one-wire interface I/O	Analog OUT or Digital I/O	Freely accessible by application
11	FBP	Positive feedback connection output stage	Analog I/O	Freely accessible by application
12	IR_TEMP	Current source resistor I/O and temperature diode in	Analog I/O	Circuitry secures potential is within VSS-VDDA range; otherwise no application access
13	VBR	Bridge top sensing in bridge current out	Analog I/O	Only short to VDDA or connection to sensor bridge; otherwise no application access
14	VINP	Positive input from sensor bridge	Analog IN	Freely accessible by application
15	VSS	Negative supply voltage	Ground	
16	VINN	Negative input from sensor bridge	Analog IN	Freely accessible by application

The standard package for the ZSC31050 is a 16-SSOP (5.3mm body width) with lead-pitch 0.65mm:

Figure 8. Pin Configuration



6. Reliability

The ZSC31050 is qualified according to the AEC-Q100 standard, operating temperature grade 0. A fit rate < 5fit (temp=55°C, S=60%) is guaranteed. A typical fit rate of the C7A technology that is used for the ZSC31050 is 2.5fit.

7. Customization

For high-volume applications that require an upgraded or downgraded functionality compared to the ZSC31050, IDT can customize the circuit design by adding or removing certain functional blocks.

IDT has a considerable library of sensor-dedicated circuitry blocks that enable IDT to provide a custom solution quickly. Please contact IDT for further information.