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Description

The ZSSC3123 is a CMOS integrated circuit for accurate capacitance-to-digital conversion and sensor-specific correction of capacitive sensor signals. Digital compensation of sensor offset, sensitivity, and temperature drift is accomplished via an internal digital signal processor running a correction algorithm with calibration coefficients stored in a non-volatile EEPROM.

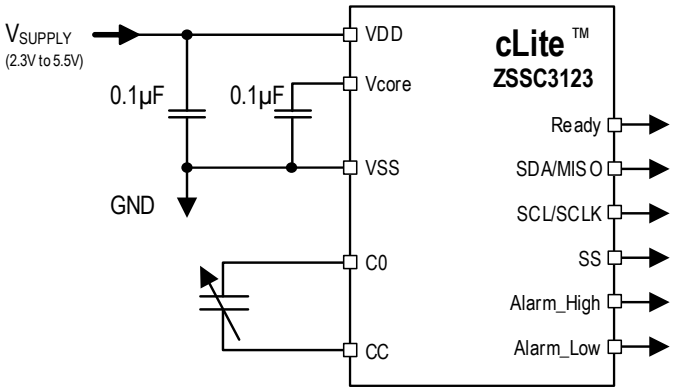
The ZSSC3123 is configurable for capacitive sensors with capacitances up to 260pF and a sensitivity of 125aF/LSB to 1pF/LSB depending on resolution, speed, and range settings. It is compatible with both single capacitive sensors (both terminals must be accessible) and differential capacitive sensors. Measured and corrected sensor values can be output as I2C, SPI, pulse density modulation (PDM), or alarms.

The I2C interface can be used for a simple PC-controlled calibration procedure to program a set of calibration coefficients into an on-chip EEPROM. The calibrated ZSSC3123 and a specific sensor are mated digitally: fast, precise, and without the cost overhead of trimming by external devices or laser.

Available Support

- ZSSC3123 SSC Evaluation Kit available: SSC Evaluation Board, samples, software, documentation.
- Support for industrial mass calibration available.
- Quick circuit customization option for large production volumes.

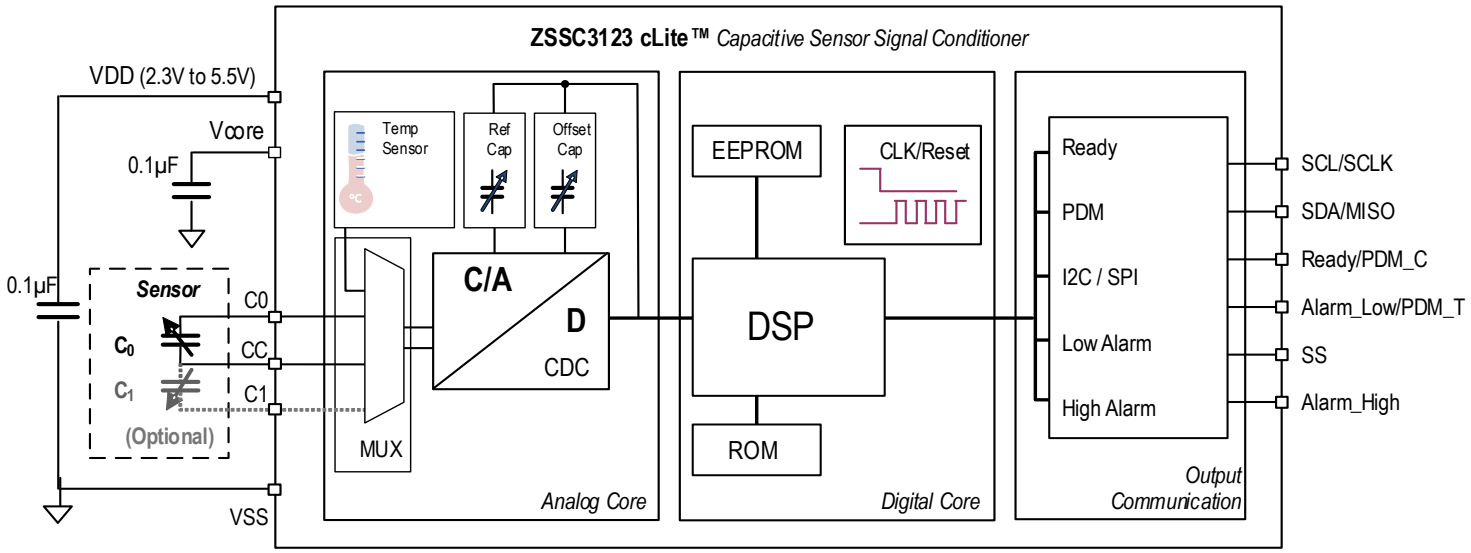
Application: Digital Output, Alarms



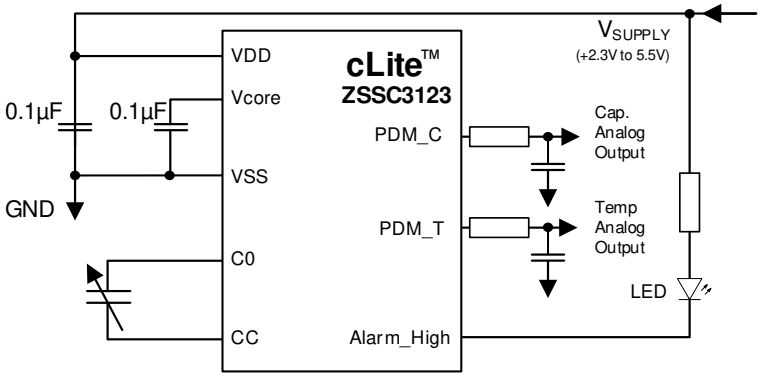
Features

- Maximum target input capacitance: 260pF
- Sampling rates as fast as 0.7ms at 8-bit resolution; 1.6ms at 10-bit; 5.0ms at 12-bit; 18.5ms at 14-bit
- Digital compensation of sensor: piece-wise 1st and 2nd order sensor compensation or up to 3rd order single-region sensor compensation
- Digital compensation of 1st and 2nd order temperature gain and offset drift
- Internal temperature compensation reference (no external components)
- Programmable capacitance span and offset
- Layout customized for die-die bonding with sensor for low-cost, high-density chip-on-board assembly
- Accuracy as high as ±0.25% FSO at -40°C to 125°C, 3V, 5V, Vsupply ±10% (see data sheet section 5 for restrictions)
- Minimized calibration costs: no laser trimming, one-pass calibration using a digital interface
- Wide capacitance range to support a broad portfolio of different sensor elements
- Excellent for low-power battery applications
- I2C or SPI interface—easy connection to a microcontroller
- PDM outputs (Filtered Analog Ratiometric) for both capacitance and temperature
- Up to two alarms that can act as full push-pull or open-drain switches
- Supply voltage: 2.3V to 5.5V
- Typical current consumption 750µA down to 60µA depending on configuration
- Typical Sleep Mode current: ≤ 1µA at 85°C
- Operation temperature: –40°C to +125°C depending on part code
- Die or 4.4 × 5.0 mm 14-TSSOP package

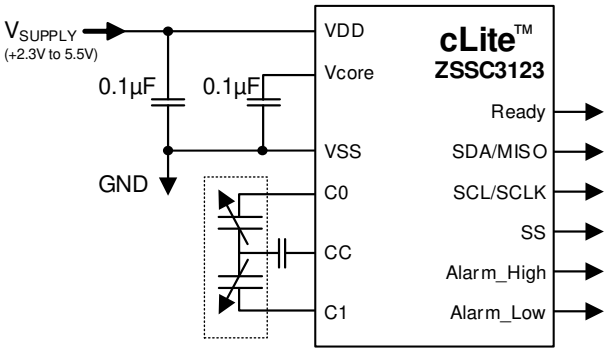
Block Diagram



Application: Analog Output



Application: Differential Capacitance Input



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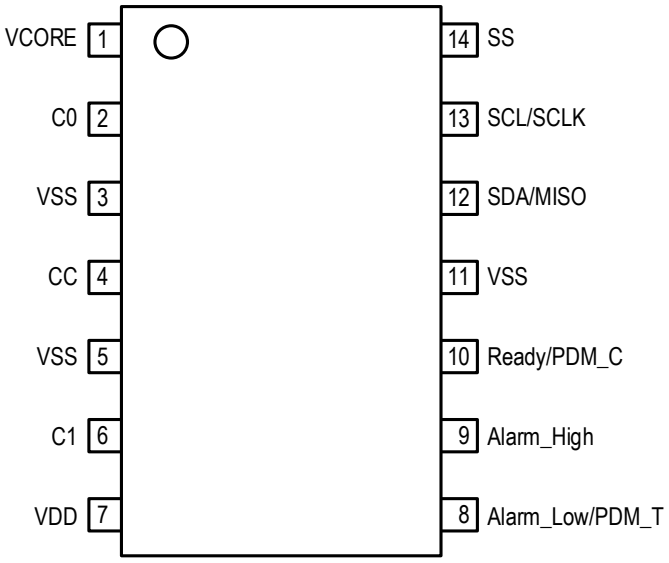
1. Pin Assignments

Figure 1. Pin Assignments for 4.4mm × 5.0mm 14-TSSOP – Top View



2. Pin Descriptions

Table 1. Pin Descriptions

Pin	Name	Description	Notes
1	VCORE	Core voltage	Always connect the VCORE pin to an external capacitor to ground that is within the specifications given in section 4 for C_{VCORE_SM} and C_{VCORE_UM}. This is the only internal module pin. For ESD details, see section 15.
2	C0	Capacitor input 0	
3	VSS	Ground supply	Connecting to GND for shielding is strongly recommended.
4	CC	Common capacitor input	
5	VSS	Ground supply	Connecting to GND for shielding is strongly recommended.
6	C1	Capacitor input 1	If not used, must be unconnected.
7	VDD	Supply voltage (1.8V to 5.5V) 2.3V to 5.5V for ZSSC3123	VDD must be connected to V_{SUPPLY}. See section 4.
8	Alarm_Low/PDM_T	Low alarm output Temperature PDM (see Table 20)	If not used, must be unconnected.
9	Alarm_High	High alarm output	If not used, must be unconnected.

Pin	Name	Description	Notes
10	Ready/PDM_C	Ready signal (conversion complete output) Capacitance PDM (see Table 20)	If not used, must be unconnected.
11	VSS	Ground supply	Must connect to GND.
12	SDA/MISO	I2C data if in I2C Mode Master-In-Slave-Out if in SPI Mode (see Table 20)	If not used, must connect to VDD.
13	SCL/SCLK	I2C clock if in I2C Mode Serial clock if in SPI Mode (see Table 20)	If not used, must connect to VDD.
14	SS	Slave Select (input) if in SPI Mode (see Table 20)	If not used, must be unconnected.

3. Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed in Table 2 can cause permanent damage to the device. Functional operation of the device at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Minimum	Typical	Maximum	Units
V_{DD}	Analog Supply Voltage	-0.3		6.0	V
V_{INA}	Voltages at Analog I/O – In Pin	-0.3		V_{DD}+0.3	V
V_{OUTA}	Voltages at Analog I/O – Out Pin	-0.3		V_{DD}+0.3	V
T_{STOR}	Storage Temperature Range	-55		150	°C

4. Recommended Operating Conditions

Table 3. Recommend Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Units
V_{SUPPLY}	Supply Voltage to Ground	2.3		5.5	V
T_{AMB}	Ambient Temperature Range[a]	-40		125	°C
I_{OUT}	Output Pads/Pins Drive Strength[b]	1.5		20	mA
$C_{VSUPPLY}$	External Capacitance between V_{DD} pin and Ground	100	220	470	nF
C_{VCORE_SM}	External Capacitance between Vcore and Ground – Sleep Mode	10		110	nF
C_{VCORE_UM}	External Capacitance between Vcore and Ground – Update Mode	90		330	nF
C_0	Input Capacitance Span (Full Scale Values)	2		260	pF
C_1	External Reference Capacitance	2		260	pF
C_{CC}	External Isolating Capacitance (Mult1) (CC pin to sensor common node) [c], [d]			16	pF
R_{PU}	I2C Pull-up Resistor	1	2.2		kΩ
C_{SDA}	SDA/MISO Load Capacitance			200	pF

[a] Caution: If buying die, select the proper package to ensure that the maximum junction temperature is not exceeded.

[b] See section 7 for full details on output pad drive strengths.

[c] An external isolating capacitor allows a non-galvanic connection to special differential or external reference sensor types. C_{CC} could also be used to lower the overall capacitance level to a value that is supported by the ZSSC3123 because it limits the maximum capacitance seen by the ZSSC3123 input to CC even if C0 and C1 have higher values. See section 9.2.1.3 for more details.

[d] The series combination of sensor and CC must not exceed the maximum capacitance allowed for the chosen Mult setting.

5. Electrical Characteristics

Table 4. Electrical Characteristics

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
Supply Current						
I_{DD}	Update Mode Current (varies with part configuration) [a]	Best case settings: [b] Mult 1, 8-bit, 125ms Power Down		60	100	µA
		Worst case settings: Mult 1, 14-bit, 0ms Power Down		750	1100	
I_{PDM}	Extra Current with PDM enabled [b]			150		µA
I_{SLEEP}	Sleep Mode Current [a]	-40 to 85°C		0.6	1	µA
		-40 to 125°C		1	3	µA
Voltage Levels						
V_{POR}	Power-On-Reset Level		1.6	1.7	2.2	V
V_{REG}	Active Regulated Voltage	Note: Regulated voltage can be measured on the Vcore pin.	2.4	2.55	2.7	V
Capacitance-to-Digital Converter (CDC)						
RES_{CDC}	Resolution		8		14	Bits
f_{MULT1}	Excitation Frequency of External Capacitances C0 and C1 (for a system frequency f_{SYS})	Mult 1		$f_{SYS}/2$		kHz
f_{MULT2}		Mult 2		$f_{SYS}/4$		kHz
f_{MULT4}		Mult 4		$f_{SYS}/8$		kHz
f_{MULT8}		Mult 8		$f_{SYS}/16$		kHz
INL_{CDC}	Integral Nonlinearity (INL) [c]	Mult 1, 10% to 90% input, 14-bit			0.2	%
DNL_{CDC}	Differential Nonlinearity (DNL) [b]	Mult 1, 10% to 90% input, 14-bit			0.9	LSB
EEPROM						
n_{WRI_EEP}	Number of Erase/Write Cycles	At 85°C			100k	
t_{WRI_EEP}	Data Retention	At 100°C			10	Year
Temperature Conversion						
RES_{TEMP}	Resolution in °C [b]	-40 to 125°C, 8-bit mode	0.64	0.96	1.6	°C
		-40 to 125°C, 14-bit mode	0.01	0.015	0.025	
INL_{CDC}	Nonlinearity First Order Fit [b], [d]	-40 to 125°C		±0.5	±1	°C
INL_{CDC}	Nonlinearity Second Order Fit [b], [e]	-40 to 125°C		±0.2	±0.4	°C
PSR_{TEMP}	Voltage Dependency [b]	$V_{SUPPLY} > V_{REG}+0.25V$		0.03	0.1	°C/V
		$2.3V \le V_{SUPPLY} \le V_{REG} + 0.25V$		1.25	2.25	

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
PDM Output						
V_{PDM_Range}	Output Range [b]		10		90	$\%V_{SUPPLY}$
f_{PDM}	PDM Frequency			$f_{SYS}/8$		kHz
t_{SETT}	Filter Settling Time [b], [f]	0% to 90% LP filter 10kΩ/400nF			9.2	ms
V_{RIPP}	Ripple [b], [f]	0% to 90% LP filter 10kΩ/400nF			1.0	mV/V
E_{PDM}	PDM Additional Error (Including Ratiometricity Error) [b]	-40 to 125°C		0.1	0.5	%
Digital I/O						
V_{OL}	Voltage Output Level Low			0	0.2	V_{SUPPLY}
V_{OH}	Voltage Output Level High		0.8	1		V_{SUPPLY}
V_{IL}	Voltage Input Level Low			0	0.2	V_{SUPPLY}
V_{IH}	Voltage Input Level High		0.8	1		V_{SUPPLY}
C_{IN}	Communication Pin Input Capacitance [b]				10	pF
Total System						
C_{tol}	Capacitive Tolerance Between Parts [b]	All capacitive values in the specification are subject to this variation			±10	%
f_{SYS}	Trimmed System Frequency	All timing in this specification is subject to this variation.	1.76	1.85	1.94	MHz
f_{var}	Frequency Variation Over Voltage and Temperature	All timing in this specification is subject to this variation.			±10	%
t_{STA}	Start-Up-Time [b], [g], [h] Power-on (POR) to data ready	Fastest and slowest settings	4.25		173	ms
t_{RESP_UP}	Update Rate (Update Mode) [b], [g], [h]	Fastest and slowest settings	0.70		288	ms
t_{RESP_SL}	Response Time (Sleep Mode) [b], [g], [h]	Fastest and slowest settings	1.25		163	ms
	Parasitic to Ground Tolerance Including package parasitics (Pins C0, CC, and C1) [b]	Mult 1			10	pF
		Mult 2			20	pF
		Mult 4			40	pF
		Mult 8			80	pF
N_{OUT}	Peak-to-Peak Noise @ output (100 measurements in 14 bit) [b]	Mult 1, 2, 4, 8		5	20	LSB

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
AE_{out}	Error Mult 1, -40 to 125°C [b], [i], [j], [k]	3V±10%, 3.3V±10%, 5V±10%		±0.25	±0.75	%FSO
		2.5V±10%		±0.50	±1.25	%FSO
AE_{out}	Mult 2, 4, 8, -40 to 125°C [b], [i], [j], [k]	3V±10%, 3.3V±10%, 5V±10%		±0.50	±1.25	%FSO
		2.5V±10%		±1.50	±3.00	%FSO

[a] See section 6 for full details for current consumption in each mode.
[b] Parameter not tested during production but guaranteed by design.
[c] Parameter measured using internal test capacitors (0pF to 7pF in Mult 1).
[d] Assumes optimal calibration points of 0°C and 100°C; see section 8 for more details.
[e] Assumes optimal calibration points of -20°C, 40°C and 100°C; see section 8 for more details.
[f] See section 10.7 for more details.
[g] See section 10 for more details.
[h] Timing values are for a nominal oscillator, for worst case, ±10% total frequency variation, multiply by 0.9 (minimum time) or 1.1 (maximum time).
[i] Accuracy specification includes a 2-point temperature calibration for correcting the internal TC.
[j] Accuracy specification assumes maximum parasitics of 10pF to ground.
[k] Accuracy specification does not include PDM errors; see the PDM Output electrical parameters for additional errors when using PDM.

6. Current Consumption Graphs

Part current consumption depends on a number of different factors including voltage, temperature, capacitive input, Mult, resolution, and power down time. The best method for calculating the ZSSC3123's power consumption is to measure the current consumption with the actual setup. If measurement is not possible, then the graphs in this section can provide a starting point for estimating the current consumption.

6.1 Update Mode Current Consumption

Figure 2. Best Case Settings (Typical Part)

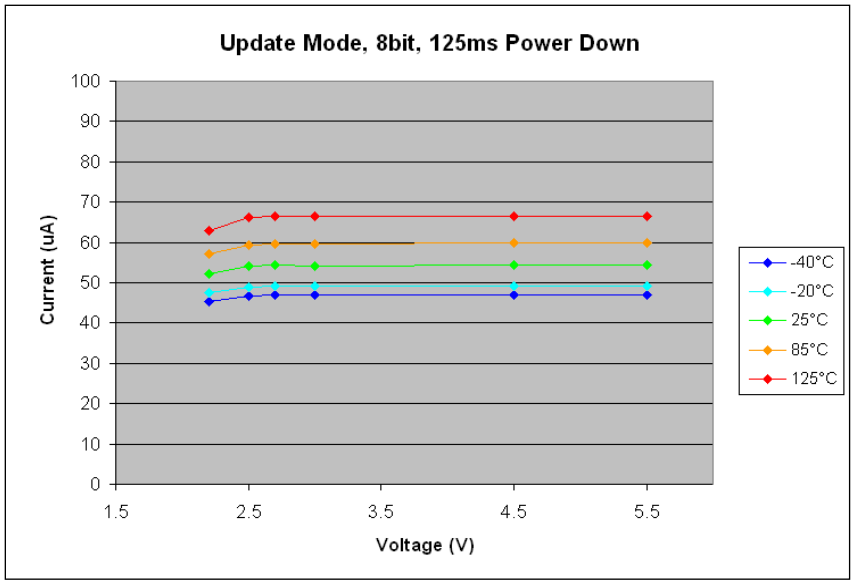
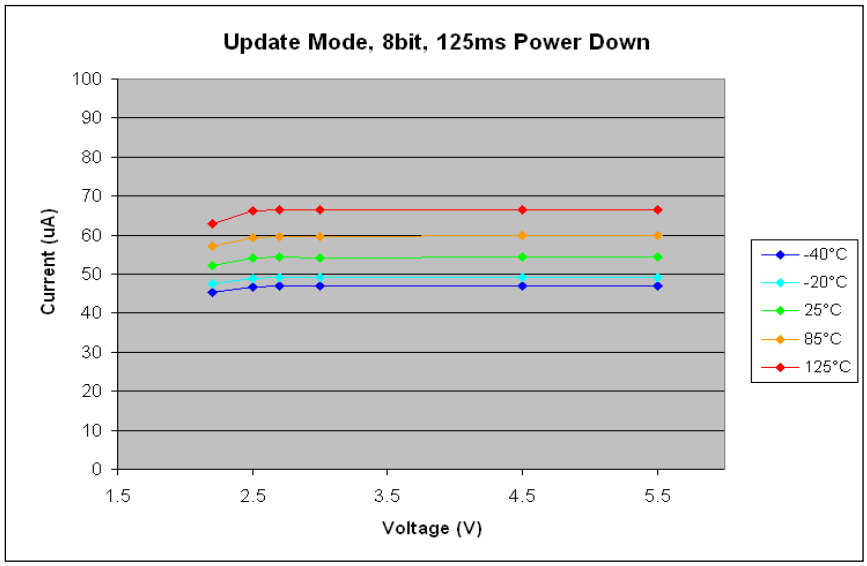
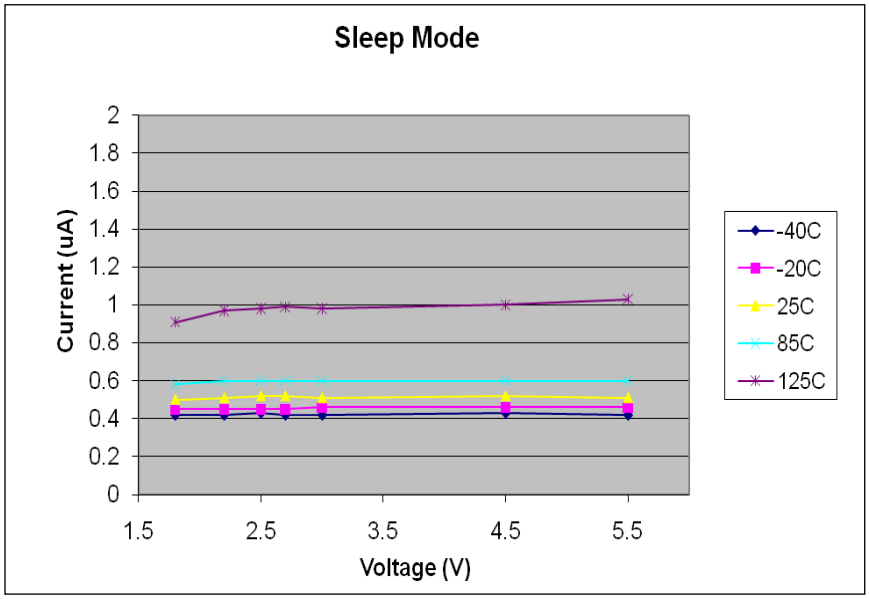


Figure 3. Worst Case Settings (Typical Part)



6.2 Sleep Mode Current Consumption

Figure 4. Typical Current Consumption during Sleep Mode (No Measurements)



7. Output Pad Drive Strength

Figure 5. Output High Drive Strength Graph

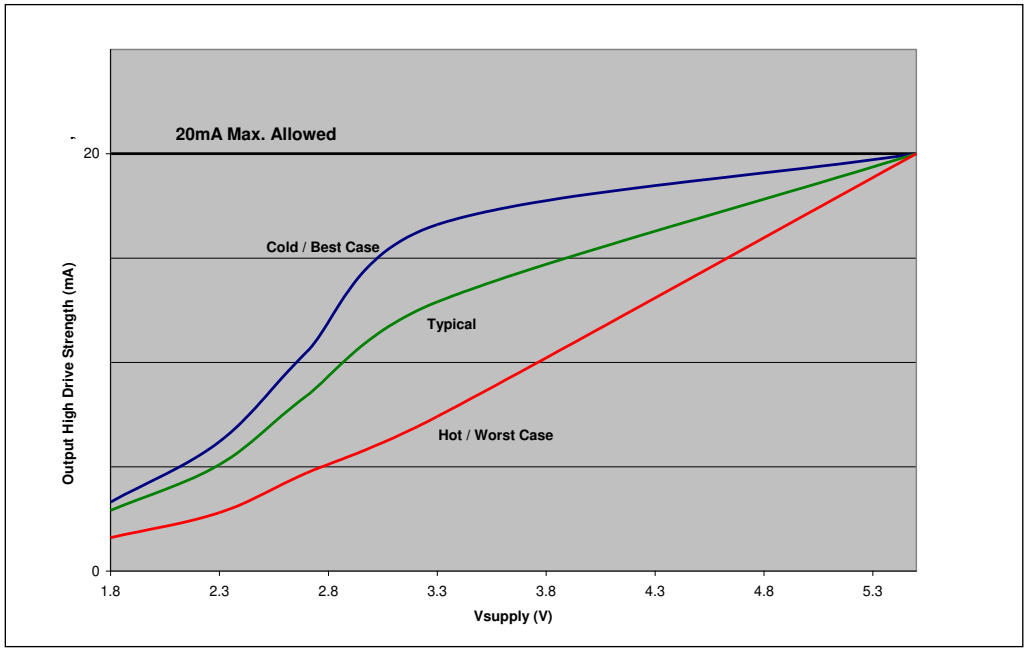
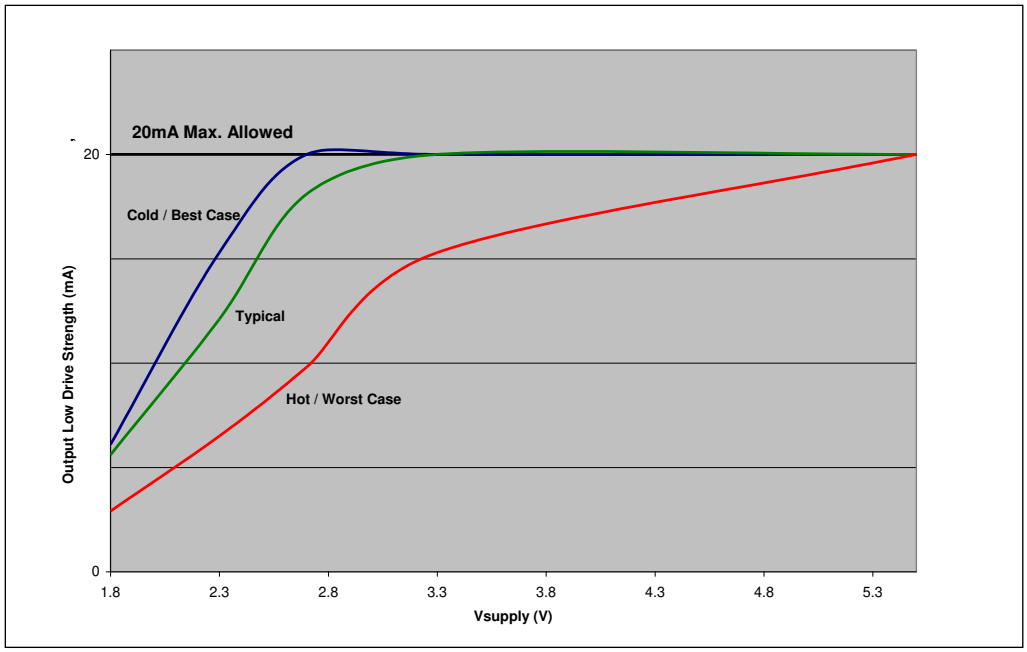


Figure 6. Output Low Drive Strength Graph



8. Temperature Sensor Nonlinearity

Temperature sensor nonlinearity can vary depending on the type of calibration and the selected calibration points. It is highly recommended that a temperature calibration is done with calibration points at least 20°C apart from each other. The following figures show the resulting nonlinearity error for the full temperature range (-40°C to 125°C) using the optimal calibration points 0°C and 100°C for a first-order fit and -20°C, 40°C, and 100°C for a second-order fit.

Figure 7. First Order Fit (Typical Part)

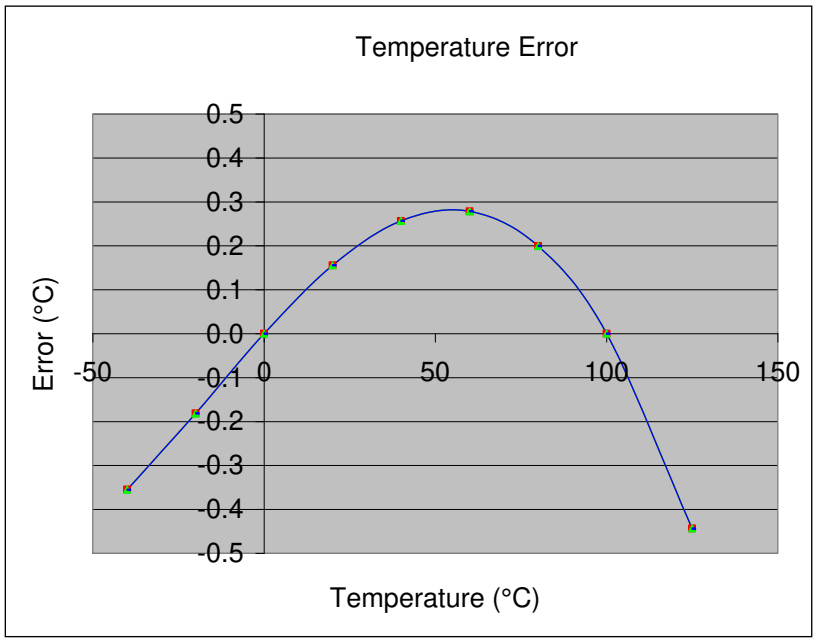
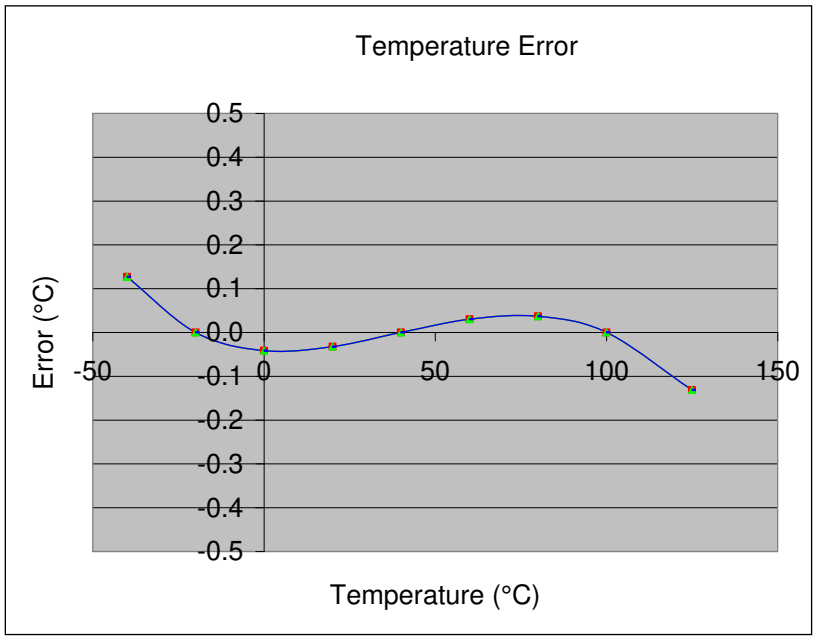


Figure 8. Second Order Fit (Typical Part)



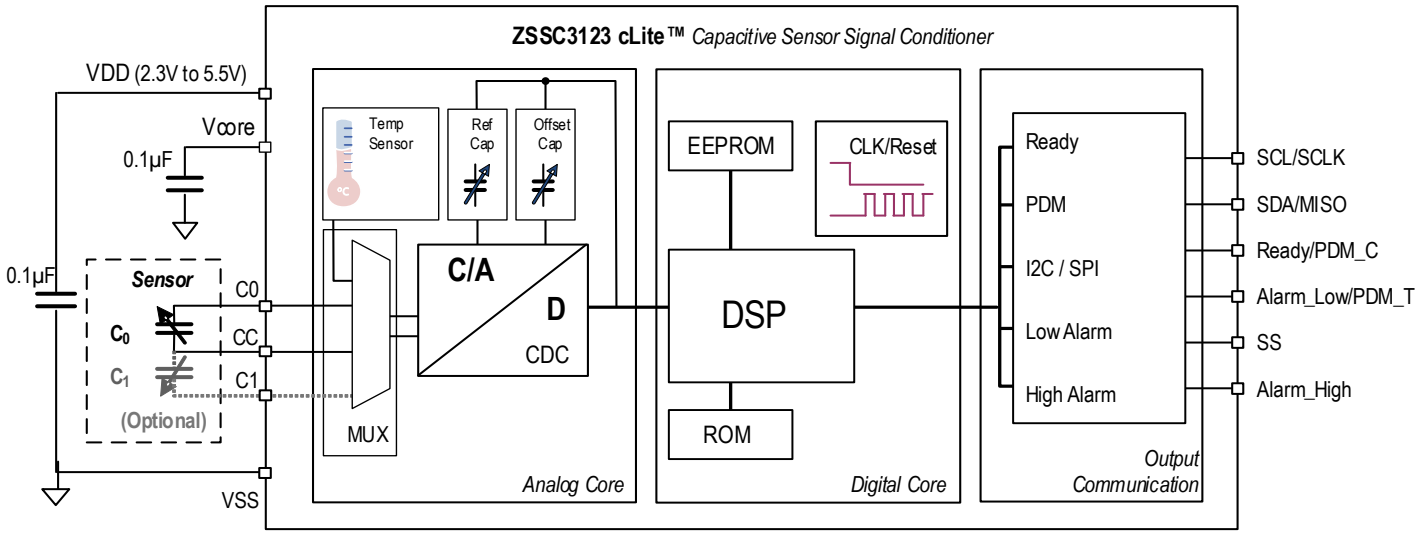
9. Circuit Description

9.1 Signal Flow and Block Diagram

As seen in the following figure, the ZSSC3123 comprises three main blocks: the analog core, digital core, and output communication. The capacitive input is first sampled by the analog core using a charge-balancing CDC and is adjusted for the appropriate capacitance range using the CDC_Offset, CDC_Reference, and CDC_Mult settings. The digital core corrects the digital sample with an on-chip digital signal processor (DSP), which uses coefficients stored in EEPROM for precise conditioning. An internal temperature sensor can be used to compensate for temperature effects of the capacitive input. A temperature value can also be calibrated and output as a 14-bit reading.

The corrected capacitance value can be read using four different output types, I2C, SPI, PDM, and alarms. They can all be directly interfaced with a microcontroller, and optional filtering of the PDM output can provide a ratiometric analog output. The alarm pins can also be used to control a variety of analog circuitry.

Figure 9. ZSSC3123 Block Diagram



9.2 Analog Front End

9.2.1 Capacitance-to-Digital Converter

A 1st-order charge-balancing capacitance-to-digital converter (CDC) is used to convert the input capacitance to the digital domain. The CDC uses a chopper-stabilized design to decrease any drift over temperature. The CDC interfaces to the sensor capacitor through the input multiplexer that controls whether the measurement is a capacitance or a temperature measurement. The input multiplexer also allows for two sensor capacitance configurations: a single-sensor capacitance or a two-sensor, ratio-based differential capacitance configuration, where the reference capacitor is part of the sensor.

As part of a switched-capacitor network, the reference capacitor C1 is driven by a square-wave voltage of the frequency f_{EXC} (see section 5). The sensor capacitance C0 is not exposed to DC voltages in order to prevent the aging effects of some sensor types. The configuration of the CDC is controlled by programming settings in EEPROM word *C_Config*. (See Table 30 for settings.)

9.2.1.1 Single Ended

In the case of a single-sensor capacitor, the CDC output is proportional to the ratio of the sensor capacitor to an internal reference capacitor (C_{REF}). This internal reference capacitor value can be adjusted using the 3-bit trim CDC_Reference and a 2-bit range selection CDC_Mult (bit settings in Table 30). To optimize the measured end-resolution further, another internal capacitor (C_{OFF}) allows the subtraction of a defined offset capacitance using the 3-bit trim CDC_Offset (bit setting in Table 30). Equation 1 and Equation 2 describe the CDC output for a single sensor capacitance measurement. For C_{MULT}, use the multiplier in the "Total Capacitance Multiplier (C_{MULT})" column in Table 5. Select the values of CDC_Offset, and CDC_Reference by using the settings given in Table 6 to Table 9, depending on the Mult value. Note: Use the bit settings (0-7) and not the value in pF.

$$Z_{SENSOR} = \frac{(C_0 - C_{OFF})}{C_{REF}}$$ **Equation 1**

$$Z_{CDC} = 2^{RES} * Z_{SENSOR}$$ **Equation 2**

With

$$C_{OFF} = C_{MULT} * CDC\_Offset * 1pF$$ **Equation 3**

And

$$C_{REF} = C_{MULT} * CDC\_Reference * 1pF$$ **Equation 4**

Where:

Symbol	Description
Z_{SENSOR}	Measured sensor ratio, must be in the range [0 to 1]
C_0	Input sensor capacitance
C_{OFF}	Zero shift of CDC
C_{REF}	Reference capacitance
Z_{CDC}	Digital raw converted capacitance value
RES	Programmable CDC resolution of 8, 10, 12, or 14 bits (bit setting in Table 30.
C_{MULT}	Capacitance range multiplier (see Table 5)
CDC_Offset	CDC offset trim setting (see section 9.2.1.4 and bit setting see Table 30
CDC_Reference	CDC reference setting (see section 9.2.1.4 and bit setting see Table 30)

9.2.1.2 Single Ended with External Reference

Some sensors include an external reference capacitor as part of the sensor construction. If the external reference capacitance (C_1) is constant or increases with increasing input sensor capacitance (C_0), then use CDC output Equation 5 through Equation 7. In this case, the CDC_Reference should be set to zero (bit setting in Table 30).

$$Z_{SENSOR} = \frac{(C_0 - C_{OFF})}{C_1}$$ **Equation 5**

$$Z_{CDC} = 2^{RES} * Z_{SENSOR}$$ **Equation 6**

$$C_{OFF} = C_{MULT} * CDC\_Offset * 1pF$$ **Equation 7**

Where:

Symbol	Description
Z_{SENSOR}	Measured sensor ratio; must be in the range [0 to 1]
C_0	Input sensor capacitance
C_{OFF}	Zero shift of CDC
C_1	External reference capacitance
Z_{CDC}	Digital raw converted capacitance value
RES	Programmable CDC resolution of 8, 10, 12, or 14 bits (bit setting in Table 30)
C_{MULT}	Capacitance range multiplier (see Table 5)
CDC_Offset	CDC offset trim setting (see section 9.2.1.4 and Table 30)

9.2.1.3 Differential

A differential capacitive sensor includes two capacitors C_0 and C_1 that are captured as a ratio. The differential sensor is built so that the sensor input capacitance C_0 increases while the external reference capacitance C_1 decreases over the input signal range, but the total sum always remains constant. Equation 8 and Equation 9 describe the CDC output for a differential sensor capacitance measurement. The CDC_Reference and CDC_Offset capacitor trim bits must be set to zero, and the Differential bit must be set to one. (See Table 30 for bit numbers and settings). The Mult bits should be set so that the total capacitance (C_0 + C_1) falls in the corresponding capacitance range (see Table 5). The sum of C_0 and C_1 must not be larger than the selected Mult's maximum input range, except when CC is used as a decoupling capacitor.

In differential mode special sensor types can allow a non-galvanic connection with an external isolating capacitor C_{CC} between the sensor and the CC pin to avoid wear caused by mechanical moving parts.

$$Z_{SENSOR} = \frac{C_0}{(C_0 + C_1)}$$ **Equation 8**

$$Z_{CDC} = 2^{RES} * Z_{SENSOR}$$ **Equation 9**

Where:

Symbol	Description
Z_{SENSOR}	Measured sensor ratio; must be in the range [0 to 1]
C_0	Input sensor capacitance (moves in the opposite direction of C_1)
C_1	External reference capacitance (moves in the opposite direction of C_0)
Z_{CDC}	Digital raw converted capacitance value
RES	Programmable CDC resolution of 8, 10, 12, or 14 bits (bit setting in Table 30)

9.2.1.4 Capacitive Range Selection

Whether the application uses a single-ended or a differential sensor, the correct capacitance range as defined in Table 5 must be selected using the Mult bits, which are configured in the *C_Config* register (see Table 30). If using a single-ended sensor, then the minimum and maximum capacitance inputs should fall into the specified ranges. If using a differential sensor then the total capacitance (C_0 + C_1) must fall into this range. The Mult range affects the conversion time (see section 10.2).

Note: If the externally applied capacitance exceeds the configured capacitance range, the converted output signal can still show an apparently correct value, which is not valid. The limit is about 500% of the selected maximum input value. For example, for a capacitance setting of Mult1, CDC_Offset at zero, and CDC_Reference at 7, an input value above 117pF will give a non-saturated input value.

Table 5. CDC Multiplier

EEPROM Encoding (CDC_Mult)	Frequency Multiplier (Mult)	Reference Multiplier	Total Capacitance Multiplier (C_{MULT})	Capacitance Range (Full Scale Values)
00_{BIN}	1	1.44	1.44	2pF to 8pF
01_{BIN}	2	2.88	5.76	8pF to 32pF
10_{BIN}	4	5.76	23.04	32pF to 130pF
11_{BIN}	8	11.52	92.16	130pF to 260pF

For single-ended sensors, use Table 6, Table 7, Table 8, and Table 9 as guidance for selecting appropriate values for the CDC (C_{OFF}) and (C_{REF}) for a particular capacitance input range. The CDC_Offset and CDC_Reference bits are found in EEPROM word C_Config. (Refer to Table 30 for bit numbers). Using the tables, the CDC input range can be adjusted to optimize the coverage of the sensor signal and offset values to give the maximum sensor span that can be processed without losing resolution. Choose a range by fitting the input sensor span within the narrowest range in the table, but note that these tables are only approximate, so the range should be chosen experimentally with the actual setup. Also note that since internal capacitance values can vary over process (see specification C_{tol} in Table 4), the minimum and maximum sensor span should be at least ±10% within the minimum and maximum of the chosen range respectively. Note: Take into consideration the effects of parasitics; if the parasitics for a particular Mult range exceed the parasitic to ground tolerance given in section 1, then the next Mult range should be considered since the CDC frequency is reduced by the Mult factor.

Note: A C_{REF} setting of 0 (marked with * in the following tables) is only supported with an external reference capacitor (C1) for single-ended sensors. C1 capacitance values should be within the defined range for each Mult setting.

Selection settings for C_{REF}, and C_{OFF}, and Mult are given in the following tables (capacitance ranges are nominal values).

Table 6. Mult 1: Sensor Capacitors Ranging from 2pF to 10pF (Full Scale Values)

		CDC_Reference															
3-bit set		0*		1		2		3		4		5		6		7	
CDC_Offset	0	0.0	C1	0.0	1.4	0.0	2.9	0.0	4.3	0.0	5.8	0.0	7.2	0.0	8.6	0.0	10.1
	1	1.4	C1	1.4	2.9	1.4	4.3	1.4	5.8	1.4	7.2	1.4	8.6	1.4	10.1	1.4	11.5
	2	2.9	C1	2.9	4.3	2.9	5.8	2.9	7.2	2.9	8.6	2.9	10.1	2.9	11.5		
	3	4.3	C1	4.3	5.8	4.3	7.2	4.3	8.6	4.3	10.1	4.3	11.5				
	4	5.8	C1	5.8	7.2	5.8	8.6	5.8	10.1	5.8	11.5						
	5	7.2	C1	7.2	8.6	7.2	10.1	7.2	11.5								
	6	8.6	C1	8.6	10.1	8.6	11.5										
	7	10.1	C1	10.1	11.5												

PROHIBITED

not recommended

Table 7. Mult 2: Sensor Capacitors Ranging from 8pF to 32pF (Full Scale Values)

		CDC_Reference															
3-bit set		0*		1		2		3		4		5		6		7	
CDC_Offset	0	0.0	C1	0.0	5.8	0.0	11.5	0.0	17.3	0.0	23.0	0.0	28.8	0.0	34.6	0.0	40.3
	1	5.8	C1	5.8	11.5	5.8	17.3	5.8	23.0	5.8	28.8	5.8	34.6	5.8	40.3		
	2	11.5	C1	11.5	17.3	11.5	23.0	11.5	28.8	11.5	34.6	11.5	40.3				
	3	17.3	C1	17.3	23.0	17.3	28.8	17.3	34.6	17.3	40.3						
	4	23.0	C1	23.0	28.8	23.0	34.6	23.0	40.3								
	5	28.8	C1	28.8	34.6	28.8	40.3										
	6	34.6	C1	34.6	40.3												
	7																

PROHIBITED

not recommended

Table 8. Mult 4: Sensor Capacitors Ranging from 32pF to 130pF (Full Scale Values)

		CDC_Reference															
3-bit set		0*		1		2		3		4		5		6		7	
CDC_Offset	0	0.0	C1	0.0	23.0	0.0	46.1	0.0	69.1	0.0	92.2	0.0	115.2	0.0	138.2	0.0	161.3
	1	23.0	C1	23.0	46.1	23.0	69.1	23.0	92.2	23.0	115.2	23.0	138.2	23.0	161.3		
	2	46.1	C1	46.1	69.1	46.1	92.2	46.1	115.2	46.1	138.2	46.1	161.3				
	3	69.1	C1	69.1	92.2	69.1	115.2	69.1	138.2	69.1	161.3						
	4	92.2	C1	92.2	115.2	92.2	138.2	92.2	161.3								
	5	115.2	C1	115.2	138.2	115.2	161.3										
	6	138.2	C1	138.2	161.3												
	7																

PROHIBITED

not recommended

Table 9. Mult 8: Sensor Capacitors Ranging from 130pF to 260pF (Full Scale Values)

		CDC_Reference															
3-bit set		0*		1		2		3		4		5		6		7	
CDC_Offset	0	0.0	C1	0.0	92.2	0.0	184.3	0.0	276.5								
	1	92.2	C1	92.2	184.3	92.2	276.5										
	2	184.3	C1	184.3	276.5												
	3																
	4																
	5																
	6																
	7																

PROHIBITED

not recommended

9.2.2 Temperature Measurement

The temperature signal comes from an internal PTAT (proportional to absolute temperature) circuit that is a measure of the die temperature. The PTAT (VPTAT) voltage is used in the CDC to charge an internal capacitor (CT), while the bandgap voltage (VBG) is used to charge the offset and the reference trimmable capacitors. The CDC temperature output (ZTEMP) is defined by Equation 10 through Equation 13:

$$Z_{TEMP} = 2^{RES} * \frac{(V_{PTAT} / V_{BG}) * C_T - C_{TOFF}}{C_{TREF}}$$ **Equation 10**

With

$$C_T = 1.44 * Temp\_Trim * 1pF$$ **Equation 11**

With

$$C_{TOFF} = 1.44 * CDC\_Offset * 1pF$$ **Equation 12**

And

$$C_{TREF} = 1.44 * CDC\_Reference * 1pF$$ **Equation 13**

Where:

Symbol	Description
Z_{TEMP}	Measured internal temperature
RES	Programmable CDC resolution of 8, 10, 12, or 14 bits (bit setting in Table 31)
V_{PTAT}	Internal PTAT voltage
V_{BG}	Internal bandgap voltage
C_T	Temperature measurement capacitor
C_{TOFF}	Temperature CDC zero shift
C_{TREF}	Temperature reference capacitance
Temp_Trim	Temperature trim setting (bit setting in Table 31)
CDC_Offset	CDC offset trim setting (bit setting in Table 31)
CDC_Reference	CDC reference setting (bit setting in Table 31)

Note: The factory settings for Temp_Trim, CDC_Offset, and CDC_Reference are optimized for the full temperature range of -40°C to 125°C guaranteeing a minimum effective resolution of 13 bits when 14 bits of resolution is selected. Unless a different temperature range is needed, it is strongly recommended that these settings not be changed.

9.3 Digital Core

The digital core provides control logic for the analog front-end, performs input signal conditioning, and handles external communication. A digital signal processor (DSP) is used for conditioning and correcting the converted sensor and temperature inputs. The DSP can correct for up to a two-region piece-wise non-linear sensor input, and up to a second-order non-linear temperature input. Alternatively a third-order correction of the sensor input for one region and up to a second-order, non-linear temperature input can be selected. Refer to section 13 for details on the signal conditioning and correction math. The analog front-end configuration and correction coefficients for both the capacitive sensor and the temperature sensor are stored in an on-chip EEPROM.

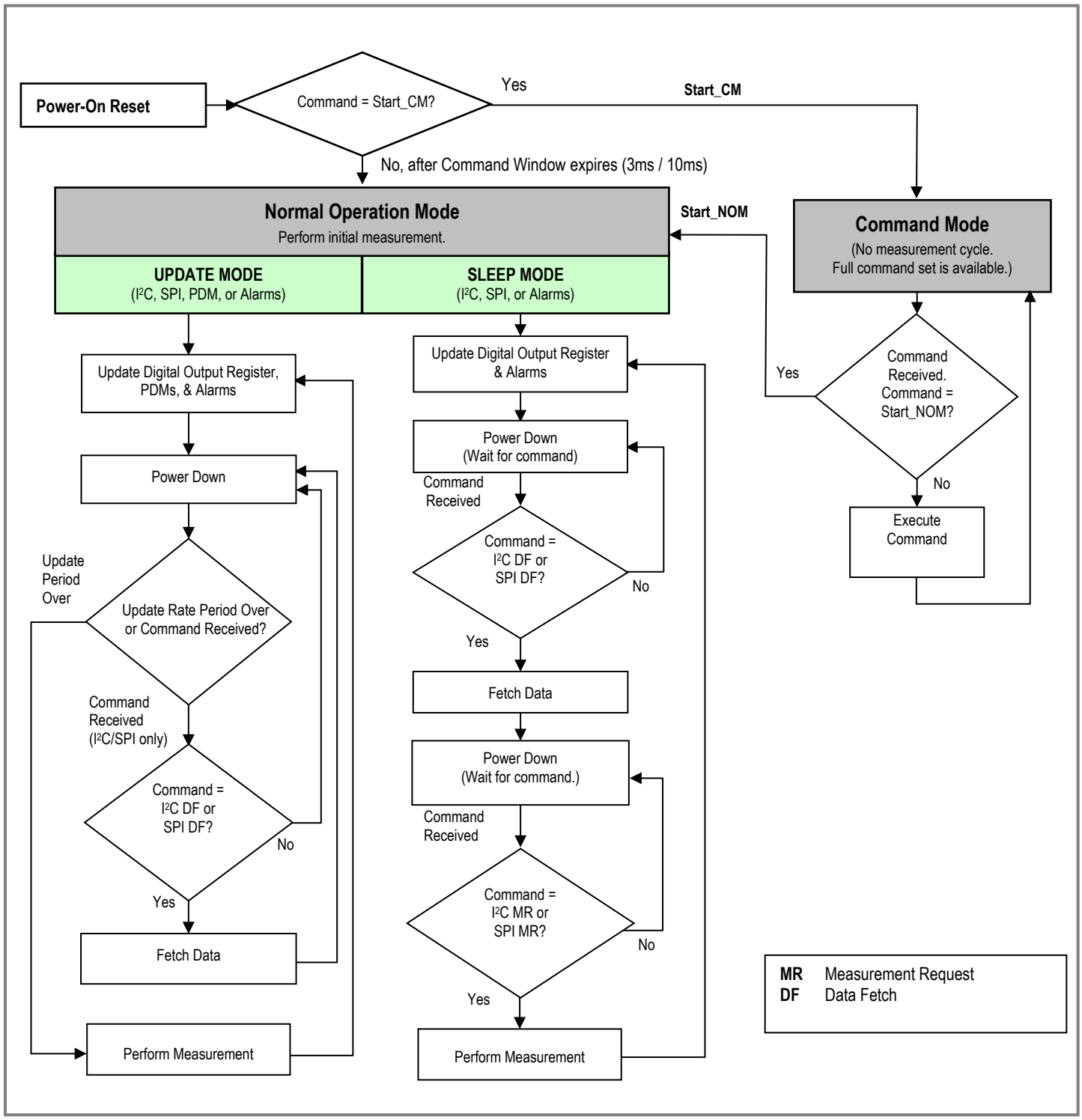
Four different types of outputs are available: I2C, SPI, PDM, and the Alarms. These output modes are used in combination with the two measurement modes: Update Mode and Sleep Mode. For a full description of normal operation in each mode, refer to section 10.

The ZSSC3123 has an internal 1.85MHz temperature-compensated oscillator that provides the time base for all operations. When VDD exceeds the POR level, the reset signal de-asserts and the clock generator starts. See section 10.1 for the subsequent power-on sequence. The exact clock frequency influences the measurement cycle time (see the frequency variation spec in section 5). To minimize the oscillator error as the VDD voltage changes, an on-chip regulator supplies the oscillator block.

10. Normal Operation Mode

The following figure gives a general overview of ZSSC3123 operation. Details of operation, including the power-up sequence, measurement modes, output modes, diagnostics, and commands, are given in the subsequent sections.

Figure 10. General Operation

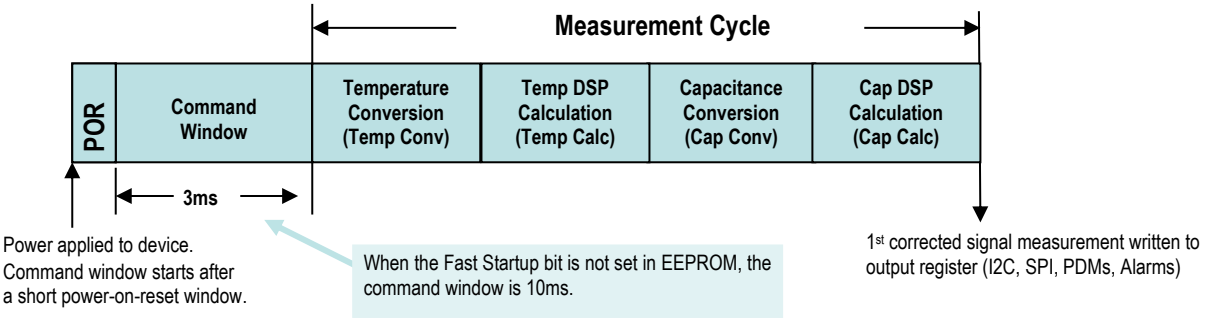


10.1 Power-On Sequence

The following figure shows the power-on sequence of the ZSSC3123. On system power-on reset (POR), the ZSSC3123 wakes as an I2C device regardless of the output protocol programmed in EEPROM. After power-on reset, the ZSSC3123 enters the command window. It then waits for a Start_CM command for 3ms if the Fast_Startup EEPROM bit is set or if the bit is not set, it waits10ms (see Table 32). If the ZSSC3123 receives the Start_CM command during the command window, it enters and remains in Command Mode. Command Mode is primarily used in the calibration environment. See section 11 for details.

If during the power-on sequence, the command window expires without receiving a Start_CM or if the part receives a Start_NOM command in Command Mode, the device will immediately assume its programmed output mode and will perform one complete measurement cycle. Timing for the initial measurement is described in section 10.2. At the end of the capacitance DSP calculation, the first data is written to the output register. Beyond this point, conversions are performed according to the programmed measurement mode settings (see section 11.3).

Figure 11. Power-On Sequence with Fast Startup Bit Set in EEPROM



Note: See section 10.2 for timing of the measurement cycle. Timing values shown are typical; for the worst case values, multiply by 1.1 (nominal frequency ±10%).