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## 4 Channel Buffer Device with high capacitance load capability

#### DEVICE DESCRIPTION

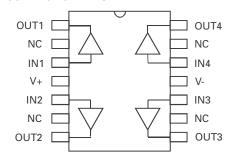
The ZXFBF05 is a low cost, high slew rate, quad buffer amplifier. Built using the Zetex CA700 technology, this buffer has a small signal bandwidth of greater than 100MHz and a 1 volt pk-pk bandwidth of greater than 20 MHz. Each channel draws only 7.5mA. The device operates from a ±5 volt supply, which makes it ideal in a majority of applications.

This space saving buffer may be used in a wide variety of applications such as, video switching matrix, multi-channel instrumentation equipment, and A/D input buffer, etc.

#### **FEATURES AND BENEFITS**

- · 4 Buffers per package
- Low distortion Class A O/P
- 100MHz bandwidth
- Low cost
- · Designed for up to 300pF load
- Low supply current (7.5mA per buffer)
- No thermal runaway
- 14 pin SOIC package

# CONNECTION DIAGRAM



14 PIN SOIC PACKAGE

#### **APPLICATIONS**

- · Video Switching Matrix input buffer
- Instrumentation
- Multi-channel A/D input buffer
- Multi-isolation buffer

1 .	PART NUMBER	PACKAGE	PART MARK
Z	XFBF05N14	SOIC14N	ZXFBF05

#### ORDERING INFORMATION

PART NUMBER	CONTAINER	INCREMENT
ZXFBF05N14TA	Reel 7"	500
ZXFBF05N14TC	Reel 13"	2500

#### RELATED PRODUCTS

ZXFBF04 4 Channel Buffer

ZXFBF08 8 Channel Buffer

ZXFBF25 4 Channel Buffer with output enable



### **ABSOLUTE MAXIMUM RATINGS**

Voltage on any pin 20V (relative to V-)

Operating temperature range 0 to 70°C (de-rated for -40 to 85°C)

Storage Temperature -55 to 125°C

## **ELECTRICAL CHARACTERISTICS**

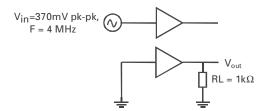
Test Conditions: Temperature =25°C, V+ = 5.00, V- = -5.00V,  $R_L$  = 1k $\Omega$ ,  $C_L$  = 10pF

Parameter	eter Conditions M		Typical	Max.	Units
Offset Voltage	V <sub>in</sub> = 0V	-25	-	25	mV
Offset Voltage Drift	V <sub>in</sub> = 0V		20		V/°C
Supply Current	All inputs = 0V	5.0	30	40	mA
Input Bias Current	put Bias Current V <sub>in</sub> = 0V		1.0	2.0	μΑ
Output Voltage	$R_L = 200\Omega$		±1		V
DC Gain	C Gain $ \begin{aligned} V_{in} &= \pm \ 0.5 \text{V}, \ \text{R}_{L} = 1 \text{k} \Omega \\ V_{offset} &= 0.0 \text{V} \end{aligned} $		0.98	1.00	V/V
DC Gain $\begin{aligned} V_{in} &= \pm 0.5 \text{V, R}_{L} = 1 \text{k}\Omega \\ V_{offset} &= 0.25 \text{V} \end{aligned}$		0.95	0.98	1.00	V/V
Sink Current	V <sub>in</sub> = 0V, V <sub>out</sub> =0.5V	4.0	6.0	12.0	mA
Source Current	V <sub>in</sub> = 0V, V <sub>out</sub> =-0.5V	8.0	15.0	18.0	mA
Input Resistance		10	20	100	MΩ
Output Resistance		5	10	15	Ω
Bandwidth	20mVp-p, 1.0Vp-p		100 20		MHz
Slew Rate			40		V/μs
Voltage Noise	10 – 100 kHz		15		nV/√Hz
Differential Gain NTSC	F = 3.58MHz, V <sub>in</sub> = 0.286Vp-p,		0.1		%
Differential Phase NTSC	DC $\Delta V_{in} = 0$ to 0.714V		0.15		Degrees
Differential Gain PAL	F = 4.43MHz, V <sub>in</sub> = 0.286Vp-p,		0.1		%
Differential Phase PAL	DC $\Delta V_{in} = 0$ to 0.714V		0.15		Degrees
Channel Isolation $V_{in} = 370 \text{mVp-p}, \text{ RL} = 1 \text{k}\Omega$ $F = 4 \text{ MHz}$			-60		dB

### **NOTES**

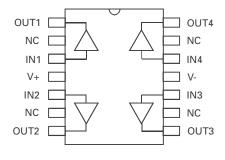
Test circuit for measuring channel isolation.

Channel Isolation =  $20 \times LOG_{10} (V_{out} / V_{in}) dB$ 





## **PIN DESCRIPTION**

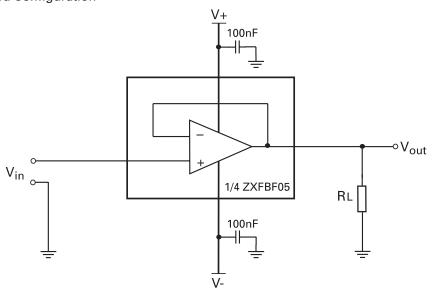


14 PIN SOIC PACKAGE

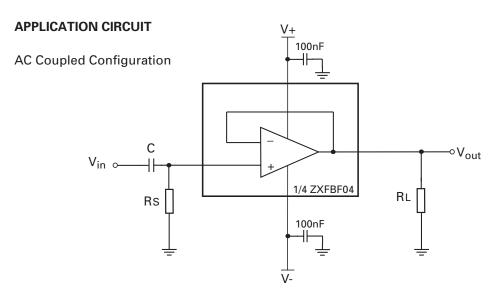
OUT 1,2,3,4 IN 1,2,3,4 V+ V- Buffer outputs.
Buffer Inputs.
Positive supply pin, +5 volts.
Negative supply pin, -5 volts.

## **APPLICATION CIRCUIT**

## DC Coupled Configuration



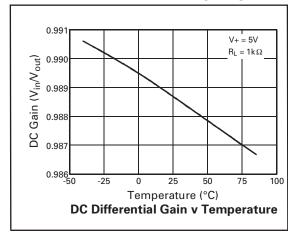


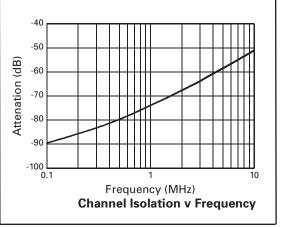


### NOTE.

Rs: Source Resistor, provides DC bias for buffer input. Rs  $\leq 10 k\Omega$ Both 100nF decoupling capacitors should be situated close to device supply pins.

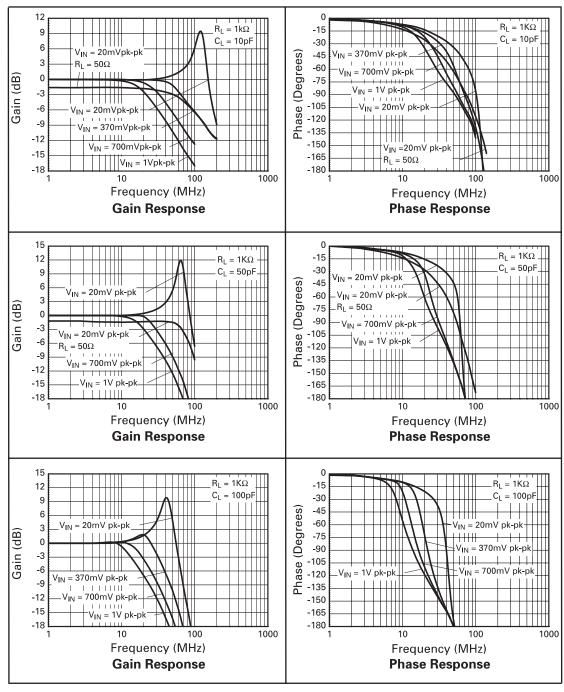
## **TYPICAL CHARACTERISTICS**







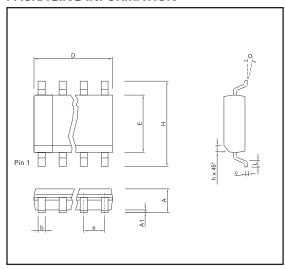
### TYPICAL CHARACTERISTICS



Test Conditions:V+=5V, Temperature=25°C.



### **PACKAGING INFORMATION**



#### SOIC 14 Lead

DIM	Inches		Millimetres		
	Min	Max	Min	Max	
А	0.053	0.069	1.35	1.75	
A1	0.004	0.010	0.10	0.25	
D	0.337	0.344	8.55	8.75	
Н	0.228	0.244	5.80	6.20	
Е	0.150	0.157	3.80	4.00	
L	0.016	0.050	0.4	1.27	
е	0.050 BSC		1.27 BSC		
b	0.013	0.020	0.33	0.51	
С	0.008	0.010	0.19	0.25	
0	0°	8°	0°	8°	



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