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ZXFV4089
Video amplifier with DC restoration

Description

The ZXFV4089 is a DC restored video amplifier (black-level clamp) in an 8 pin SOIC package. It integrates a high performance video amplifier with a nulling sample and hold amplifier specially designed to provide brightness level stability.

The input video signal is AC coupled to the main amplifier and this AC coupling capacitor also acts as the holding capacitor for the sample and hold amplifier. This configuration reduces both pin count and external components over traditional solutions.

Typically, during the back-porch interval of an analog video waveform the sample and hold amplifier forces the input of the video amplifier to the reference voltage.

The video waveform is now referenced to the new reference voltage for the remainder of the line-scan interval.

The video amplifier has been optimised for video applications and as such drives back-terminated 75Ω loads with good differential gain and phase errors. The current feedback architecture allows the bandwidth to remain fixed over a wide range of gains, and is set by two external resistors.

The ZXFV4089 is specified for operation at ±5V and over the -40°C to +85°C temperature range and is pin compatible with the industry standard EL4089.

Features

- Complete analog video DC level restoration system
  - Supports various TV systems
- PAL, NTSC, SECAM
- Excellent video performance
  - 0.08% differential gain
  - 0.1° differential phase
  - 30 MHz 0.1 dB bandwidth
- 210 MHz -3 dB bandwidth
- 400V/ms slewrate
- TTL/CMOS logic compatible HOLD input
- Pin and function compatible with industry standard EL4089

Applications

- Black level clamp, providing stable intensity in video systems such as:
  - cameras
  - image capture
  - video mixing
  - displays
- DC restoration of other high frequency signals

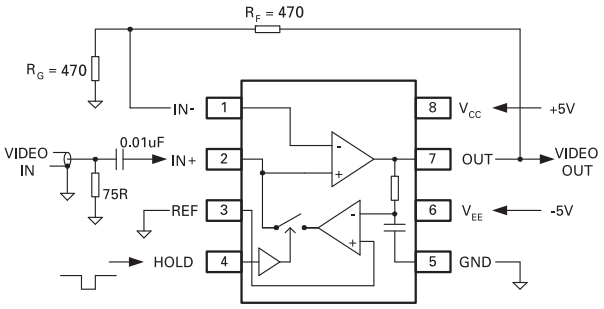


Figure 1 Pin connection diagram

Ordering information

Part number	Reel size (inches)	Quantity per reel	Device marking
ZXFV4089N8TA	7	500	4089
ZXFV4089N8TC	13	2500	4089

Absolute maximum ratings - Over operating free-air temperature (unless otherwise stated)[b]

Positive supply voltage V_{CC} to GND	-0.5V to +5.5V
Negative supply voltage V_{EE} to GND	-5.5V to +0.5V
Input voltage, pins 1,2,3 to GND	V_{EE} -0.5V to V_{CC} +0.5V
Differential input voltage 2, pin 1 to pin 2	±3 V
Output current, pin 7 (continuous, TJ < 110°C)	±60 mA
Internal power dissipation	See note[d]
Input current, IN- pin 1	±5 mA
Current into IN+ and HOLD, pins 2 and 4	±5 mA
Operating ambient temperature range	-40°C to 85°C
Storage temperature range	-65°C to 150°C
Operating junction temperature T_{JMAX}	150°C

NOTES:

(b) Stresses above those listed under absolute maximum ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(c) At high closed loop gains and low gain setting resistors care must be taken if large input signals are applied to the device which cause the output stage to saturate for extended periods of time.

(d) The power dissipation of the device when loaded must be designed to keep the device junction temperature below T_{JMAX}, de-rated according to the Theta-ja for the SO8 package, which is typically 168°C/W, i.e. 0.74W at 25°C.

ESD: This device is sensitive to static discharge and proper handling precautions are required.

Recommended operating conditions

Parameter		Min.	Max.	Unit
$V_{S\pm}$	Dual supply voltage range	±4.75	±5.25	V
V_{CMR}	Common mode input voltage range	-3	+3	V
T_A	Ambient temperature range	-40	85	°C
V_{REFCMR}	Common mode input range of V_{REF}	-2	+2	V
R_{DRIVE}	Effective resistance driving pin 2	30	150	Ω

Recommended resistor values

$V_{S\pm}$ = 5V, C_L = 10pF

G_{CL}	R_F	R_G	Peaking
1	680	n/c	2 dB
	820		0
	1000		-2dB
2	430	430	2dB
	470	470	1.5dB
	560	560	0

Electrical characteristics

V_{CC} = 5V, V_{EE} = -5V, G =1, R_F = 1kV, R_{LOAD} = 1kV, T_{amb} = 25°C unless otherwise stated.

Parameter		Conditions	Min.	Typ.	Max.	Unit
I_{CCH}	Positive supply current, holding	HOLD = HIGH	5	8	10	mA
I_{CCS}	Positive supply current, sampling	HOLD = LOW	5	8.5	11	mA
I_{EEH}	Negative supply current, holding	HOLD = HIGH	5	8	10	mA
I_{EES}	Negative supply current, sampling	HOLD = LOW	5	8.5	11	mA
Amplifier section, hold Input = high unless otherwise stated						
V_{OS}	Input offset voltage	V_{IN+} = 0V		1	10	mV
I_{B+}	+ input bias current			1	5	µA
I_{B-}	– input bias current			1	10	µA
R_{OL}	Trans-impedance	V_{IN+} = ±3V		1800		kΩ
R_{IN+}	+ input resistance		1	2		MΩ
V_O	Output voltage swing	V_{IN+} = ±3V, I_{OUT} = 740mA	±2.95	±3.0		V
I_O	Output drive current		40			mA
+PSRR	Positive power supply rejection ratio	V_{CC} = 5V±5%, V_{EE} = -5V	49	57		dB
-PSRR	Negative power supply rejection ratio	V_{CC} = 5V, V_{EE} = -5V ±5%	51	58		dB
C_{MRR}	Common mode rejection ratio	V_{IN} = ±3V	48	57		dB
Restore section, HOLD = low unless otherwise stated						
V_{OSCOMP}	Composite input offset voltage, from V_{REF} to amplifier output	V_{REF} = 0V		0.3	7	mV
I_{REF}	V_{REF} input bias current	V_{REF} = 0V		3	12	µA
I_{O-IN+}	Input restore current available, pin 2		180	300	600	µA
CMRR	Common mode rejection ratio	V_{REF} = ±2V	54	90		dB
+PSRR	Positive power supply rejection ratio	V_{CC} = 5V±5%, V_{EE} = -5V	50	60		dB
-PSRR	Negative power supply rejection ratio	V_{CC} = 5V, V_{EE} = -5V ±5%	50	60		dB
V_{Hmin}	HOLD pin high logic level		2			V
V_{Lmax}	HOLD pin low logic level				0.8	V
I_{IL}	Logic low input current	HOLD = LOW		40	100	µA
I_{IH}	Logic high input current	HOLD = HIGH		12		µA

AC electrical characteristics

V_{CC} = 5V, V_{EE} = -5V, R_F = 470V, G = 2, R_{LOAD} = 150V, C_{LOAD} = 10 pF, T_{amb} = 25°C unless otherwise stated.

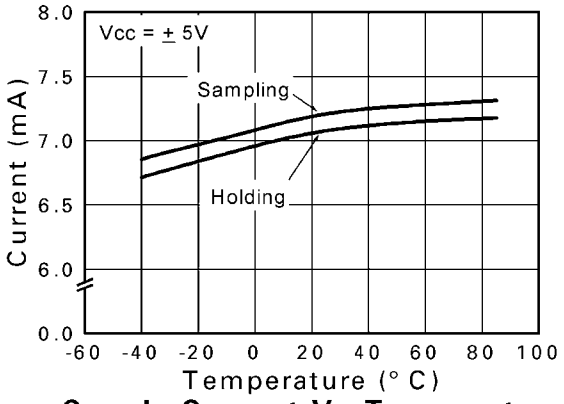
Parameter		Conditions	Min.	Typ.	Max.	Unit
Amplifier section HOLD = high unless otherwise stated						
SR	Slew rate	V_{OUT} = $2V_{PP}$		400		V/µs
BW_{-3}	Bandwidth, -3dB	V_{OUT} = $0.2V_{PP}$, G = 2		210		MHz
BW_{-3}	Bandwidth, -3dB	V_{OUT} = $0.2V_{PP}$, G = 1, R_F = 820V		210		MHz
$BW_{0.1}$	Bandwidth, ±0.1dB	V_{OUT} = 0.2VPP		30		MHz
dG	Differential gain, NTSC	HOLD = HIGH, f = 3.58 MHz, 280mV pk-pk, DC = -714 to +714 mV		0.08		%
dP	Differential phase, NTSC			0.1		deg
Restore section HOLD = low unless otherwise stated						
SR	Slew rate	V_{OUT} = $2V_{PP}$, C_{HOLD} = 0.01µF (*)		25		V/µs
t_{ENH}	Time to enable hold			25		ns
t_{DISH}	Time to disable hold			40		ns

NOTES:

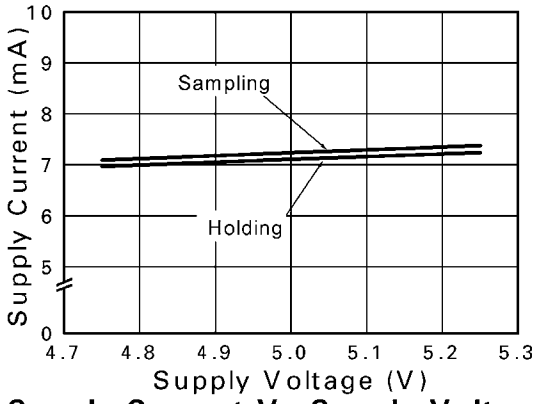
(*) During power-up and power-down, these voltage ratings require that signals be applied only when the power supply is connected.

(1) The voltage at the input to pin 2 should be limited to +2.7V for the best DC restoration accuracy. See later explanation under 'Common-mode input range.'

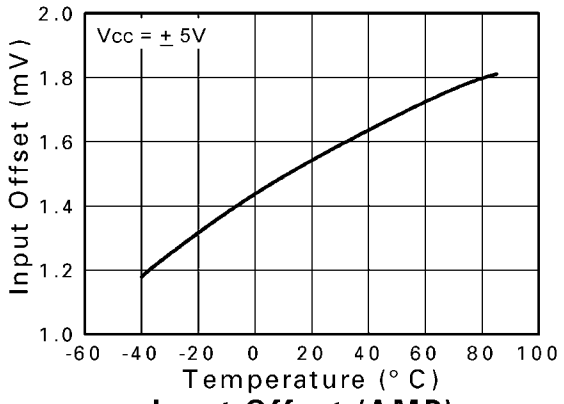
Typical characteristics



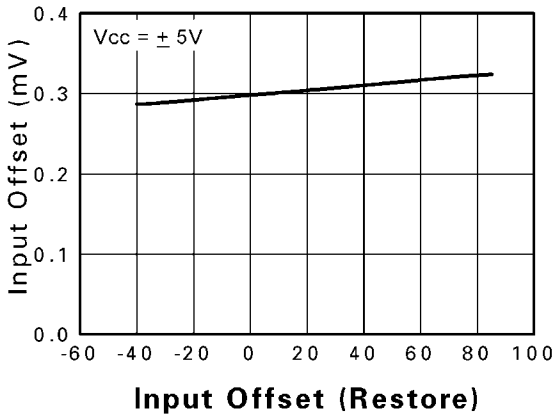
Supply Current Vs Temperature



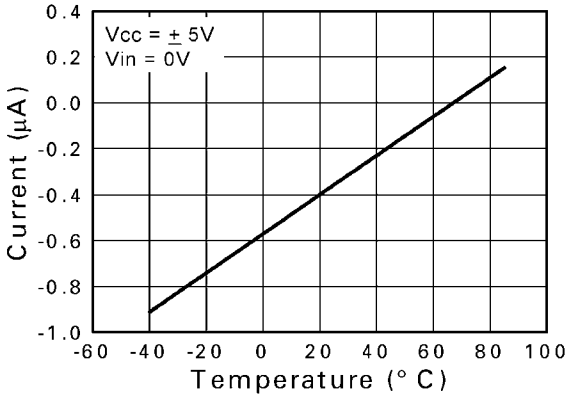
Supply Current Vs Supply Voltage



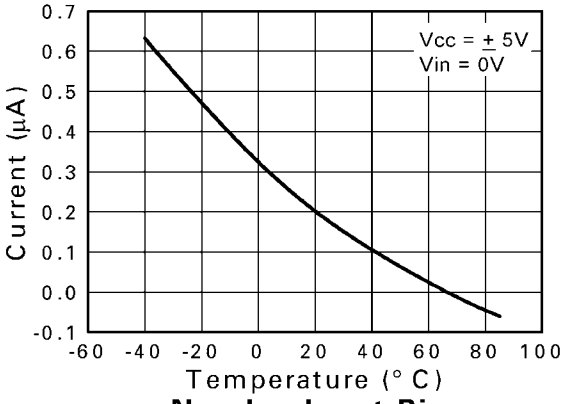
Input Offset (AMP) Vs Temperature



Input Offset (Restore) Vs Temperature

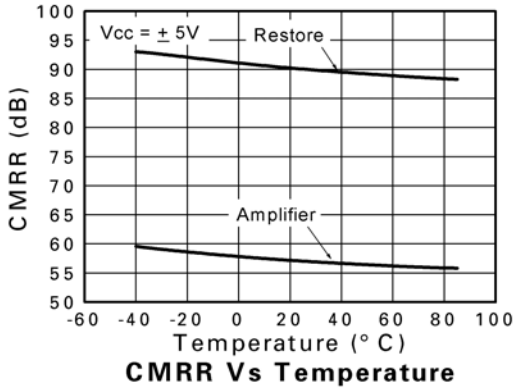


Inverting Input Bias Current Vs Temp

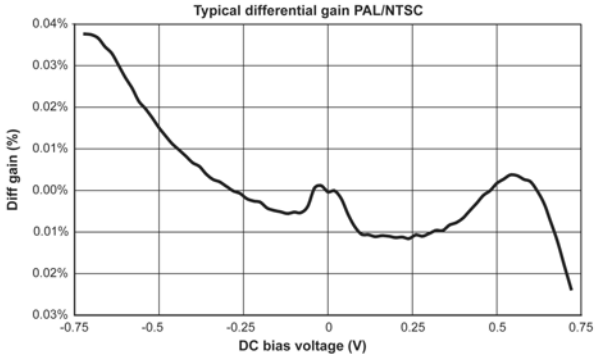


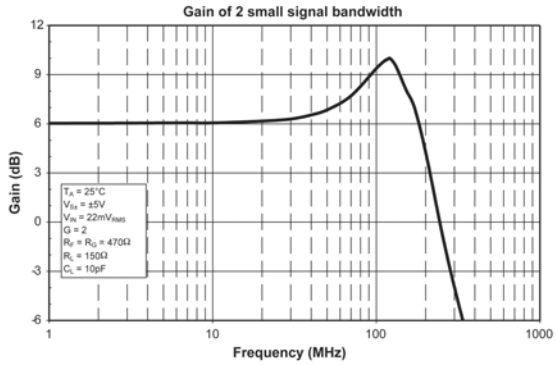
Non-Inv Input Bias Current Vs Temp

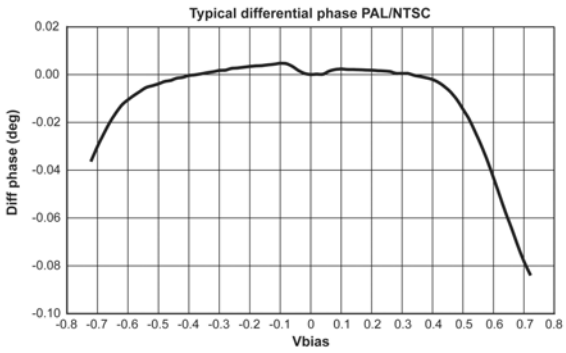
Typical characteristics (cont.)



CMRR Vs Temperature







ZXFV4089 detailed operating notes

Introduction
This device provides an uncommitted video feed-back amplifier together with a sample-hold system to allow restoration or level-shifting of the input waveform to a controlled DC level.

The connection diagram, Figure 1 shows a typical video signal application. No output termination is shown in the diagram, but if desired the output can drive a 75Ω cable via a 75Ω series terminating resistor.

Amplifier configuration
The main amplifier uses current feedback in a non-inverting configuration. Two external resistors are required to set the gain.

An external reference, V_{REF}, normally ground, is used to set the new DC level of the video signal. The input video signal is applied via an external input AC coupling capacitor, which is used to store a DC control level when the sample-hold switch is open. Typically an external sampling pulse (active low) is applied to the HOLD input. During this pulse, the sample-hold switch is closed. This completes the DC feedback loop and the stored level is driven towards a new value. At the end of the sampling pulse, the switch opens again and the DC level remains close to the new established value until the next sample pulse. The sample-hold charging current is limited to 300µA. Therefore the convergence towards the steady condition is typically slow, but after several HOLD pulse cycles, the DC level settles closely to the Reference level at the V_{REF} input.

The sample-hold loop contains the video amplifier within its path, and also includes an additional sample-hold sense amplifier that compares V_{REF} with the output voltage using an internal low-pass filter. In the high state, the switch is open and the average DC level remains fixed apart from a small drift due to the input bias current of the amplifier and switch leakage (see below).

DC restoration
The HOLD input is a TTL compatible signal that is buffered and controls the sample-hold switch. A logic LOW state closes the switch and so enables the feedback control loop to set the output level equal to V_{REF} (usually ground). The level of DC shift is maintained when the logic control returns to the HIGH state and the switch opens. In this way the whole waveform is conditionally level shifted, or 'restored' to the new DC level. Figure 2 shows the response of the circuit to a stationary or very slowly varying waveform with an initial voltage offset difference between V+ and V_{REF}, applied to the input coupling capacitor, when the HOLD input is cycled with a repetitive pulse waveform. When the HOLD input is at a logic LOW level, the signal input V+ is driven towards V_{REF}. After a number of cycles, the waveform settles to the DC stabilised value. The waveform is unaffected during the logic HIGH interval of the HOLD input.

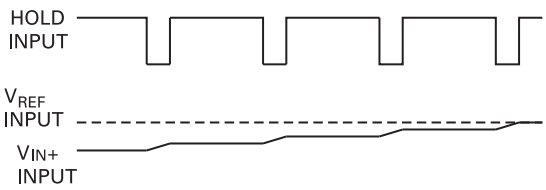


Figure 2 Response to slow input signal

Figure 3 shows a portion of a typical video waveform, where the sample pulse is synchronised to fall within the back porch interval. This can for example be achieved using the Zetex ZXFV4583 sync separator to derive the pulse as in the evaluation circuit described in the data sheet for that part. Again, during the logic LOW period of the HOLD input, the waveform is driven towards VREF. Eventually, after a few line scans, the video waveform is stabilised with the back porch level equal to V_{REF} and this condition is maintained despite any small changes in the input waveform.

In the video application, the HOLD input state will be HIGH during the picture line sweep and a negative-going sampling pulse of typically 1.2µs duration will be applied during a central portion of the back porch interval, so that the back porch or 'Black' level is clamped to V_{REF} (typically ground).

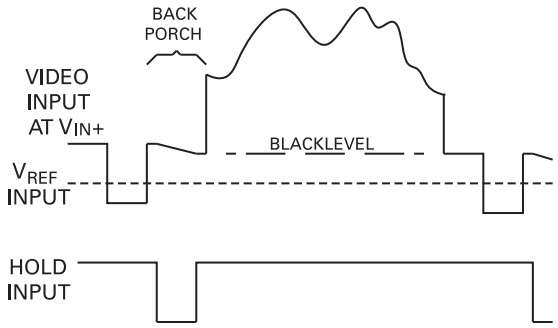


Figure 3 Response to typical video signal

If desired, by changing the external pulse timing the signal may be restored such that the sync tip voltage is clamped to V_{REF} instead of the back porch.

In either case, for each line scan, this gives a brightness level consistent with that of the original camera signal, despite the AC coupling. The value of the coupling capacitor affects two main characteristics of the circuit:

1. DC level acquisition change
2. DC level droop

DC level acquisition change
In the restore mode the available charging current, together with the capacitor value, determines the maximum DC voltage correction which can be applied at each sample. For a charging current limit of 300µA applied for 1.2µs, the charge injected is:

Qmax = 300µA x 1.2µs = 360pC

Then the maximum voltage shift correction is:

Vmax = Qmax/C = 360pC / 0.01µF
= 36mV

DC level droop
In the hold state, a small voltage drift is caused by leakage from the sample-hold circuit and bias current from the main amplifier charging or discharging the coupling capacitor.

The drift rate is equal to the bias/leakage current of up to about 1µA divided by the coupling capacitor value. For a coupling capacitor of 0.01µF the drift rate is then up to ±100µV/µs.

For a typical video line scan the switch remains open for the rest of the scan duration, or about 62µs. The drift at the end of the line scan has therefore accumulated to about 6.2mV.

This is acceptable for most applications, but if desired it can be reduced by increasing the value of the coupling capacitor. This will result in a proportionately smaller value of the maximum available correction voltage at each scan as described above. Normally, once settled, the video system requires only a very small correction at each scan, so this will not present any problem.

Supply filtering and printed circuit layout
In the applied circuit, the power filtering and printed layout design needs special attention as is appropriate for a high-speed analog circuit. For each supply lead, use a leadless ceramic chip capacitor placed very close to the device power pin. A value of 0.1µF is recommended. In addition, a larger value capacitor, which should be ceramic or solid tantalum construction, with a value of 1 to 10µF, is also recommended for connection to each supply fairly close to the device. The layout naturally requires some short interconnections on the component side (top copper layer) and a continuous ground plane should be provided on another layer with plated via holes providing low inductance ground connections for the device and other components. The amplifier frequency response is affected to some extent by stray capacitance at the inverting input at pin 1. This effect can be minimised by providing a small cut-out area in the ground plane and other layers around pin 1, though this may not always be necessary for the application.

Further Applications Information
The ZXFV4089 is a high speed device requiring the appropriate care in the layout of the application printed circuit board. A continuous ground plane construction is preferred. Suitable power supply decoupling suggested includes a 100nF leadless ceramic capacitor close to the power supply connections at pin 8 and pin 6.

As stated earlier the main video amplifier of the ZXFV4089 is a current feedback amplifier. Compared to a voltage-feedback amplifier, current feedback provides better bandwidths at higher gains and also much faster slew rates. To optimize performance from a current feedback amplifier choice of feedback resistor is very important. In this case, typically the device will be used with a voltage gain of two, using two resistors of 1kΩ as in Figure 1. Stray capacitance at the inverting input node of this circuit can affect frequency and pulse response, so the printed circuit layout should take account of this. Place the feedback resistors as close as possible to the inverting input pin and minimize the printed metal connected to this pin.

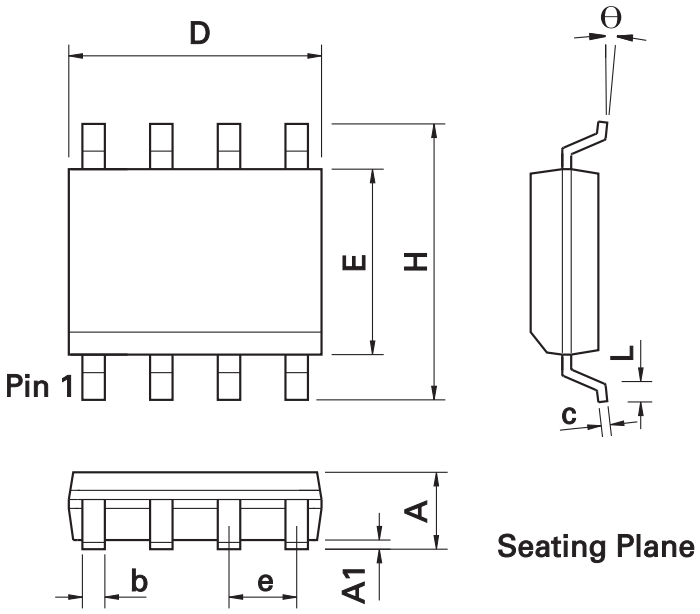
Common-mode input range
The signal input voltage range is determined partly by the common-mode input range of the main amplifier. The amplifier configuration is non-inverting, and so the inverting input will follow the signal input voltage. It is also necessary to observe the maximum limit on the value of V_{REF} (±2V) which is less than the amplifier input voltage range. Therefore the input range of the system is limited to this value. In addition the restore amplifier voltage input range is restricted to a similar value.

Attention is drawn to the footnote of the DC electrical characteristics table, regarding input signal amplitude. The video signal is ac coupled into the main amplifier and clamped to V_{REF}. As a result of this the actual voltage seen by the device input at pin 2 is the sum of V_{REF} plus the video input signal voltage excursion above V_{REF} (when clamping the back porch, this excursion is normally the luminance waveform of up to about 0.72V white level). At a particular positive value at pin 2 close to 2.7V, the leakage current of the Sample-hold switch increases causing an increase in the droop rate. Therefore, for example, a reference voltage of 2V with a peak white video signal of 0.7V could result in increased restoration error arising from the increased DC offset. If pin 2 is driven above +2.7V peak voltage the DC restoration accuracy could be affected and care should be taken in this respect. When using 0.7V luminance, this is consistent with the maximum recommended reference voltage of +2V.

Evaluation circuit

An evaluation circuit is available to allow demonstration of the video black-level clamping function. The circuit uses the Zetex ZXFV4583 sync separator circuit to provide the HOLD function timing signal. This circuit is described in the datasheet for ZXFV4583. To order the evaluation board, ask for ZXFV4583EV.

Package outline - SO8



DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.053	0.069	1.35	1.75	e	0.050 BSC		1.27 BSC	
A1	0.004	0.010	0.10	0.25	b	0.013	0.020	0.33	0.51
D	0.189	0.197	4.80	5.00	c	0.008	0.010	0.19	0.25
H	0.228	0.244	5.80	6.20	θ	0°	8°	0°	8°
E	0.150	0.157	3.80	4.00	h	0.010	0.020	0.25	0.50
L	0.016	0.050	0.40	1.27	-	-	-	-	-

Note: Controlling dimensions are in inches. Approximate dimensions are provided in millimeters

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"Active"	Product status recommended for new designs
"Last time buy (LTB)"	Device will be discontinued and last time buy period and delivery is in effect
"Not recommended for new designs"	Device is still in production to support existing designs and production
"Obsolete"	Production has been discontinued

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"Provisional version"	This term denotes a pre-release datasheet. It provides a clear indication of anticipated performance. However, changes to the test conditions and specifications may occur, at any time and without notice.
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