

Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from, Europe, America and south Asia, supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of "Quality Parts, Customers Priority, Honest Operation, and Considerate Service", our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip, ALPS, ROHM, Xilinx, Pulse, ON, Everlight and Freescale. Main products comprise IC, Modules, Potentiometer, IC Socket, Relay, Connector. Our parts cover such applications as commercial, industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China











60V HIGH ACCURACY BUCK/BOOST/BUCK-BOOST LED DRIVER-CONTROLLER

Description

The ZXLD1371 is an LED driver controller IC for driving external MOSFETs to drive high-current LEDs. It is a multi-topology controller enabling it to efficiently control the current through series connected LEDs. The multi-topology enables it to operate in buck, boost and buck-boost configurations.

The 60V capability coupled with its multi-topology capability enables it to be used in a wide range of applications and drive in excess of 15 LEDs in series.

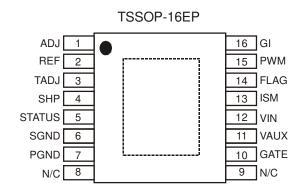
The ZXLD1371 is a modified hysteretic controller using a patent pending control scheme providing high output current accuracy in all three modes of operation. High accuracy dimming is achieved through DC control and high frequency PWM control.

The ZXLD1371 uses two pins for fault diagnosis. A flag output highlights a fault, while the multi-level status pin gives further information on the exact fault.

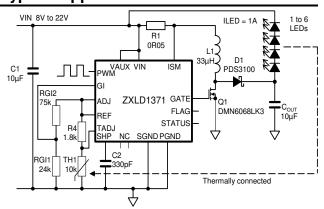
Features

- 0.5% typical output current accuracy
- 5 to 60V operating voltage range
- LED driver supports Buck, Boost and Buck-boost
- configurations
- Wide dynamic range dimming
 - o 10:1 DC dimming
 - o 1000:1 dimming range at 500Hz
- Up to 1MHz switching
- High temperature control of LED current using T_{ADJ}
- Available in Automotive Grade with AEC-Q100 and TS16949 certification
- Lead-Free Finish; RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- An Automotive-Compliant Part is Available Under Separate Datasheet (ZXLD1371Q)

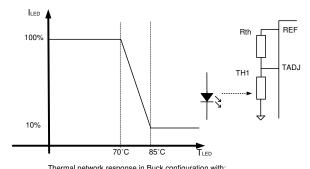
Pin Assignments



Typical Application Circuit



Buck-Boost Diagram Utilizing Thermistor and TAD.I



Thermal network response in Buck configuration with: Rth = $1.8k\Omega$ and TH1= $10k\Omega$ (beta =3900)

Curve Showing LED Current vs. TLED

Notes: 1. EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant. All applicable RoHS exemptions applied.

- 2. See http://www.diodes.com/quality/lead-free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.



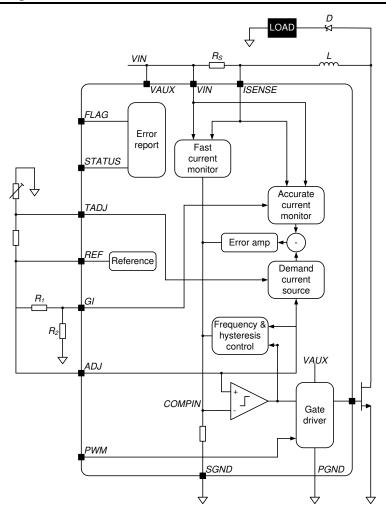
Pin Descriptions

Pin Name	Pin	Type (Note 4)	Description
ADJ	1	ı	Adjust input (for DC output current control) Connect to REF to set 100% output current. Drive with DC voltage (125mV <v<sub>ADJ< 1.25V) to adjust output current from 10% to 100% of set value. The ADJ pin has an internal clamp that limits the internal node to less than 3V. This provides some failsafe should they get overdriven</v<sub>
REF	2	0	Internal 1.25V reference voltage output
TADJ	3	I	Temperature Adjust input for LED thermal current control Connect thermistor/resistor network to this pin to reduce output current above a preset temperature threshold. Connect to REF to disable thermal compensation function. (See section on thermal control.)
SHP	4	I/O	Shaping capacitor for feedback control loop Connect 330pF ±20% capacitor from this pin to ground to provide loop compensation
STATUS	5	0	Operation status output (analog output) Pin is at 4.5V (nominal) during normal operation. Pin switches to a lower voltage to indicate specific operation warnings or fault conditions. (See section on STATUS output.) Status pin voltage is low during shutdown mode
SGND	6	Р	Signal ground (Connect to 0V)
PGND	7	Р	Power ground - Connect to 0V and pin 8 to maximize copper area
N/C	8	-	Not Connected internally – recommend connection to pin 7, (PGND), to maximize PCB copper for thermal dissipation
N/C	9		Not Connected internally – recommend connection pin 10 (GATE) to permit wide copper trace to gate of MOSFET
GATE	10	0	Gate drive output to external NMOS transistor – connect to pin 9
V _{AUX}	11	Р	Auxiliary positive supply to internal switch gate driver At V _{IN} < 8V; a bootstrap circuit is recommended to ensure adequate gate drive voltage (see Applications section) At V _{IN} > 8V; connect to V _{IN} At V _{IN} > 24V; to reduce power dissipation, V _{AUX} can be connected to an 8V to 15V auxiliary power supply (see Applications section). Decouple to ground with capacitor close to device (see Applications section)
V _{IN}	12	Р	Input supply to device 5V to 60V Decouple to ground with capacitor close to device (refer to Applications section)
ISM	13	I	Current monitor input. Connect current sense resistor between this pin and V_{IN} The nominal voltage, V_{SENSE} , across the resistor is 218mV fixed in Buck mode and initially 225mV in Boost and Buck-Boost modes, varying with duty cycle.
FLAG	14	0	Flag open drain output Pin is high impedance during normal operation Pin switches low to indicate a fault, or warning condition
PWM	15	I	Digital PWM output current control Pin driven either by open Drain or push-pull 3.3V or 5V logic levels. Drive with frequency higher than 100Hz to gate output 'on' and 'off' during dimming control. The device enters standby mode when PWM pin is driven with logic low level for more than 15ms nominal (Refer to application section for more details)
GI	16	1	Gain setting input Used to set the device in Buck mode or Boost, Buck-boost modes and to control the sense voltage in Boost and Buck-boost modes Connect to ADJ pin for Buck mode operation For Boost and Buck-boost modes, connect to resistive divider from ADJ to SGND. The GI divider is required to compensate for duty cycle gating in the internal feedback loop (see Application section). The GI pin has an internal clamp that limits the internal node to less than 3V. This provides some failsafe should it become overdriven.
EP	PAD	Р	Exposed pad. Connect to 0V plane for electrical and thermal management.

Note: 4. Type refers to whether or not pin is an Input, Output, Input/Output or Power supply pin.



Functional Block Diagram



Absolute Maximum Ratings (Voltages to GND Unless Otherwise Stated) (Note 5)

Symbol	Parameter	Rating	Unit
V _{IN}	Input supply voltage	-0.3 to 65	V
V _{AUX}	Auxiliary supply voltage	-0.3 to 65	V
V _{ISM}	Current monitor input relative to GND	-0.3 to 65	V
V _{SENSE}	Current monitor sense voltage (V _{IN} -V _{ISM})	-0.3 to 5	V
V _{GATE}	Gate driver output voltage	-0.3 to 20	V
IGATE	Gate driver continuous output current	18	mA
V _{FLAG}	Flag output voltage	-0.3 to 40	V
V _{PWM} , V _{ADJ} , V _{TADJ} , V _{GI} , V _{PWM}	Other input pins	-0.3 to 5.5	V
TJ	Maximum junction temperature	150	°C
T _{ST}	Storage temperature	-55 to 150	°C

Note: 5. For correct operation SGND and PGND should always be connected together.

Stresses greater than the 'Absolute Maximum Ratings' specified above, may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions exceeding those indicated in this specification is not implied. Device reliability may be affected by exposure to absolute maximum rating conditions for extended periods of time.

Semiconductor devices are ESD sensitive and may be damaged by exposure to ESD events. Suitable ESD precautions should be taken when handling and transporting these devices.



Package Thermal Data

Thermal Resistance	Package	Typical	Unit
Junction-to-Ambient, θ _{JA} (Note 6)	TSSOP-16 EP	50	°C/W
Junction-to-Case, θ _{JC}	TSSOP-16 EP	23	°C/W

Recommended Operating Conditions (-40°C ≤ T_J ≤ 125°C)

Symbol	Parameter	Performance/Comment	Min	Max	Unit
	Input supply voltage range	Normal Operation	8.0	60	V
V_{IN}		(Note 7) Reduced performance operation	5.0	8.0	
		Normal Operation	8.0	60	
V _{AUX}	Auxiliary supply voltage range (Note 8)	(Note 7) Reduced performance operation	5.0	8.0	V
V _{SENSE}	Differential input voltage	V_{IN} - V_{ISM} , with $0 \le V_{ADJ} \le 2.5$	0	450	mV
V_{ADJ}	External dc control voltage applied to ADJ pin to adjust output current	DC brightness control mode from 10% to 100%	0.125	1.25	V
I _{REF}	Reference external load current	REF sourcing current	-	1	mA
f _{max}	Recommended switching frequency range	(Note 9)	300	1,000	kHz
V_{TADJ}	Temperature adjustment (T _{ADJ}) input voltage range	-	0	V_{REF}	V
t	Recommended PWM dimming frequency range	To achieve 1000:1 resolution	100	500	Hz
f _{PWM}	Recommended FWW dimining frequency range	To achieve 500:1 resolution	100	1,000	Hz
t _{PWMH/L}	PWM pulse width in dimming mode	PWM input high or low	0.002	10	ms
V_{PWMH}	PWM pin high level input voltage	-	2	5.5	V
V _{PWML}	PWM pin low level input voltage	-	0	0.4	V
TJ	Operating Junction Temperature Range	-	-40	125	°C
GI	Gain setting ratio for boost and buck-boost modes	Ratio= V _{GI} /V _{ADJ}	0.20	0.50	-

Notes:

- Measured on "High Effective Thermal Conductivity Test Board" according to JESD51.

 Device starts up above 5.4V and as such the minimum applied supply voltage has to be above 5.4V (plus any noise margin). The ZXLD1371 will however, continue to function when the input voltage is reduced from \geq 8V down to 5.0V.
 - When operating with input voltages below 8V the output current and device parameters may deviate from their normal values; and is dependent on power MOSFET switch, load and ambient temperature conditions. To ensure best operation in Boost and Buck-boost modes with input voltages, VIN, between 5.0 and 8V a suitable boot-strap network on VAUX pin is recommended.
 - Performance in Buck mode will be reduced at input voltages (VIN, VAUX) below 8V. a boot-strap network cannot be implemented in buck mode and so a suitable low V_T MOSFET should be selected.
- VAUX can be driven from a voltage higher than VIN to provide higher efficiency at low VIN voltages, but to avoid false operation; a voltage should not be applied to VAUX in the absence of a voltage at VIN. VAUX can also be operated at a lower voltage than VIN to increase efficiencies
- The device contains circuitry to control the switching frequency to approximately 400kHz. The maximum and minimum operating frequency is not tested in production.



Electrical Characteristics (Test conditions: V_{IN} = V_{AUX} = 12V, T_A = 25°C, unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Тур	Max	Units
Supply and i	reference parameters					
V _{UV-}	Undervoltage detection threshold Normal operation to switch disabled	V _{IN} or V _{AUX} falling (Note 10)	-	4.5	-	٧
V_{UV+}	Undervoltage detection threshold Switch disabled to normal operation	V _{IN} or V _{AUX} rising (Note 10)	-	4.9	-	V
I _{Q-IN}	Quiescent current into V _{IN}	PWM pin floating.	-	1.5	3	mA
I _{Q-AUX}	Quiescent current into V _{AUX}	Output not switching	-	150	300	μΑ
I _{SB-IN}	Standby current into V _{IN} .	PWM pin grounded	-	90	150	μΑ
I _{SB-AUX}	Standby current into V _{AUX} .	for more than 15ms	-	0.7	10	μΑ
V_{REF}	Internal reference voltage	No load	1.237	1.25	1.263	V
437	Change in reference voltage with output	Sourcing 1mA	-5	-	-	mV
ΔV_{REF}	current	Sinking 25µA	-	-	5	mv
V _{REF_LINE}	Reference voltage line regulation	$V_{IN} = V_{AUX}, 8.0V < V_{IN} = <60V$	-60	-90	-	dB
V _{REF-TC}	Reference temperature coefficient	-	-	±50	-	ppm/°C
DC-DC con	verter parameters					
_	ADJ input current (Note 11)	V _{ADJ} ≤ 1.25V	-	-	100	nA
I _{ADJ}		$V_{ADJ} = 5.0V$	-	-	5	μΑ
V_{GI}	GI Voltage threshold for boost and buck-boost modes selection (Note 11)	V _{ADJ} = 1.25V	-	-	0.8	٧
	GI input current (Note 11)	V _{GI} ≤ 1.25V	-	-	100	nA
I _{GI}		$V_{GI} = 5.0V$	-	-	5	μΑ
I _{PWM}	PWM input current	$V_{PWM} = 5.5V$	-	36	100	μΑ
t_{PWMoff}	PWM pulse width (to enter shutdown state)	PWM input low	10	15	25	ms
T _{SDH}	Thermal shutdown upper threshold (GATE output forced low)	Temperature rising	-	150	-	°C
T _{SDL}	Thermal shutdown lower threshold (GATE output re-enabled)	Temperature falling	-	125	-	°C
High-Side Co	urrent Monitor (Pin ISM)					
I _{ISM}	Input Current	Measured into ISM pin V _{ISM} = 12V	-	11	20	μΑ
V _{SENSE_acc}	Accuracy of nominal V _{SENSE} threshold voltage	1.057/	-	±0.25	±2	%
V _{SENSE-OC}	Overcurrent sense threshold voltage	V _{ADJ} = 1.25V	300	350	375	mV

Notes: 10. UVLO levels are such that all ZXLD1371 will function above 5.4V for rising supply voltages and function down to 5V for falling supply voltages. 11. The ADJ and GI pins have an internal clamp that limits the internal node to less than 3V. This provides some failsafe should those pins get



$\textbf{Electrical Characteristics} \ \, \text{(continued) (Test conditions: } \ \, V_{\text{IN}} = V_{\text{AUX}} = 12 \text{V}, \ \, T_{\text{A}} = 25 ^{\circ} \text{C}, \ \, \text{unless otherwise specified.)}$

Symbol	Parameter	Conditions	Min	Тур	Max	Units
Output Para	ameters					
V_{FLAGL}	FLAG pin low level output voltage	Output sinking 1mA	1	-	0.5	V
I _{FLAGOFF}	FLAG pin open-drain leakage current	$V_{FLAG} = 40V$	ı	-	1	μΑ
		Normal operation	4.2	4.5	4.8	
		Out of regulation (V _{SHP} out of range) (Note 13)	3.3	3.6	3.9	
	STATUS Flag no-load output voltage	V _{IN} undervoltage (V _{IN} < UVLO)	3.3	3.6	3.9	V
V_{STATUS}	(Note 12)	Switch stalled (t _{ON} or t _{OFF} > 100µs)	3.3	3.6	3.9	
		Over-temperature (T _J > 125°C)	1.5	1.8	2.1	
		Excess sense resistor current (V _{SENSE} > 0.32V)	0.6	0.9	1.2	
R _{STATUS}	Output impedance of STATUS output	Normal operation	-	10	-	kΩ
Driver outp	ut (PIN GATE)	•				•
V_{GATEH}	High-level output voltage	No load Sourcing 1mA $V_{IN} = V_{AUX} = 12V$ (Note 14)	9.5	10.5	-	V
V_{GATEL}	Low-level output voltage	Sinking 1mA, (Note 15)	-	-	0.5	٧
V _{GATECL}	High level GATE CLAMP voltage	$V_{IN} = V_{AU X} = V_{ISM} = 18V$ $I_{GATE} = 1mA$	-	12.8	15	V
I _{GATE}	Dynamic peak current available during rise or fall of output voltage	Charging or discharging gate of external switch with $Q_G = 10nC$ and $400kHz$	-	±300	-	mA
t _{stall}	Time to assert 'STALL' flag and warning on STATUS output (Note 16)	GATE low or high		100	170	μs
LED Therm	al control circuit (T _{ADJ}) parameters					
V_{TADJH}	Upper threshold voltage	Onset of output current reduction (V _{TADJ} falling)	560	625	690	mV
V_{TADJL}	Lower threshold voltage	Output current reduced to <10% of set value (V _{TADJ} falling)	380	440	500	mV
I_{TADJ}	T _{ADJ} pin Input current	$V_{TADJ} = 1.25V$	-	-	1	μΑ

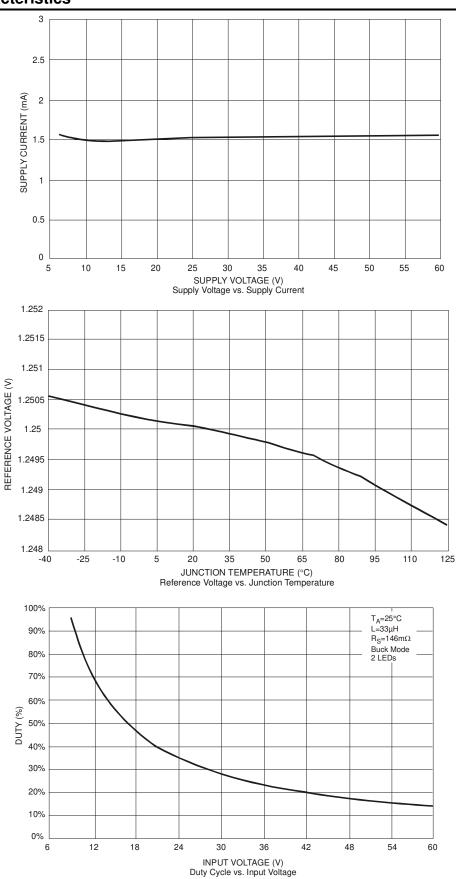
Notes: 12. In the event of more than one fault/warning condition occurring, the higher priority condition will take precedence. For example, 'Excessive coil current' and 'Out of regulation' occurring together will produce an output of 0.9V on the STATUS pin. These STATUS pin voltages apply for an input voltage to V_{IN} of 7.5V < V_{IN} < 60V. Below 7.5V the STATUS pin voltage levels reduce and therefore may not report the correct status. For 5.4V < V_{IN} < 7.5V the flag pin still reports any error by going low. At low V_{IN} in Boost and Buck-boost modes an over-current status may be indicated when operating at high boost ratios – this due to the feedback loop increasing the sense voltage.

For more information see the Application Information section about Flag/Status levels.

- 13. Flag is asserted if $V_{SHP} < 1.5V$ or $V_{SHP} > 2.5V$.
- 14. GATE is switched to the supply voltage V_{AUX} for low values of V_{AUX} (5V ≤ V_{AUX} ≤ ~12V). For V_{AUX} > 12V, GATE is clamped internally to prevent it exceeding 15V. Below 12V the minimum gate pin voltage will be 2.5V below Vaux.
- 15. GATE is switched to PGND by an NMOS transistor.
- 16. If toN exceeds t_{STALL}, the device will force GATE low to turn off the external switch and then initiate a restart cycle. During this phase, ADJ is grounded internally and the SHP pin is switched to its nominal operating voltage, before operation is allowed to resume. Restart cycles will be repeated automatically until the operating conditions are such that normal operation can be sustained. If t_{OFF} exceeds t_{STALL}, the switch will remain off until normal operation is possible.

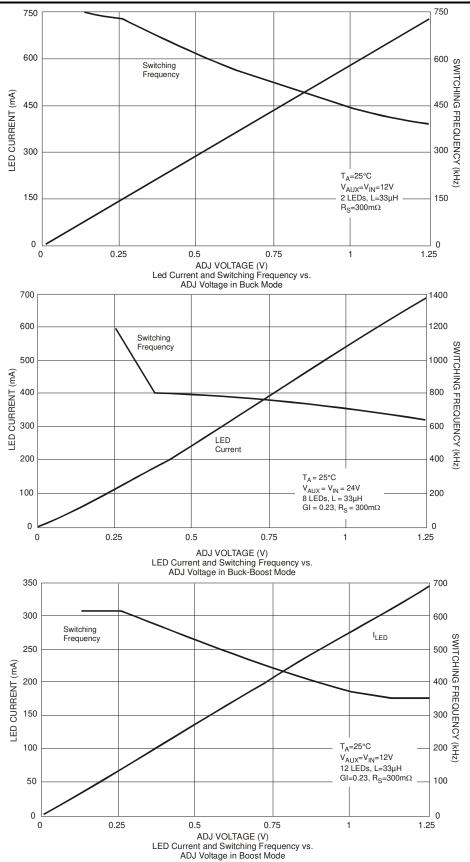


Typical Characteristics



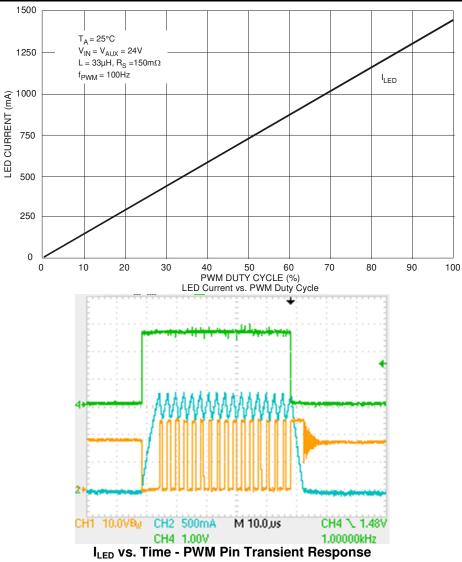


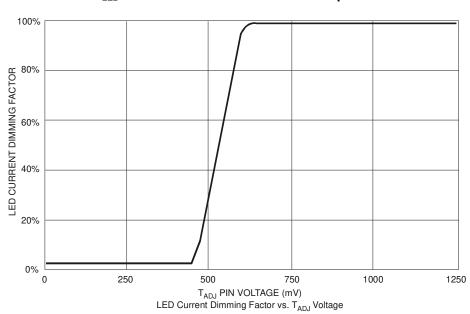
Typical Characteristics - Linear/DC Dimming





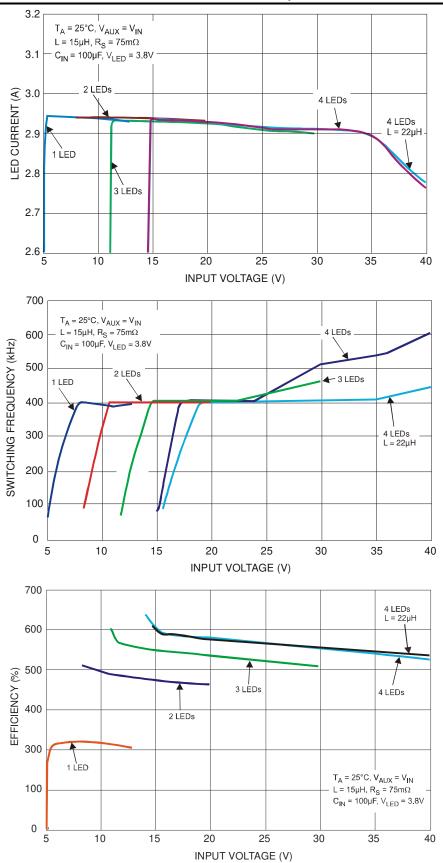
Typical Characteristics - PWM/Thermal Dimming





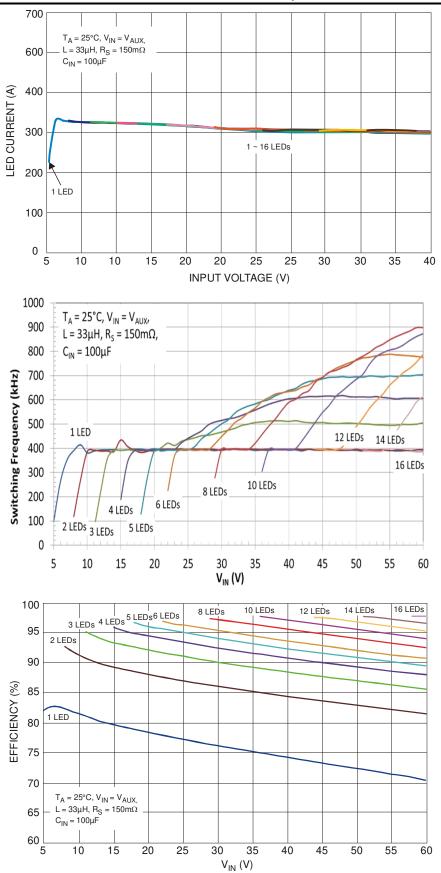


Typical Characteristics - Buck Mode - R_S = 75mΩ - L = 33μH - I_{LED} = 2.9A



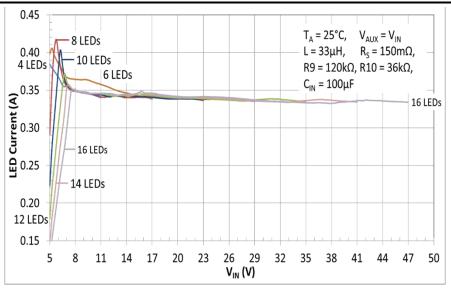


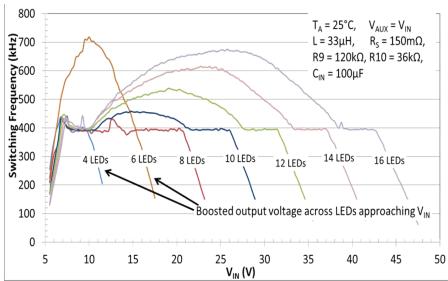
Typical Characteristics - Buck Mode - R_S =150m Ω - L = 33 μ H - I_{LED} = 1.45A

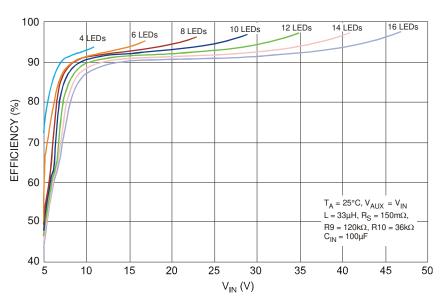




Typical Characteristics - Boost Mode - I_{LED} = 350mA - R_S = 150m Ω - GI_{RATIO} = 0.23

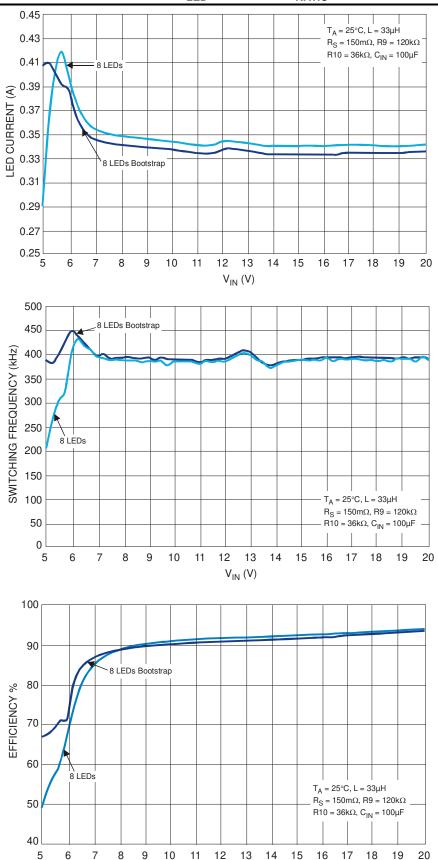








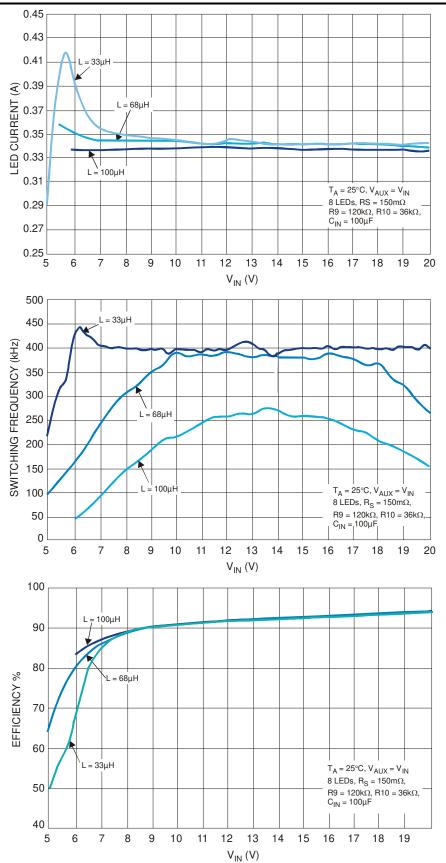
Typical Characteristics - Boost Mode - I_{LED} = 350mA - GI_{RATIO} = 0.23 - Bootstrap comparison



 $V_{IN}(V)$

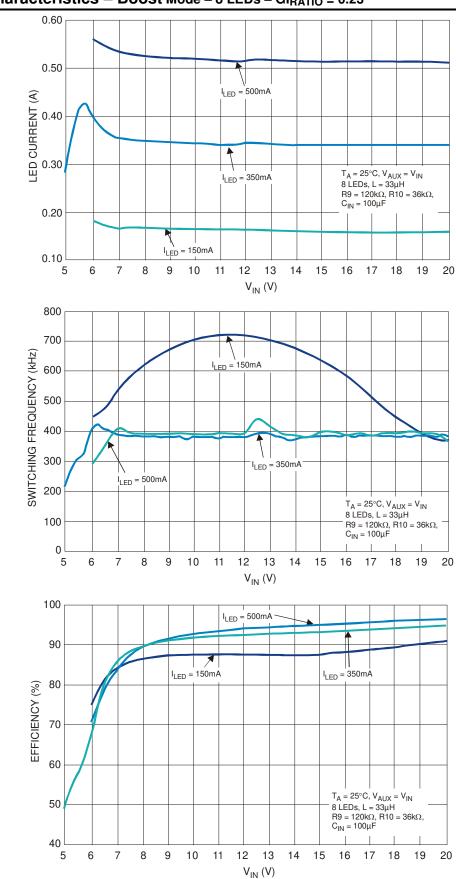


Typical Characteristics - Boost Mode - I_{LED} = 350mA - R_S = 150m Ω - GI_{RATIO} = 0.23



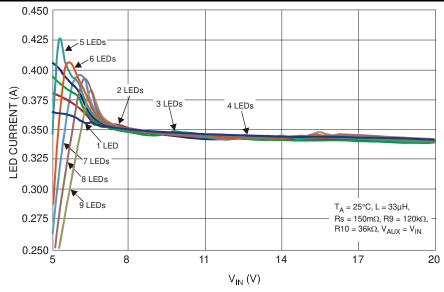


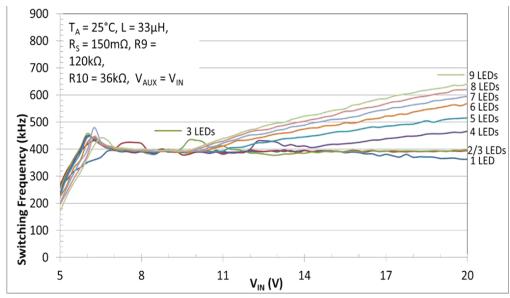
Typical Characteristics - Boost Mode - 8 LEDs - GIRATIO = 0.23

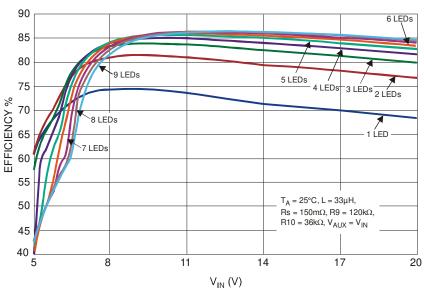




Typical Characteristics – Buck-Boost Mode – R_S = 150m Ω - I_{LED} = 350mA – GI_{RATIO} = 0.23

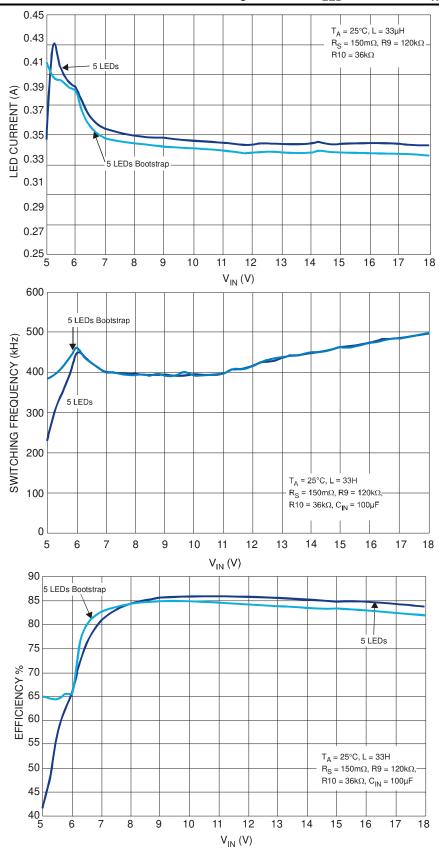






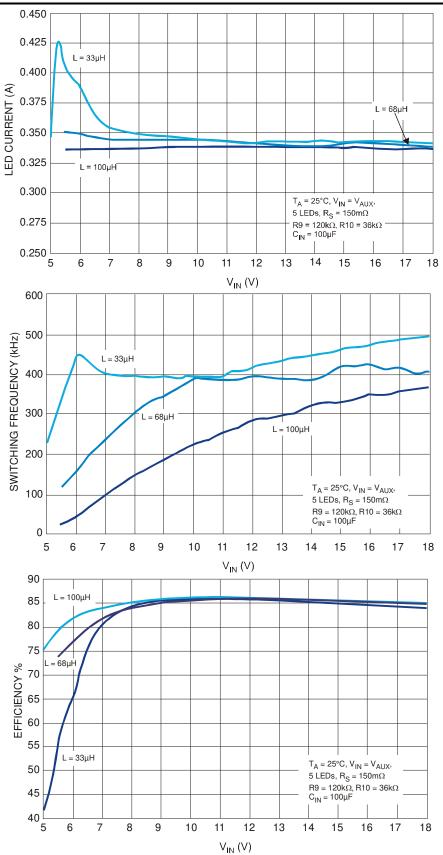


Typical Characteristics – Buck-Boost Mode – R_S = 150m Ω - I_{LED} = 350mA – GI_{RATIO} = 0.23



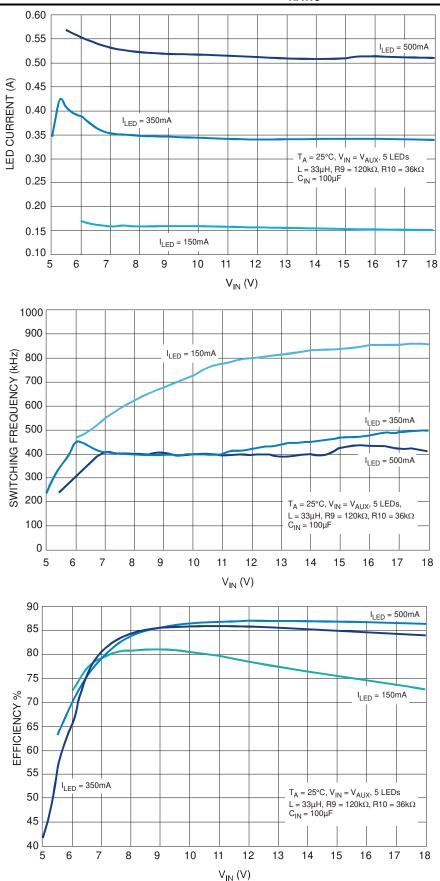


Typical Characteristics - Buck-Boost Mode - R_S = 150m Ω - I_{LED} = 350mA - GI_{RATIO} = 0.23





Typical Characteristics - Buck-Boost Mode -5 LEDs GIRATIO = 0.23





Applications Information

The ZXLD1371 is a high-accuracy hysteretic inductive buck/boost/buck-boost controller designed to be used with an external NMOS switch for current-driving single or multiple series-connected LEDs. The device can be configured to operate in buck, boost, or buck-boost modes by suitable configuration of the external components as shown in the schematics shown in the device operation description.

DEVICE DESCRIPTION

a) Buck mode - the most simple buck circuit is shown in Figure 1 Control of the LED current buck mode is achieved by sensing the coil current in the sense resistor Rs, connected between the two inputs of a current monitor within the control loop block. An output from the control loop drives the input of a comparator which drives the gate of the external NMOS switch transistor Q1 via the internal Gate Driver. When the switch is on, the drain voltage of Q1 is near zero. Current flows from VIN, via Rs, LED, coil and switch to ground. This current ramps up until an upper threshold value is reached (see Figure 2). At this point GATE goes low, the switch is turned off and the drain voltage increases to $V_{\mbox{\scriptsize IN}}$ plus the forward voltage, V_F, of the Schottky diode D1. Current flows via Rs, LED, coil and D1 back to V_{IN}. When the coil current has ramped down to a lower threshold value, GATE goes high, the switch is turned on again and the cycle of events repeats, resulting in continuous oscillation. The feedback loop adjusts the NMOS switch duty cycle to stabilize the LED current in response to changes in external conditions, including input voltage and load voltage.

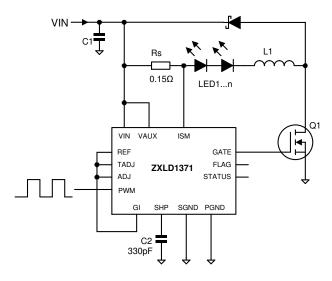


Figure 1. Buck configuration

The average current in the sense resistor, LED and coil is equal to the average of the maximum and minimum threshold currents. The ripple current (hysteresis) is equal to the difference between the thresholds. The control loop maintains the average LED current at the set level by adjusting the switch duty cycle continuously to force the average sense resistor current to the value demanded by the voltage on the ADJ pin. This minimizes variation in output current with changes in operating conditions.

The control loop also regulates the switching frequency by varying the level of hysteresis. The hysteresis has a defined minimum (typ 5%) and a maximum (typ 30%). The frequency may deviate from nominal in some conditions. This depends upon the desired LED current, the coil inductance and the voltages at the input and the load. Loop compensation is achieved by a single external capacitor C2, connected between SHP and SGND.

The control loop sets the duty cycle so that the sense voltage is: V_{SENSE} = 0.218 $\left(\frac{V_{ADJ}}{V_{DEE}}\right)$

$$V_{SENSE} = 0.218 \left(\frac{V_{ADJ}}{V_{REF}} \right)$$

Therefore.

$$I_{LED} = \left(\frac{0.218}{R_S}\right) \left(\frac{V_{ADJ}}{V_{REF}}\right)$$
 (Buck mode) Equation 1

If the ADJ pin is connected to the REF pin, this simplifies to:

$$I_{LED} = \left(\frac{0.218}{R_S}\right)$$
 (Buck mode).

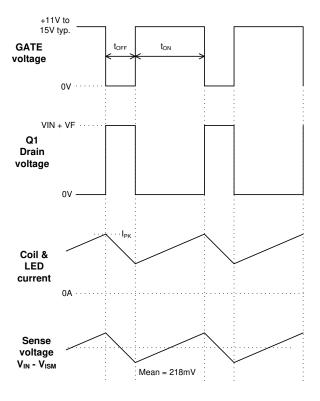


Figure 2. Operating waveforms (Buck mode)

February 2017

© Diodes Incorporated



b) Boost and Buck-Boost modes - the most simple boost/buck-boost circuit is shown in Figure 3

Control in Boost and Buck-boost mode is achieved by sensing the

 the load voltage VLEDS plus the forward voltage of D1 in Boost configuration,

or

2) the load voltage VLEDS plus the forward Current flows via Rs, coil, D1 and LED back to VIN (Buck-boost

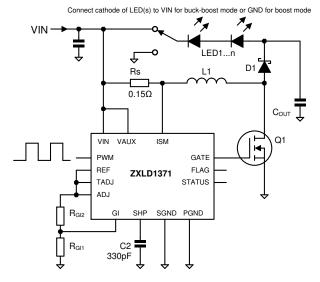


Figure 3. Boost and Buck-boost configuration

The feeback loop adjusts the NMOS switch duty cycle to stabilize

The average current in the sense resistor and coil, I_{RS} , is equal to

The average current in the LED, I_{LED} , is always less than I_{RS} . The $GI_ADJ = \left(\frac{RGI1}{RGI1 + RGI2}\right)$ **Equation 2** (Boost and Buck-boost modes)

The control loop sets the duty cycle so that the sense resistor current is

$$I_{RS} = \begin{pmatrix} \frac{0.225}{R_S} \end{pmatrix} \begin{pmatrix} \frac{GI_ADJ}{1-D} \end{pmatrix} \begin{pmatrix} \frac{V_{ADJ}}{V_{REF}} \end{pmatrix}$$
 Equation 3
(Boost and Buck-boost modes)

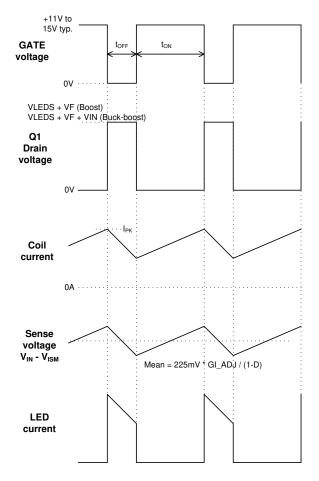


Figure 4. Operating waveforms (Boost and Buck-boost modes)

 I_{RS} equals the coil current. The coil is connected only to the switch and the schottky diode. The schottky diode passes the LED current. Therefore the average LED current is the coil current multiplied by the schottky diode duty cycle, 1-D.

ZXLD1371 Document number: DS35436 Rev. 2 - 2 21 of 43 www.diodes.com



$$I_{LED} = I_{RS} (1-D) = \left(\frac{0.225}{R_S}\right) GI_ADJ \left(\frac{V_{ADJ}}{V_{REF}}\right)$$
 (Boost and Buck-boost) **Equation 4**

This shows that the LED current depends on the ADJ pin voltage, the reference voltage and 3 resistor values (RS, RGI1 and RGI2). It is independent of the input and output voltages.

If the ADJ pin is connected to the REF pin, this simplifies to

$$I_{LED} = \left(\frac{0.225}{R_S}\right) GI_ADJ$$
 (Boost and Buck-boost)

Now I_{LED} is dependent only on the 3 resistor values.

Considering power dissipation and accuracy, it is useful to know how the mean sense voltage varies with input voltage and other parameters.

$$V_{RS} = I_{RS} R_S = 0.225 \left(\frac{GI_ADJ}{1-D}\right) \left(\frac{V_{ADJ}}{V_{REF}}\right)$$
 (Boost and Buck-boost) **Equation 5**

This shows that the sense voltage varies with duty cycle in Boost and Buck-boost configurations.



APPLICATION CIRCUIT DESIGN

External component selection is driven by the characteristics of the load and the input supply, since this will determine the kind of topology being used for the system. Component selection begins with the current setting procedure, the inductor/frequency setting and the MOSFET selection. Finally, after selecting the freewheeling diode and the output capacitor (if needed), the application section will cover the PWM dimming and thermal feedback. The full procedure is greatly accelerated by the web **Calculator** spreadsheet, which includes fully automated component selection, and is available on the Diodes website. However, the full calculation is also given here.

Please note the following particular feature of the web Calculator. The GI ratio can be set for Automatic calculation, or it can be fixed at a chosen value. When optimizing a design, it is best first to optimize for the chosen voltage range of most interest, using the Automatic setting. In order to subsequently evaluate performance of the circuit over a wider input voltage range, fix the GI ratio in the Calculator input field, and then set the desired input voltage range.

Some components depend upon the switching frequency and the duty cycle. The switching frequency is regulated by the ZXLD1371 to a large extent, depending upon conditions. This is discussed in a later paragraph dealing with coil selection.

Duty Cycle Calculation and Topology Selection

The duty cycle is a function of the input and output voltages. Approximately, the MOSFET switching duty cycle is:

$$D_{BUCK} \approx rac{V_{OUT}}{V_{IN}}$$
 for Buck

 $D_{BOOST} \approx rac{V_{OUT} \cdot V_{IN}}{V_{OUT}}$ for Boost

 $D_{BB} \approx rac{V_{OUT}}{V_{OUT} + V_{IN}}$ for Buck-Boost

Because D must always be a positive number less than 1, these equations show that:

$$\begin{array}{ll} V_{OUT} \, < \, V_{IN} & \qquad \qquad \qquad \text{for Buck (voltage step-down)} \\ V_{OUT} \, > \, V_{IN} & \qquad \qquad \qquad \text{for Boost (voltage step-up)} \\ V_{OUT} \, > \, \text{or} = \, \text{or} \, < \, V_{IN} & \qquad \qquad \text{for Buck-boost (voltage step-down or step-up)} \\ \end{array}$$

This allows us to select the topology for the required voltage range.

More exact equations are used in the web Calculator. These are:

$$\begin{split} D_{BUCK} &= \frac{V_{OUT} + V_F + I_{OUT}(R_S + R_{COIL})}{V_{IN} + V_F - V_{DSON}} & \text{for Buck} \\ D_{BOOST} &= \frac{V_{OUT} - V_{IN} + I_{IN}(R_S + R_{COIL}) + V_F}{V_{OUT} + V_F - V_{DSON}} & \text{for Boost} \\ D_{BB} &= \frac{V_{OUT} + V_F + (I_{IN} + I_{OUT})(R_S + R_{COIL})}{V_{OUT} + V_{IN} + V_F - V_{DSON}} & \text{for Buck-boost} \end{split}$$

Where: V_F = Schottky diode forward voltage, estimated for the expected coil current, I_{COIL}

V_{DSON} = MOSFET drain source voltage in the ON condition (dependent on R_{DSON} and drain current = I_{COIL})

R_{COIL} = DC winding resistance of L1



The additional terms are relatively small, so the exact equations will only make a significant difference at lower operating voltages at the input and output, i.e. low input voltage or a small number of LEDs connected in series. The estimates of V_F and V_{DSON} depend on the coil current. The mean coil current, I_{COIL} depends upon the topology and upon the mean terminal currents as follows:

$$\begin{split} I_{CO|L} &= I_{LED} & \text{for Buck} \\ I_{CO|L} &= I_{|N} & \text{for Boost} \\ I_{CO|L} &= I_{|N} + I_{LED} & \text{for Buck-boost} \end{split}$$

 I_{LED} is the target LED current and is already known. I_{IN} will be calculated with some accuracy later, but can be estimated now from the electrical power efficiency. If the expected efficiency is roughly 90%, the output power P_{OUT} is 90% of the input power, P_{IN} , and the coil current is estimated as follows.

$$\begin{array}{cc} P_{OUT} & \approx 0.9 \; P_{IN} \\ \\ \text{or} \\ & I_{LED} \; N \; V_{LED} \; \approx 0.9 \; I_{IN} \; V_{IN} \end{array}$$

where N is the number of LEDs connected in series, and V_{LED} is the forward voltage drop of a single LED at I_{LED} .

So
$$I_{IN} \approx \frac{I_{LED} N V_{LED}}{0.9 V_{IN}}$$
 Equation 9

Equation 9 can now be used to find I_{COIL} in **Equation 8**, which can then be used to estimate the small terms in **Equation 7**. This completes the calculation of Duty Cycle and the selection of Buck, Boost or Buck-boost topology.

An initial estimate of duty cycle is required before we can choose a coil. In Equation 7, the following approximations are recommended:

$$\begin{array}{lll} V_F & = 0.5V \\ I_{IN \times} (R_S + R_{COIL}) & = 0.5V \\ I_{OUT \times} (R_S + R_{COIL}) & = 0.5V \\ V_{DSON} & = 0.1V \\ (I_{IN} + I_{OUT})(R_S + R_{COIL}) & = 1.1V \\ \end{array}$$

Then Equation 7 becomes:

$$\begin{array}{ll} D_{BUCK} & \approx \frac{V_{OUT} + 1}{V_{IN} + 0.4} & \text{for Buck} \\ \\ D_{BOOST} & \approx \frac{V_{OUT} - V_{IN} + 1}{V_{OUT} + 0.4} & \text{for Boost} & \textbf{Equation 7a} \\ \\ D_{BB} & \approx \frac{V_{OUT} + 1.6}{V_{OUT} + V_{IN} + 0.4} & \text{for Buck-boost} \end{array}$$

Setting the LED Current

The LED current requirement determines the choice of the sense resistor Rs. This also depends on the voltage on the ADJ pin and the voltage on the GI pin, according to the topology required.

The ADJ pin may be connected directly to the internal 1.25V reference (V_{REF}) to define the nominal 100% LED current. The ADJ pin can also be driven with an external DC voltage between 125mV and 1.25V to adjust the LED current proportionally between 10% and 100% of the nominal value.

For a divider ratio GI_ADJ greater than 0.65V, the ZXLD1371 operates in Buck mode when $V_{ADJ} = 1.25V$. If GI_ADJ is less than 0.65V (typical), the device operates in Boost or Buck-boost mode, according to the load connection. This 0.65V threshold varies in proportion to V_{ADJ} , i.e., the Buck mode threshold voltage is 0.65 V_{ADJ} /1.25 V.

ADJ and GI are high-impedance inputs within their normal operating voltage ranges. An internal 1.3V clamp protects the device against excessive input voltage and limits the maximum output current to approximately 4% above the maximum current set by V_{REF} if the maximum input voltage is exceeded.



Buck topology

In Buck mode, GI is connected to ADJ as in **Figure 5**. The LED current depends only upon R_S , V_{ADJ} and V_{REF} . From **Equation 1** above,

$$R_{SBuck} = \left(\frac{0.218}{I_{LED}}\right) \left(\frac{V_{ADJ}}{V_{REF}}\right)$$
 Equation 10

If ADJ is directly connected to VREF, this becomes:

$$R_{SBuck} = \left(\frac{0.218}{I_{LED}}\right)$$

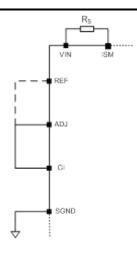


Figure 5. Setting LED current in Buck configuration

Boost and Buck-boost topology

For Boost and Buck-boost topologies, the LED current depends upon the resistors, R_{S} , R_{GI1} , and R_{GI2} as in **Equations 4** and **2** above. There is more than one degree of freedom. That is to say, there is not a unique solution. From **Equation 4**,

$$R_{SBoostBB} = \left(\frac{0.225}{I_{LED}}\right) GI_ADJ \left(\frac{V_{ADJ}}{V_{REF}}\right)$$
 Equation 11

If ADJ is connected to REF, this becomes:

$$R_{SBoostBB} = \left(\frac{0.225}{I_{LED}}\right) GI_ADJ$$

GI_ADJ is given by Equation 2, repeated here for convenience:

$$GI_ADJ = \left(\frac{RGI1}{RGI1 + RGI2}\right)$$

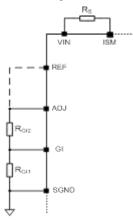


Figure 6. Setting LED current in Boost and Buck-boost configurations

Note that from considerations of ZXLD1371 input bias current, the recommended limits for R_{GI1} are:

$$22k\Omega$$
 < R_{GI1} < $100k\Omega$ Equation 12

The additional degree of freedom allows us to select GI_ADJ within limits but this may affect overall performance a little. As mentioned above, the working voltage range at the GI pin is restricted. The permitted range of GI_ADJ in Boost or Buck-boost configuration is:

$$0.2 < GI ADJ < 0.5$$
 Equation 13

The mean voltage across the sense resistor is:

$$V_{RS} = I_{COIL} R_S$$
 Equation 14

Note that if GI_ADJ is made larger, these equations show that R_S is increased and V_{RS} is increased. Therefore, for the same coil current, the dissipation in R_S is increased. So, in some cases, it is better to minimize GI_ADJ . However, consider **Equation 5**. If ADJ is connected to REF, this becomes

$$V_{RS} = 0.225 \left(\frac{GI_ADJ}{1-D} \right)$$

This shows that V_{RS} becomes smaller than 225mV if GI_ADJ < 1 - D. If also D is small, V_{RS} can become too small. For example if D = 0.2, and GI_ADJ is the minimum value of 0.2, then V_{RS} becomes 0.225* 0.2 / 0.8 = 56.25 mV. This will increase the LED current error due to small offsets in the system, such as mV drop in the copper printed wiring circuit, or offset uncertainty in the ZXLD1371. If now, GI_ADJ is increased to 0.4 or 0.5, V_{RS} is increased to a value greater than 100mV.

ZXLD1371 25 of 43 February 2017

Document number: DS35436 Rev. 2 - 2 www.diodes.com © Diodes Incorporated