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ZY7007 7A DC-DC Intelligent POL Data Sheet
3V to 14V Input • 0.5V to 5.5V Output

power-one® Changing the Shape of Power

Member of the maXyz Family

RoHS Compliant

Applications

- Low voltage, high density systems with Intermediate Bus Architectures (IBA)
- Point-of-load regulators for high performance DSP, FPGA, ASIC, and microprocessor applications
- Desktops, servers, and portable computing
- Broadband, networking, optical, and communications systems
- Active memory bus terminators

Benefits

- Integrates digital power conversion with intelligent power management
- Eliminates the need for external power management components
- Completely programmable via industry-standard I^2C communication bus
- One part that covers all applications
- Reduces board space, system cost and complexity, and time to market

Features

- RoHS lead free and lead-solder-exempt products are available
- Wide input voltage range: 3V–14V
- High continuous output current: 7A
- Wide programmable output voltage range: 0.5V–5.5V
- Active digital current share
- Single-wire serial communication bus for frequency synchronization, programming, and monitoring
- Optimal voltage positioning with programmable slope of the VI line
- Overcurrent, overvoltage, undervoltage, and overtemperature protection with programmable thresholds and types
- Programmable fixed switching frequency 0.5-1.0MHz
- Programmable turn-on and turn-off delays
- Programmable turn-on and turn-off voltage slew rates with tracking protection
- Programmable feedback loop compensation
- Power Good signal with programmable limits
- Programmable fault management
- Start up into the load pre-biased up to 100%
- Full rated current sink
- Real time voltage, current, and temperature measurements, monitoring, and reporting
- Small footprint SMT package: 12.5x22.2mm
- Extremely low profile of 6.5mm
- Compatible with conventional pick-and-place equipment
- Wide operating temperature range
- UL 60950-1/CSA 22.2 No. 60950-1-07 Second Edition, IEC 60950-1: 2005, and EN 60950-1:2006

Description

Power-One's point-of-load converters are recommended for use with regulated bus converters in an Intermediate Bus Architecture (IBA). The ZY7007 is an intelligent, fully programmable step-down point-of-load DC-DC module integrating digital power conversion and intelligent power management. When used with ZM7300 Series Digital Power Managers, the ZY7007 completely eliminates the need for external components for sequencing, tracking, protection, monitoring, and reporting. All parameters of the ZY7007 are programmable via the industry-standard I^2C communication bus and can be changed by a user at any time during product development and service.

Reference Documents:

- ZM7300 Digital Power Manager Data Sheet
- ZM7300 PrgManual - Digital Power Manager Programming Manual
- Power-One I2C GEN II Graphical User Interface
- ZM00056-KIT USB to I^{2}C Adapter Kit. User Manual

1. Ordering Information

ZY	70	07	x	y	–	zz
Product family: Z-One Module	**Series:** Intelligent POL Converter	**Output Current:** 7A	**Output voltage setpoint accuracy:** **L** – 1.2% or 20mV, whichever is greater. **H**[1] – 1.0% or 10mV, whichever is greater	**RoHS compliance:** **No suffix** - RoHS compliant with Pb solder exemption[2] **G** - RoHS compliant for all six substances	**Dash**	**Packaging Option**[3]**:** **T1** - 500pcs T&R **T2** – 100pcs T&R **T3** – 50pcs T&R **Q1** – 1pc sample for evaluation only

[1] Contact factory for availability.
[2] The solder exemption refers to all the restricted materials except lead in solder. These materials are Cadmium (Cd), Hexavalent chromium (Cr6+), Mercury (Hg), Polybrominated biphenyls (PBB), Polybrominated diphenylethers (PBDE), and Lead (Pb) used anywhere except in solder.
[3] Packaging option is used only for ordering and not included in the part number printed on the POL converter label.
[4] The evaluation board is available in only one configuration: ZM7300-KIT-HKS.

Example: **ZY7007HG-T2**: A 100-piece reel of RoHS compliant POL converters with the output voltage setpoint of 1.0% or 10mV, whichever is greater. Each POL converter is labeled ZY7007HG.

2. Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings may cause performance degradation, adversely affect long-term reliability, and cause permanent damage to the converter.

Parameter	Conditions/Description	Min	Max	Units
Operating Temperature	Controller case temperature	-40	105	°C
Input Voltage	250ms Transient		15	VDC
Output Current	(See Output Current De-rating Curves)	-7	7	ADC

3. Environmental and Mechanical Specifications

Parameter	Conditions/Description	Min	Nom	Max	Units
Ambient Temperature Range		-40		85	°C
Storage Temperature (Ts)		-55		125	°C
Weight				8	grams
MTBF	Calculated Per Telcordia Technologies SR-332	6.24			MHrs
Peak Reflow Temperature	ZY7007 ZY7007G		 245	220 260	°C °C
Lead Plating	ZY7007 and ZY7007G	100% Matte Tin			
Moisture Sensitivity Level	ZY7007 and ZY7007G	3			

4. Electrical Specifications

Specifications apply at the input voltage from 3V to 14V, output load from 0 to 7A, ambient temperature from -40°C to 85°C, 100µF output capacitance, and default performance parameters settings unless otherwise noted.

4.1 Input Specifications

Parameter	Conditions/Description	Min	Nom	Max	Units
Input voltage (V_{IN})	At V_{IN}<4.75V, VLDO pin needs to be connected to an external voltage source higher than 4.75V	3		14	VDC
Input Current (at no load)	V_{IN}≥4.75V, VLDO pin connected to VIN		50		mADC
Undervoltage Lockout (VLDO connected to VIN)	Ramping Up Ramping Down		4.2 3.75		VDC VDC
Undervoltage Lockout (VLDO connected to V_{AUX}=5V)	Ramping Up Ramping Down		3.0 2.5		VDC VDC
External Low Voltage Supply	Connect to VLDO pin when V_{IN}<4.75V	4.75		14	VDC
VLDO Input Current	Current drawn from the external low voltage supply at VLDO=5V		50		mADC

4.2 Output Specifications

Parameter	Conditions/Description	Min	Nom	Max	Units
Output Voltage Range (V_{OUT})	Programmable[1] Default (no programming)	0.5	 0.5	5.5	VDC VDC
Output Voltage Setpoint Accuracy	V_{IN}=12V, I_{OUT}=0.5*$I_{OUT\ MAX}$, F_{SW}=500kHz, room temperature	(See Ordering Information)			
Output Current (I_{OUT})	$V_{IN\ MIN}$ to $V_{IN\ MAX}$	-7[2]		7	ADC
Line Regulation	$V_{IN\ MIN}$ to $V_{IN\ MAX}$		±0.3		%V_{OUT}
Load Regulation	0 to $I_{OUT\ MAX}$		±0.3		%V_{OUT}
Dynamic Regulation Peak Deviation Settling Time	Slew rate 2.5A/µs, 50 - 100% load step C_{OUT}=220µF, F_{SW}=1MHz to 10% of peak deviation		 50 50		 mV µs
Output Voltage Peak-to-Peak Ripple and Noise BW=20MHz Full Load	V_{IN}=5.0V, V_{OUT}=0.5V, F_{SW}=500kHz V_{IN}=5.0V, V_{OUT}=2.5V, F_{SW}=500kHz V_{IN}=13.2V, V_{OUT}=0.5V, F_{SW}=500kHz V_{IN}=13.2V, V_{OUT}=2.5V, F_{SW}=500kHz V_{IN}=13.2V, V_{OUT}=5.0V, F_{SW}=500kHz V_{IN}=13.2V, V_{OUT}=5.0V, F_{SW}=1MHz		15 15 20 25 40 20		mV mV mV mV mV mV
Temperature Coefficient	V_{IN}=12V, I_{OUT}=0.5*$I_{OUT\ MAX}$		20		ppm/°C
Switching Frequency	Default Programmable, 250kHz steps	 500	500	 1,000	kHz kHz
Duty Cycle Limit	Default Programmable, 1.56% steps	 0	90.5	 95	% %

[1] ZY7007 is a step-down converter, thus the output voltage is always lower than the input voltage as show in Figure 1.
[2] At the negative output current (bus terminator mode) efficiency of the ZY7007 degrades resulting in increased internal power dissipation. Therefore maximum allowable negative current under specific conditions is 20% lower than the current determined from the derating curves shown in paragraph 5.5.

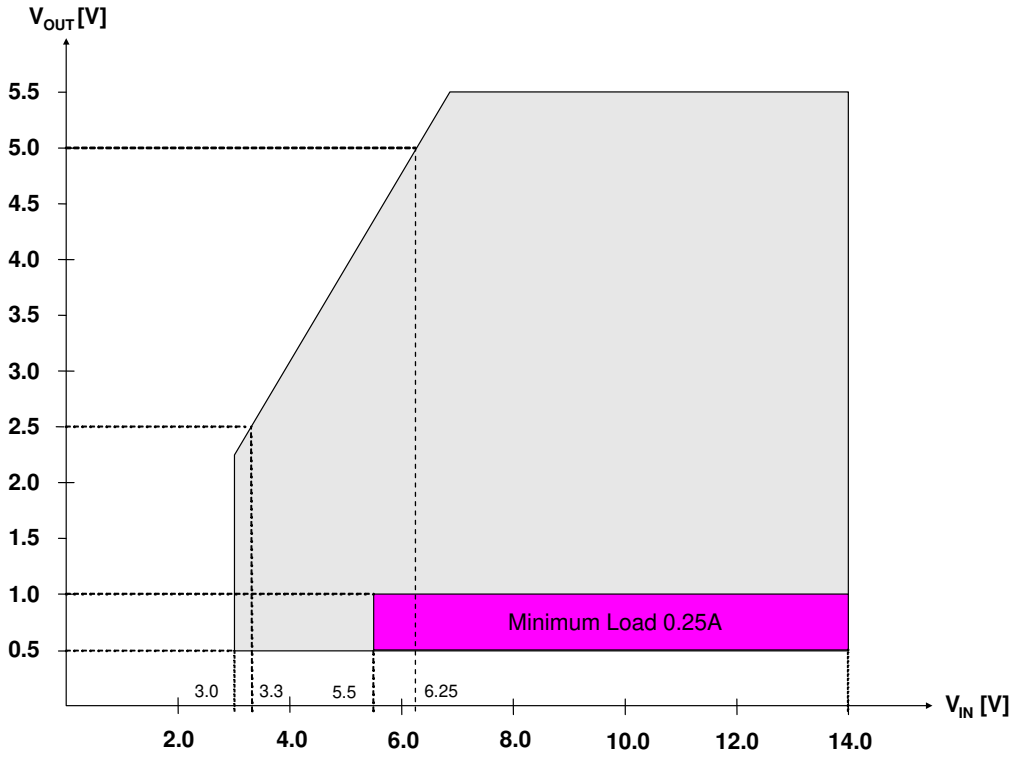

Figure 1. Output Voltage as a Function of Input Voltage and Output Current

4.3 Protection Specifications

Parameter	Conditions/Description	Min	Nom	Max	Units
Output Overcurrent Protection					
Type	Default Programmable	Non-Latching, 130ms period Latching/Non-Latching			
Threshold	Default Programmable in 11 steps	60	180	180	$\%I_{OUT}$ $\%I_{OUT}$
Threshold Accuracy		-25		25	$\%I_{OCP.SET}$
Output Overvoltage Protection					
Type	Default Programmable	Non-Latching, 130ms period Latching/Non-Latching			
Threshold	Default Programmable in 10% steps	110[1]	130	130	$\%V_{O.SET}$ $\%V_{O.SET}$
Threshold Accuracy	Measured at $V_{O.SET}$=2.5V	-2		2	$\%V_{OVP.SET}$
Delay	From instant when threshold is exceeded until the turn-off command is generated		6		µs

[1] Minimum OVP threshold is 1.0V

Output Undervoltage Protection					
Type	Default Programmable	Non-Latching, 130ms period Latching/Non-Latching			
Threshold	Default Programmable in 5% steps	75	75	85	$\%V_{O.SET}$ $\%V_{O.SET}$
Threshold Accuracy	Measured at $V_{O.SET}$=2.5V	-2		2	$\%V_{UVP.SET}$
Delay	From instant when threshold is exceeded until the turn-off command is generated		6		µs
Over Temperature Protection					
Type	Default Programmable	Non-Latching, 130ms period Latching/Non-Latching			
Turn Off Threshold	Temperature is increasing		130		°C
Turn On Threshold	Temperature is decreasing after the module was shut down by OTP		120		°C
Threshold Accuracy		-5		5	°C
Delay	From instant when threshold is exceeded until the turn-off command is generated		6		µs
Tracking Protection (when Enabled)					
Type	Default Programmable	Disabled Latching/Non-Latching, 130ms period			
Threshold	Enabled during output voltage ramping up			±250	mVDC
Threshold Accuracy		-50		50	mVDC
Delay	From instant when threshold is exceeded until the turn-off command is generated		6		µs
Over Temperature Warning					
Threshold	Always enabled, reported in Status register		120		°C
Threshold Accuracy		-5		5	°C
Hysteresis			3		°C
Delay	From instant when threshold is exceeded until the warning signal is generated		6		µs
Power Good Signal (PGOOD pin)					
Logic	V_{OUT} is inside the PG window V_{OUT} is outside the PG window	High Low			N/A
Lower Threshold	Default Programmable in 5% steps	90	90	95	$\%V_{O.SET}$ $\%V_{O.SET}$
Upper Threshold			110		$\%V_{O.SET}$
Delay	From instant when threshold is exceeded until status of PG signal changes		6		µs
Threshold Accuracy	Measured at $V_{O.SET}$=2.5V	-2		2	$\%V_{O.SET}$

4.4 Feature Specifications

Parameter	Conditions/Description	Min	Nom	Max	Units
Current Share					
Type		Active, Single Line			
Maximum Number of Modules Connected in Parallel	$I_{OUT\ MIN}$=0	4			
Current Share Accuracy	$I_{OUT\ MIN}$≥20%*$I_{OUT\ NOM}$			±20	%I_{OUT}
Interleave					
Interleave (Phase Shift)	Default Programmable in 11.25° steps	0	0	348.75	Degree degree
Sequencing					
Turn ON Delay	Default Programmable in 1ms steps	0	0	255	ms ms
Turn OFF Delay	Default Programmable in 1ms steps	0	0	63	ms ms
Tracking					
Turn ON Slew Rate	Default Programmable in 7 steps	0.1	0.1	8.33[1]	V/ms V/ms
Turn OFF Slew Rate	Default Programmable in 7 steps	-0.1	-0.1	-8.33[1]	V/ms V/ms
Optimal Voltage Positioning					
Load Regulation	Default Programmable in 7 steps	0	0	13	mV/A mV/A
Feedback Loop Compensation					
Zero1 (Effects phase lead and increases gain in mid-band)	Programmable	0.05		50	kHz
Zero 2 (Effects phase lead and increases gain in mid-band)	Programmable	0.05		50	kHz
Pole 1 (Integrator Pole, effects loop gain)	Programmable	0.05		50	kHz
Pole 2 (Effects phase lag and limits gain in mid-band)	Programmable	1		1000	kHz
Pole 3 (High frequency low- pass filter to limit PWM noise)	Programmable	1		1000	kHz
Monitoring					
Voltage Monitoring Accuracy	1 LSB=22mV	-2%V_{OUT} – 1 LSB		2%V_{OUT} + 1 LSB	mV
Current Monitoring Accuracy	20%*$I_{OUT\ NOM}$ < I_{OUT} < $I_{OUT\ NOM}$	-20		+20	%I_{OUT}
Temperature Monitoring Accuracy	Junction temperature of POL controller	-5		+5	°C
Remote Voltage Sense (+VS and –VS pins)					
Voltage Drop Compensation	Between +VS and VOUT			300	mV
Voltage Drop Compensation	Between -VS and PGND			100	mV

[1] Achieving fast slew rates under specific line and load conditions may require feedback loop adjustment

4.5 Signal Specifications

Parameter	Conditions/Description	Min	Nom	Max	Units
VDD	Internal supply voltage	3.15	3.3	3.45	V
SYNC/DATA Line (SD pin)					
ViL_sd	LOW level input voltage	-0.5		0.3 x VDD	V
ViH_sd	HIGH level input voltage	0.75 x VDD		VDD + 0.5	V
Vhyst_sd	Hysteresis of input Schmitt trigger	0.25 x VDD		0.45 x VDD	V
VoL	LOW level sink current @ 0.5V	14		60	mA
Tr_sd	Maximum allowed rise time 10/90%VDD			300	ns
Cnode_sd	Added node capacitance		5	10	pF
Ipu_sd	Pull-up current source at Vsd=0V	0.3		1.0	mA
Freq_sd	Clock frequency of external SD line	475		525	kHz
Tsynq	Sync pulse duration	22		28	% of clock cycle
T0	Data=0 pulse duration	72		78	% of clock cycle
Inputs: ADDR0…ADDR4, EN, IM					
ViL_x	LOW level input voltage	-0.5		0.3 x VDD	V
ViH_x	HIGH level input voltage	0.7 x VDD		VDD+0.5	V
Vhyst_x	Hysteresis of input Schmitt trigger	0.1 x VDD		0.3 x VDD	V
RdnL_ADDR	External pull down resistance ADDRX forced low			10	kOhm
Power Good and OK Inputs/Outputs					
Iup_PG	Pull-up current source input forced low PG	25		110	µA
Iup_OK	Pull-up current source input forced low OK	175		725	µA
ViL_x	LOW level input voltage	-0.5		0.3 x VDD	V
ViH_x	HIGH level input voltage	0.7 x VDD		VDD+0.5	V
Vhyst_x	Hysteresis of input Schmitt trigger	0.1 x VDD		0.3 x VDD	V
IoL	LOW level sink current at 0.5V	4		20	mA
Current Share Bus (CS pin)					
Iup_CS	Pull-up current source at VCS = 0V	0.84		3.1	mA
ViL_CS	LOW level input voltage	-0.5		0.3 x VDD	V
ViH_CS	HIGH level input voltage	0.75 x VDD		VDD+0.5	V
Vhyst_CS	Hysteresis of input Schmitt trigger	0.25 x VDD		0.45 x VDD	V
IoL	LOW level sink current at 0.5V	14		60	mA
Tr_CS	Maximum allowed rise time 10/90% VDD			100	ns

5. Typical Performance Characteristics

5.1 Efficiency Curves

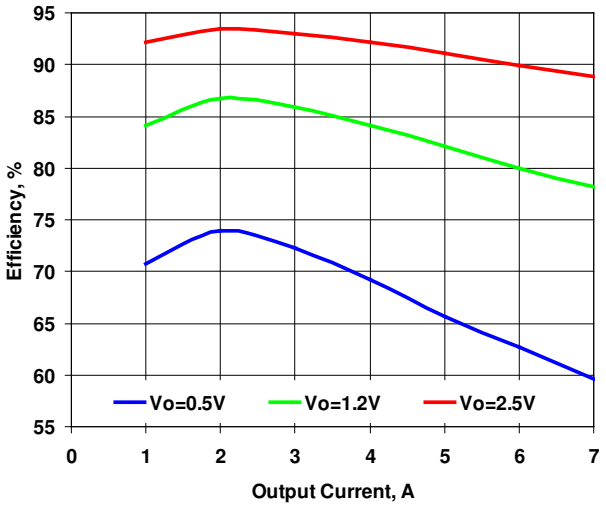

Figure 2. Efficiency vs. Load. Vin=3.3V, Fsw=500kHz

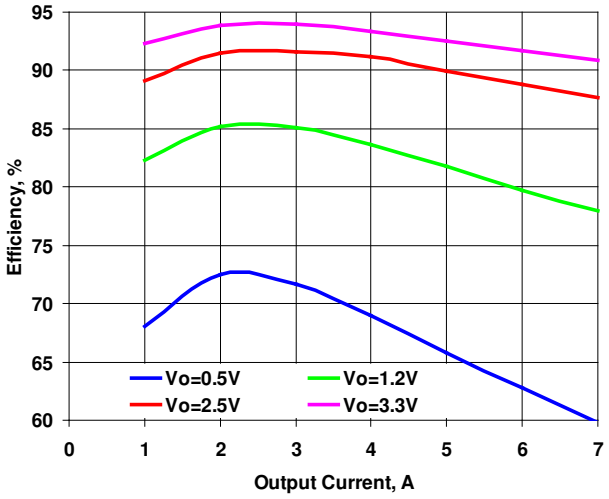

Figure 3. Efficiency vs. Load. Vin=5V, Fsw=500kHz

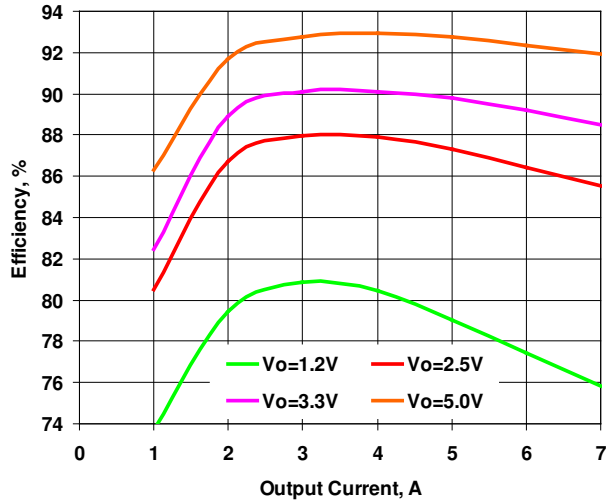

Figure 4. Efficiency vs. Load. Vin=9.6V, Fsw=500kHz

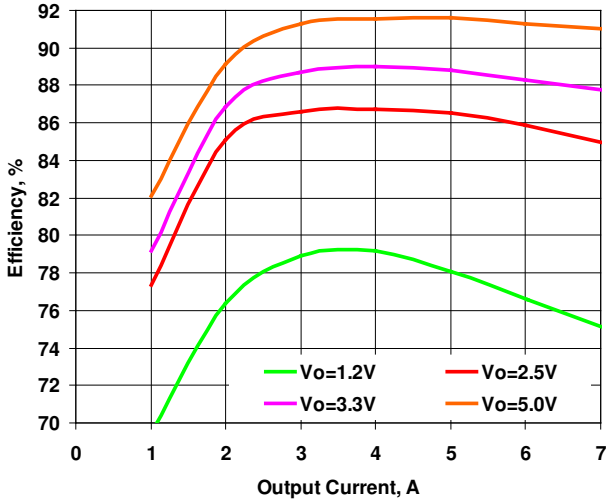

Figure 5. Efficiency vs. Load. Vin=12V, Fsw=500kHz

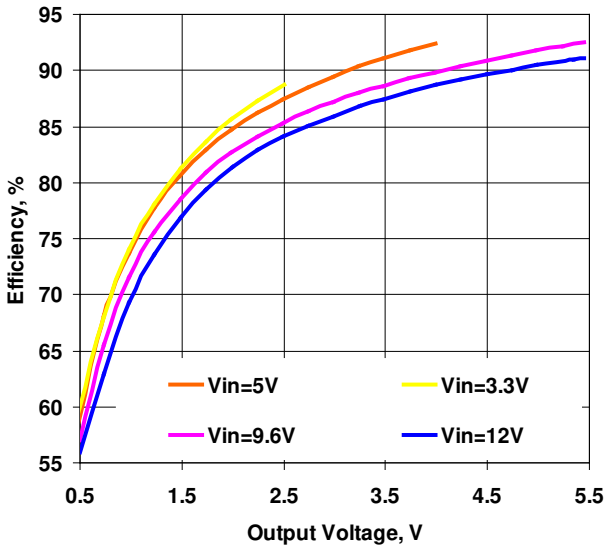

Figure 6. Efficiency vs. Output Voltage, Iout=7A, Fsw=500kHz

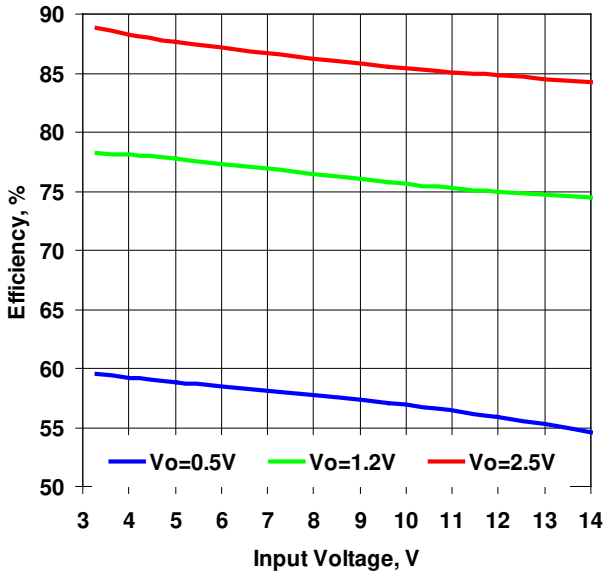

Figure 7. Efficiency vs. Input Voltage. Iout=7A, Fsw=500kHz

5.2 Turn-On Characteristics

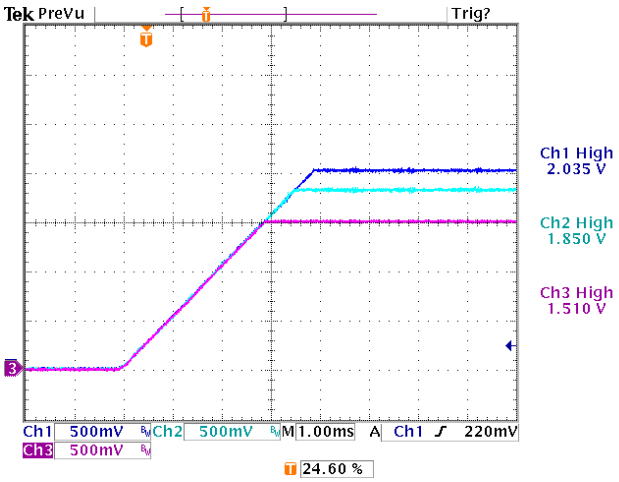

Figure 8. Tracking Turn-On. Rising Slew Rate is Programmed at 0.5V/ms.
Vin=12V, Ch1 – V1, Ch2 – V2, Ch3 – V3

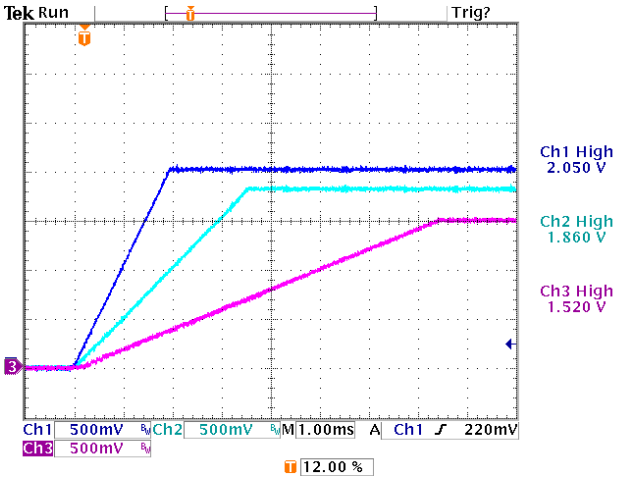

Figure 9. Turn-On with Different Rising Slew Rates.
Rising Slew Rates are Programmed as follows: V1-1V/ms, V2-0.5V/ms, V3-0.2V/ms.
Vin=12V, Ch1 – V1, Ch2 – V2, Ch3 – V3

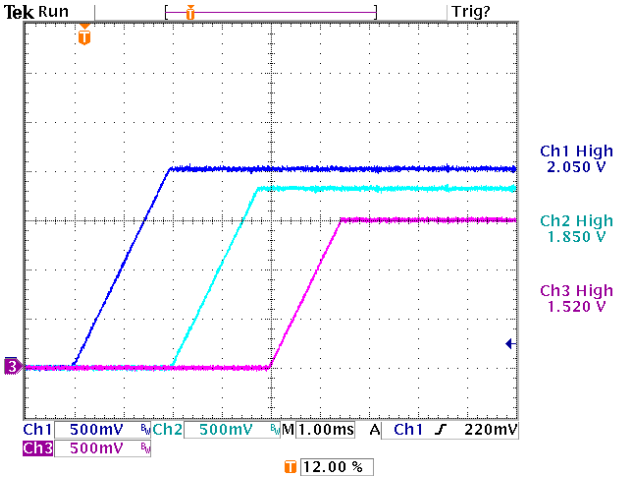

Figure 10. Sequenced Turn-On. Rising Slew Rate is Programmed at 1V/ms. V2 Delay is 2ms, V3 delay is 4ms. Vin=12V, Ch1 – V1, Ch2 – V2, Ch3 – V3

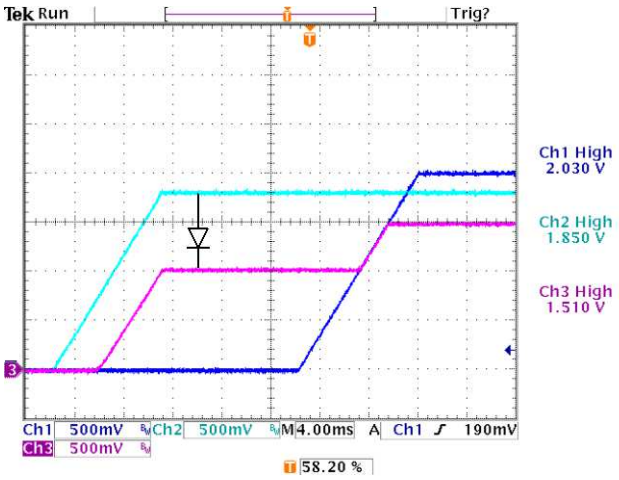

**Figure 11. Turn On into Prebiased Load. V3 is Prebiased by V2 via a Diode.
Vin=12V, Ch1 – V1, Ch2 – V2, Ch3 – V3**

5.3 Turn-Off Characteristics

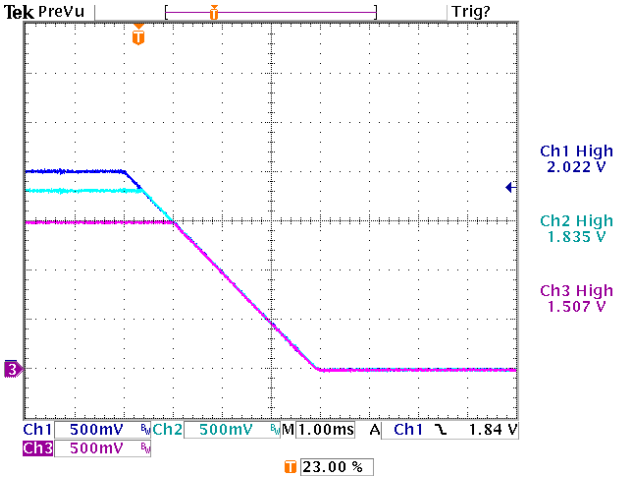

**Figure 12. Tracking Turn-Off. Falling Slew Rate is Programmed at 0.5V/ms.
Vin=12V, Ch1 – V1, Ch2 – V2, Ch3 – V3**

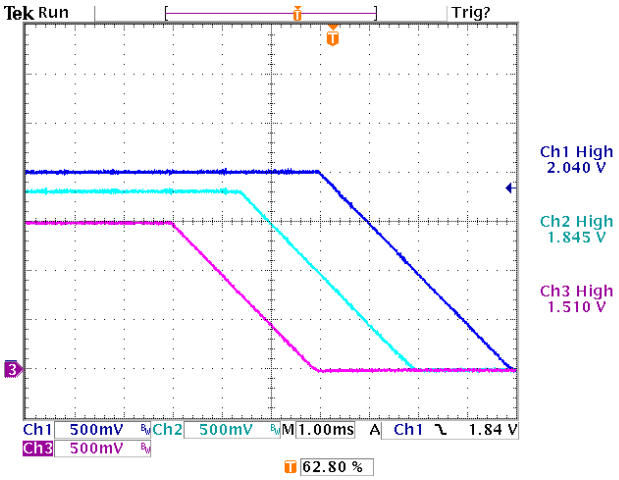

**Figure 13. Turn-Off with Tracking and Sequencing. Falling Slew Rate is Programmed at 0.5V/ms.
Vin=12V, Ch1 – V1, Ch2 – V2, Ch3 – V3**

5.4 Transient Response

The pictures below show the deviation of the output voltage in response to the 50-100-50% step load at 2.5A/µs. In all tests the POL converters were switching at 1MHz and had 10 x 22µF ceramic capacitors connected across the output pins. Bandwidth of the feedback loop was programmed for faster transient response.

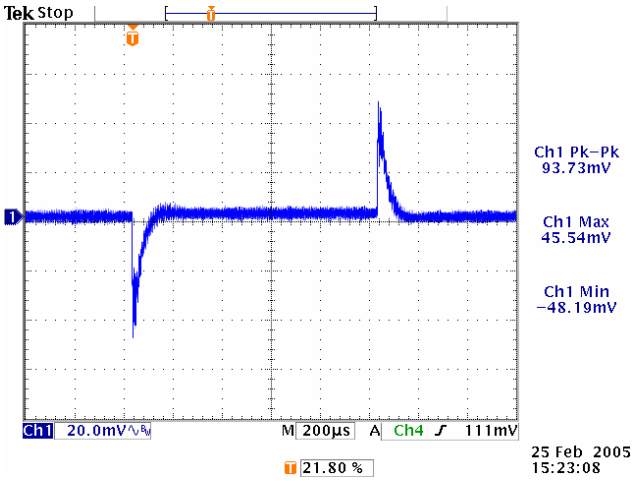

Figure 14. Vin=12V, Vout=5V, BW~50kHz

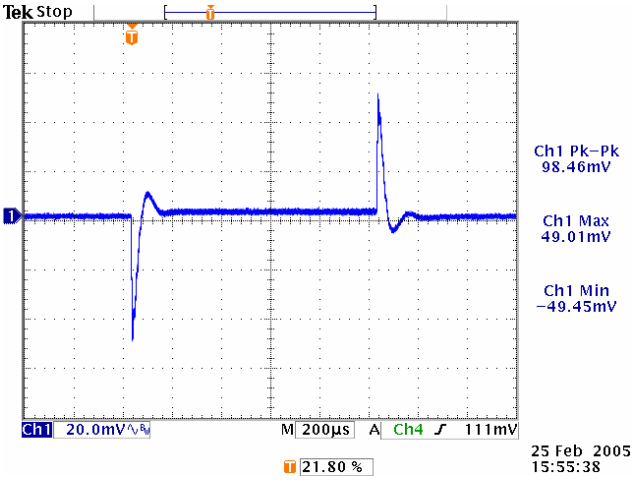

Figure 15. Vin=12V, Vout=1V, BW~40kHz

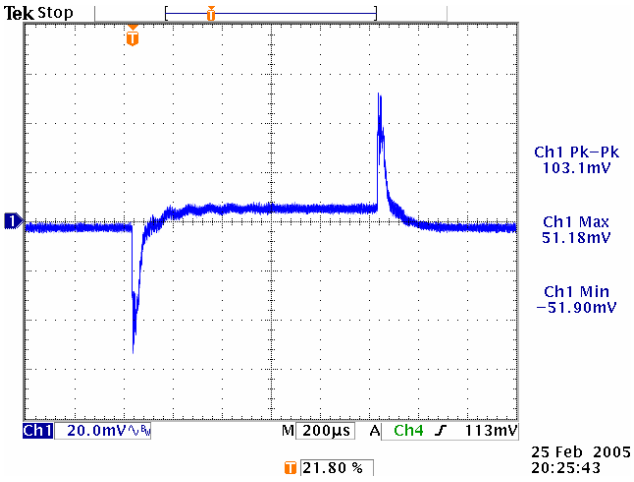

Figure 16. Vin=5V, Vout=2.5V, BW~40kHz

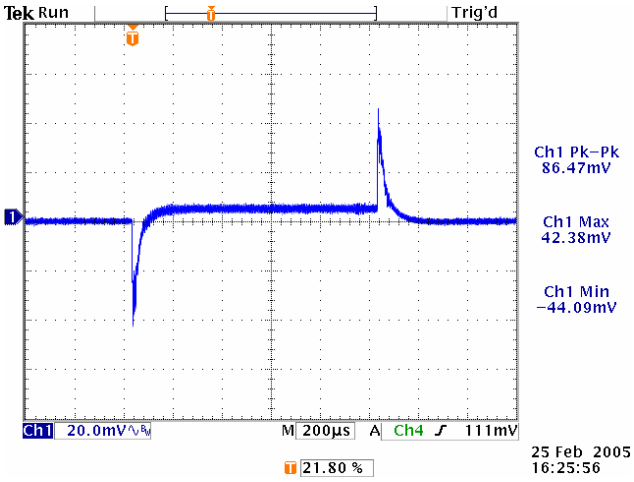

Figure 17. Vin=5V, Vout=1V, BW~40kHz

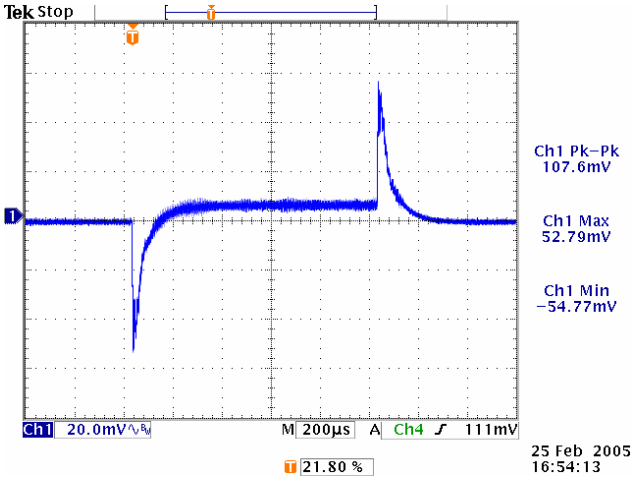

Figure 18. Vin=3.3V, Vout=1V, BW~40kHz

5.5 Thermal De-rating Curves

Figure 19. Thermal Derating Curves. Vin=12V, Vout=5.0V, Fsw=500kHz

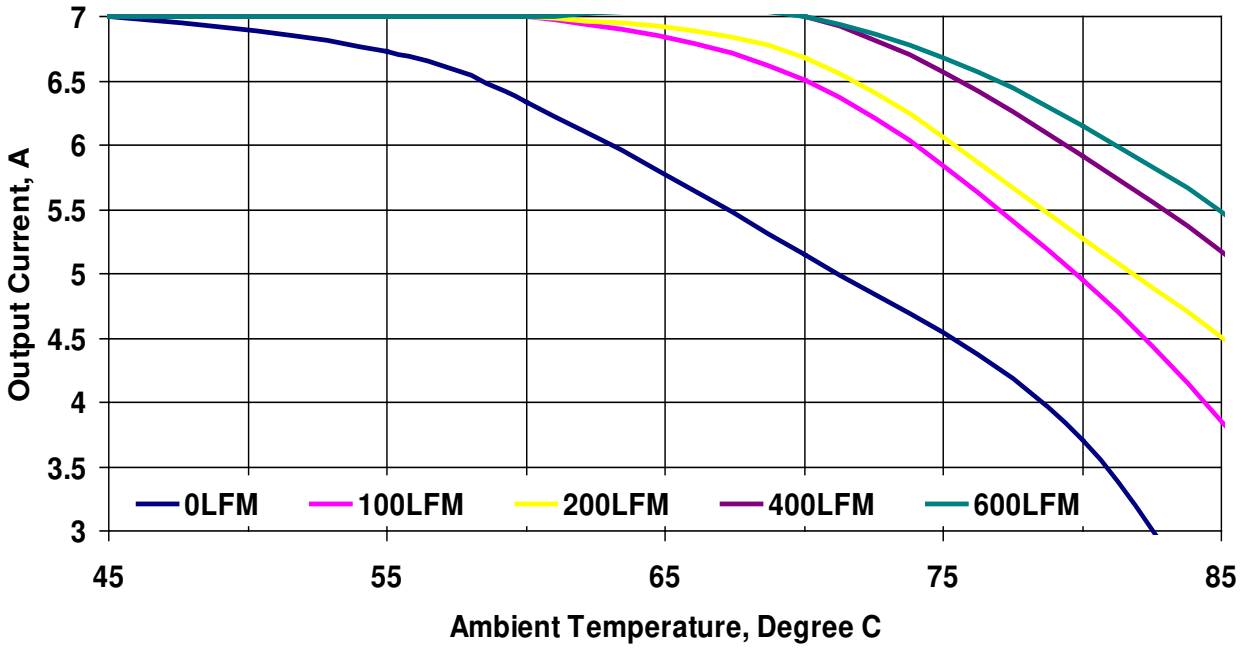

Figure 20. Thermal Derating Curves. Vin=14V, Vout=5.0V, Fsw=500kHz

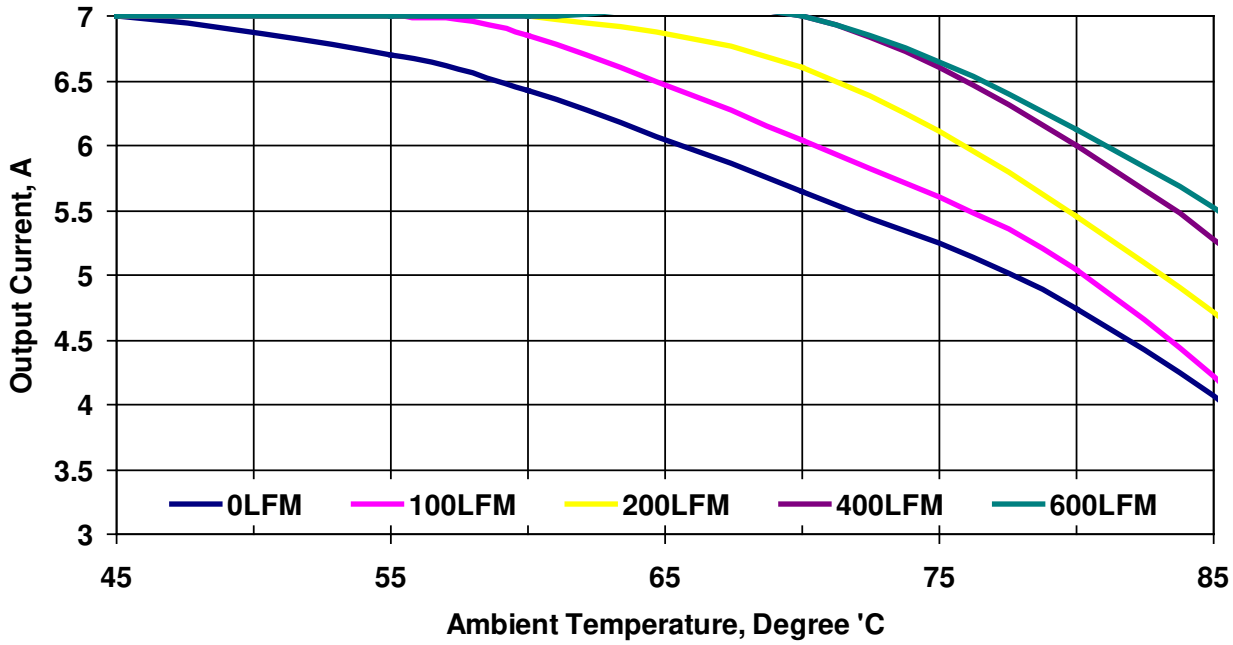

Figure 21. Thermal Derating Curves. Vin=12V, Vout=5.0V, Fsw=1MHz

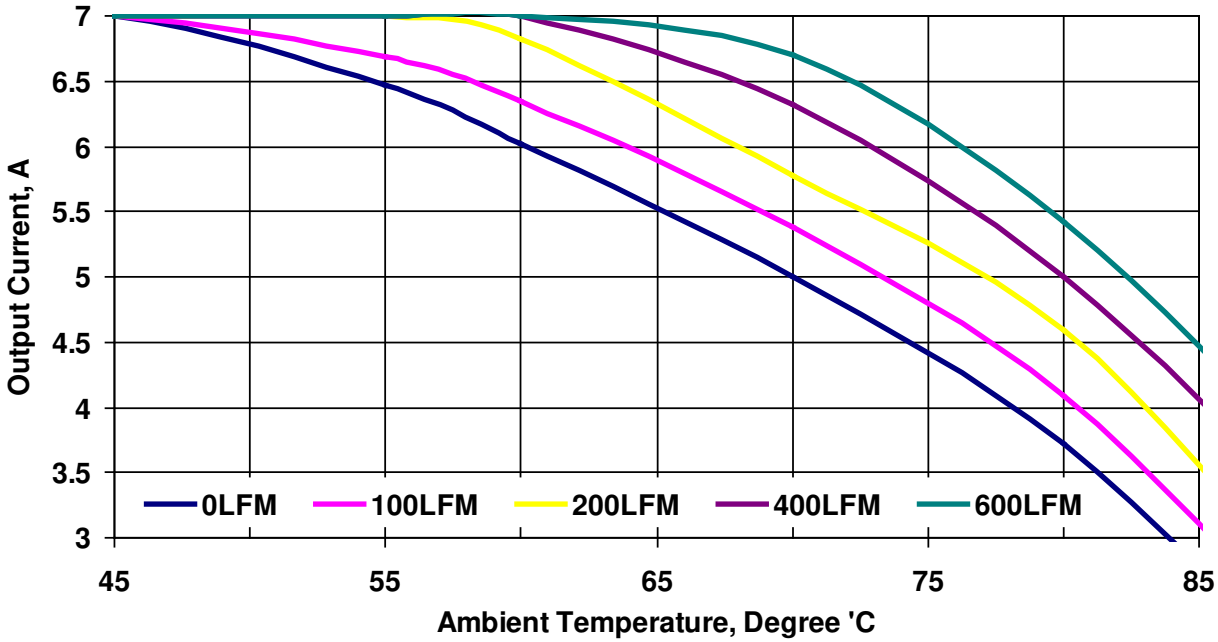

Figure 22. Thermal Derating Curves. Vin=14V, Vout=5.0V, Fsw=1MHz

6. Typical Application

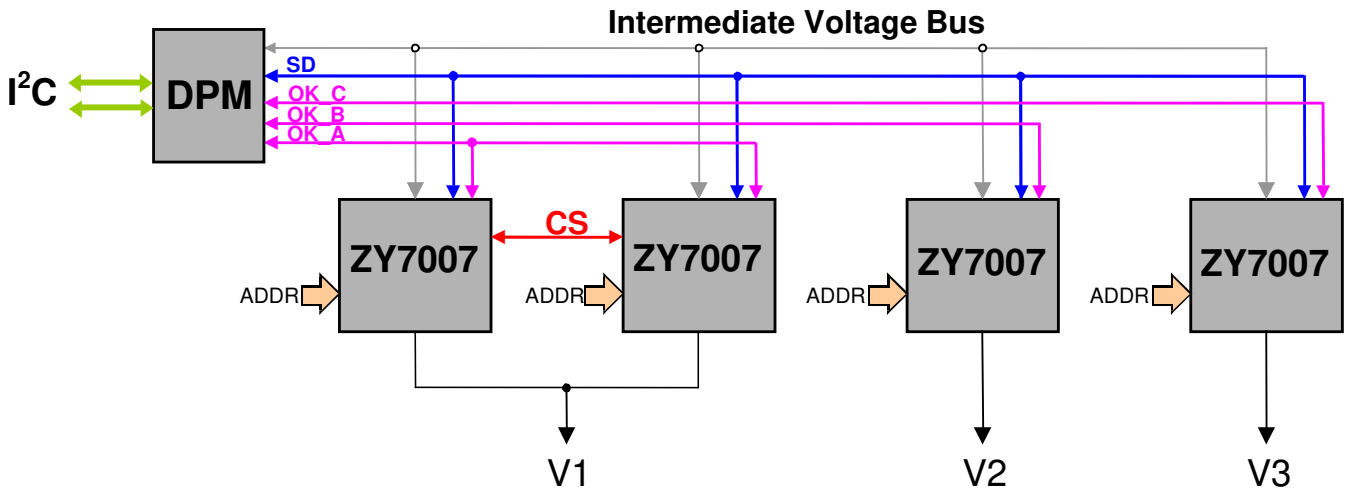

Figure 23. Block Diagram of Typical Multiple Output Application with Digital Power Manager and I²C Interface

The block diagram of a typical application of ZY7007 point-of-load converters (POL) is shown in Figure 23. The system includes multiple POLs and a ZM7300 series Digital Power Manager (DPM). All POLs are connected to the DPM and to each other via a single-wire SD (sync/data) line. The line provides synchronization of all POLs to the master clock generated by the DPM and simultaneously performs bidirectional data transfer between POLs and the DPM. Each POL has a unique 5-bit address programmed by grounding respective address pins. To enable the current share, CS pins of POLs connected in parallel are linked together.

There are three groups of POLs in the application, groups A, B, and group C. A group is defined as a number of POLs interconnected via OK pins. Grouping of POLs enables users to program, control, and monitor multiple POLs simultaneously and execute advanced fault management schemes.

The complete schematic of the application is shown in Figure 24.

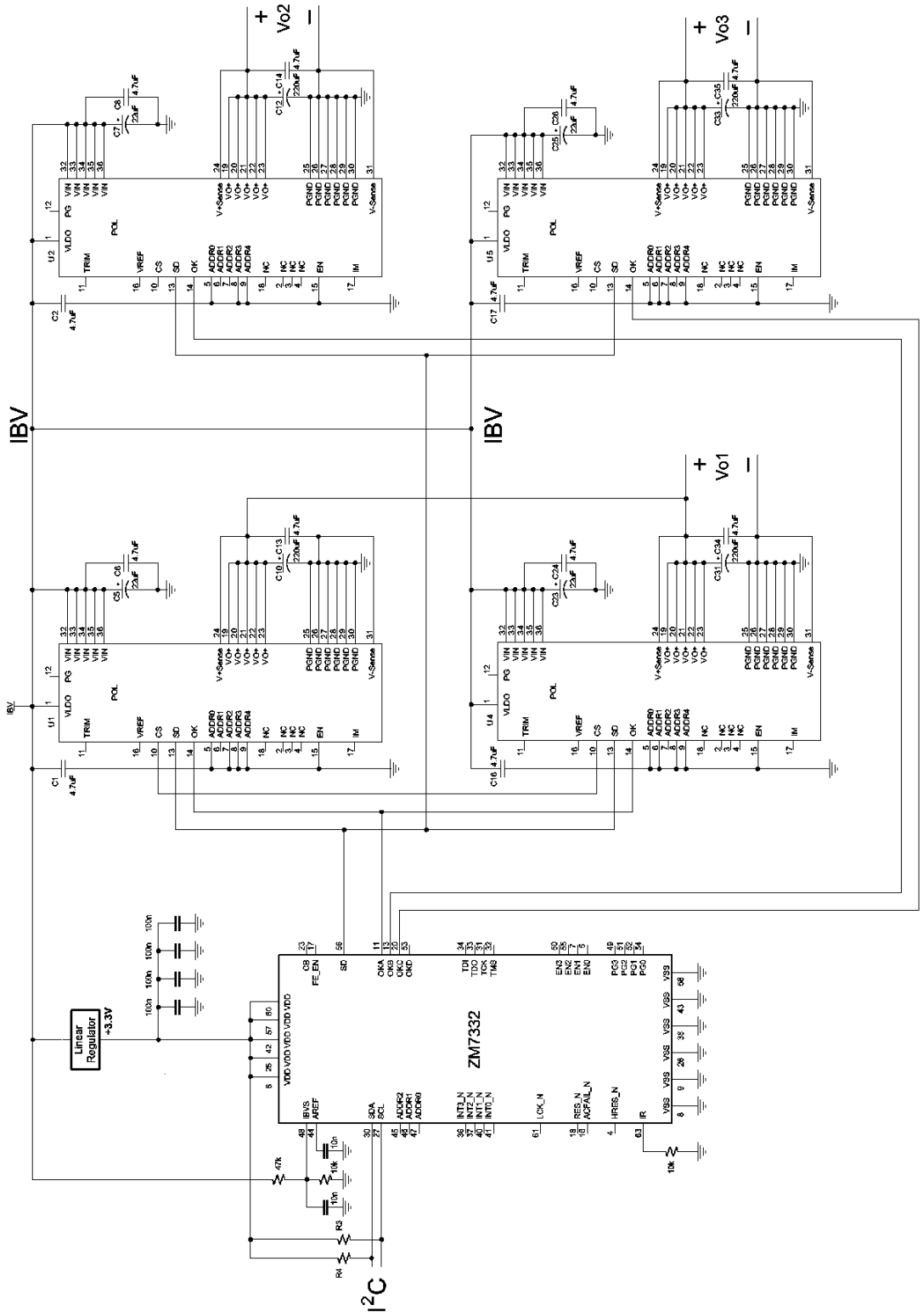

Figure 24. Complete Schematic of the Application Shown in Figure 23. Intermediate Bus Voltage is from 4.75V to 13.2V.

7. Pin Assignments and Descriptions

Pin Name	Pin Number	Pin Type	Buffer Type	Pin Description	Notes
VLDO	1	P		Low Voltage Dropout	Connect to an external voltage source higher than 4.75V, if V_{IN}<4.75V. Connect to V_{IN}, if V_{IN}≥4.75V
NC	2			Not Used	Leave floating
NC	3			Not Used	Leave floating
NC	4			Not Used	Leave floating
ADDR0	5	I	PU	POL Address Bit 0	Tie to PGND for 0 or leave floating for 1
ADDR1	6	I	PU	POL Address Bit 1	Tie to PGND for 0 or leave floating for 1
ADDR2	7	I	PU	POL Address Bit 2	Tie to PGND for 0 or leave floating for 1
ADDR3	8	I	PU	POL Address Bit 3	Tie to PGND for 0 or leave floating for 1
ADDR4	9	I	PU	POL Address Bit 4	Tie to PGND for 0 or leave floating for 1
CS	10	I/O	PU	Current Share	Connect to CS pins of other Z-POLs connected in parallel
TRIM	11			Not Used	Leave floating
PGOOD	12	I/O	PU	Power Good	
SD	13	I/O	PU	Sync/Data Line	Connect to SD pin of DPM
OK	14	I/O	PU	Fault/Status Condition	Connect to OK pin of other Z-POLs and/or DPM. Leave floating, if not used
EN	15			Connect to PGND	Connect to PGND
VREF	16			Not Used	Leave floating
IM	17			Not Used	Leave floating
NC	18			Not Used	Leave floating
VOUT	19-23	P		Output Voltage	
+VS	24	I	PU	Positive Voltage Sense	Connect to the positive point close to the load
PGND	25-30	P		Power Ground	
-VS	31	I	PU	Negative Voltage Sense	Connect to the negative point close to the load
VIN	32-36	P		Input Voltage	

Legend: I=input, O=output, I/O=input/output, P=power, A=analog, PU=internal pull-up

8. Programmable Features

Performance parameters of ZY7007 POL converters can be programmed via the industry standard I²C communication bus without replacing any components or rewiring PCB traces. Each parameter has a default value stored in the volatile memory registers detailed in Table 1. The setup registers 00h through 14h are programmed at the system power-up. When the user programs new performance parameters, the values in the registers are overwritten. Upon removal of the input voltage, the default values are restored.

Table 1. ZY7007 Memory Registers

Register	Content	Address
PC1	Protection Configuration 1	00h
PC2	Protection Configuration 2	01h
PC3	Protection Configuration 3	02h
DON	Turn-On Delay	05h
DOF	Turn-Off Delay	06h
TC	Tracking Configuration	03h
INT	Interleave Configuration and Frequency Selection	04h
RUN	RUN Register	15h
ST	Status Register	16h
VOS	Output Voltage Setpoint	07h
CLS	Current Limit Setpoint	08h
DCL	Duty Cycle Limit	09h
B1	Dig Controller Denominator z^{-1} Coefficient	0Ah
B2	Dig Controller Denominator z^{-2} Coefficient	0Bh
B3	Dig Controller Denominator z^{-3} Coefficient	0Ch
C0L	Dig Controller Numerator z^{0} Coefficient, Low Byte	0Dh
C0H	Dig Controller Numerator z^{0} Coefficient, High Byte	0Eh
C1L	Dig Controller Numerator z^{-1} Coefficient, Low Byte	0Fh
C1H	Dig Controller Numerator z^{-1} Coefficient, High Byte	10h
C2L	Dig Controller Numerator z^{-2} Coefficient, Low Byte	11h
C2H	Dig Controller Numerator z^{-2} Coefficient, High Byte	12h
C3L	Dig Controller Numerator z^{-3} Coefficient, High Byte	13h
C3H	Dig Controller Numerator z^{-3} Coefficient, Low Byte	14h
VOM	Output Voltage Monitoring	17h
IOM	Output Current Monitoring	18h
TMP	Temperature Monitoring	19h

ZY7007 converters can be programmed using the Graphical User Interface or directly via the I²C bus by using high and low level commands as described in the ”ZM7300 Programming Manual”.

ZY7007 parameters can be reprogrammed at any time during the system operation and service except for the digital filter coefficients, the switching frequency and the duty cycle limit, that can only be changed when the POL is turned off.

8.1 Output Voltage

The output voltage can be programmed in the POL Output Configure window shown in the Figure 25 or directly via the I²C bus by writing into the VOS register shown in Figure 26.

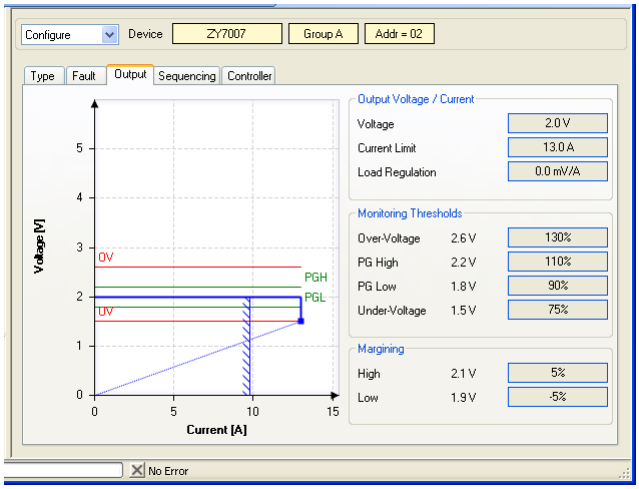

Figure 25. Output Configuration Window

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
VOS7	VOS6	VOS5	VOS4	VOS3	VOS2	VOS1	VOS0
Bit 7							Bit 0

Bit 7:0 **VOS[7:0]**, Output voltage setting
00h: corresponds to 0.5000V
01h: corresponds to 0.5125V
…
77h: corresponds to 1.9875V
78h: corresponds to 2.0000V
79h: corresponds to 2.025V
…
F9h: corresponds to 5.225V
FAh: corresponds to 5.250V
FBh: corresponds to 5.300V
…
FFh: corresponds to 5.500V

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as ‘0’
- n = Value at POR reset

Figure 26. Output Voltage Setpoint Register VOS

8.1.1 Output Voltage Setpoint

The output voltage programming range is from 0.5V to 5.5V. Within this range, there are 256 predefined voltage set points. To improve resolution of the output voltage settings, the voltage range is divided into three sub-ranges as shown in Table 2.

Table 2. Output Voltage Adjustment Resolution

$V_{OUT\ MIN}$, V	$V_{OUT\ MAX}$, V	Resolution, mV
0.500	2.000	12.5
2.025	5.25	25
5.3	5.5	50

8.1.2 Output Voltage Margining

If the output voltage needs to be varied by a certain percentage, the margining function can be utilized. The margining can be programmed in the POL Configuration window or directly via the I^2C bus using high level commands as described in the "ZM7300 Digital Power Manager Programming Manual".

In order to properly margin POLs that are connected in parallel, the POLs must be members of one of the Parallel Buses. Refer to the DPM Configure Devices window shown in Figure 53.

8.1.3 Optimal Voltage Positioning

Optimal voltage positioning increases the voltage regulation window by properly positioning the output voltage setpoint. Positioning is determined by the load regulation that can be programmed in the POL Configure Output window shown in Figure 25 or directly via the I^2C bus by writing into the CLS register shown in Figure 36.

Figure 27 illustrates optimal voltage positioning concept. If no load regulation is programmed, the headroom (voltage differential between the output voltage setpoint and a regulation limit) is approximately half of the voltage regulation window. When load regulation is programmed, the output voltage will decrease as the output current increases, so the VI characteristic will have a negative slope. Therefore, by properly selecting the operating point, it is possible to increase the headroom as shown in the picture.

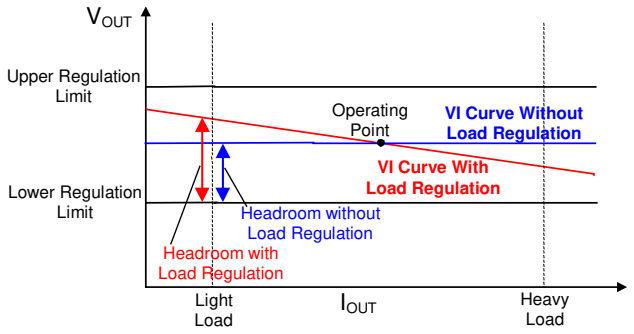

Figure 27. Optimal Voltage Positioning Concept

Increased headroom allows tolerating larger voltage deviations. For example, the step load change from light to heavy load will cause the output voltage to drop. If the optimal voltage positioning is utilized, the output voltage will stay within the regulation window. Otherwise, the output voltage will drop below the lower regulation limit. To compensate for the voltage drop external output capacitance will need to be added, thus increasing cost and complexity of the system.

The effect of optimal voltage positioning is shown in Figure 28 and Figure 29. In this case, switching output load causes large peak-to-peak deviation of the output voltage. By programming load regulation, the peak to peak deviation is dramatically reduced.

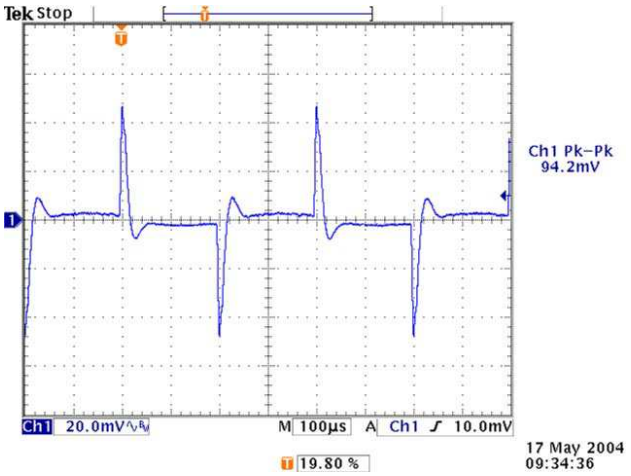

Figure 28. Transient Response without Optimal Voltage Positioning

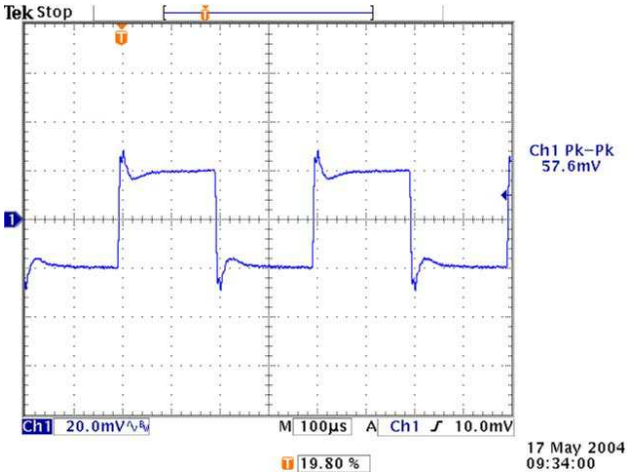

Figure 29. Transient Response with Optimal Voltage Positioning

8.2 Sequencing and Tracking

Turn-on delay, turn-off delay, and rising and falling output voltage slew rates can be programmed in the POL Configure Sequencing window shown in Figure 30 or directly via the I^2C bus by writing into the DON, DOF, and TC registers, respectively. The registers are shown in Figure 31, Figure 32, and Figure 34.

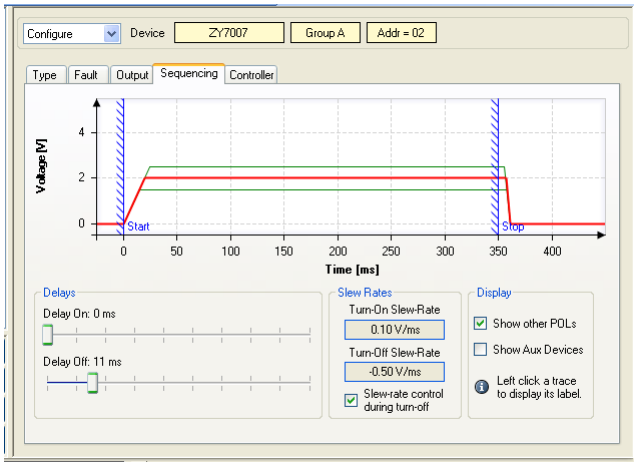

Figure 30. POL Configure Sequencing Window

8.2.1 Turn-On Delay

Turn-on delay is defined as an interval from the application of the Turn-On command until the output voltage starts ramping up.

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DON7	DON6	DON5	DON4	DON3	DON2	DON1	DON0
Bit 7							Bit 0

Bit 7:0 **DON[7:0]**: Turn-on delay time
00h: corresponds to 0ms delay after turn-on command has occurred
…
FFh: corresponds to 255ms delay after turn-on command has occurred

Figure 31. Turn-On Delay Register DON

8.2.2 Turn-Off Delay

U	U	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
---	---	DOF5	DOF4	DOF3	DOF2	DOF1	DOF0
Bit 7							Bit 0

Bit 7:6 **Unimplemented**, read as '0'

Bit 5:0 **DOF[5:0]**: Turn-off delay time
00h: corresponds to 0ms delay after turn-off command has occurred
…
3Fh: corresponds to 63ms delay after turn-off command has occurred

Figure 32. Turn-Off Delay Register DOF

Turn-off delay is defined as an interval from the application of the Turn-Off command until the output voltage reaches zero (if the falling slew rate is programmed) or until both high side and low side switches are turned off (if the slew rate is not programmed). Therefore, for the slew rate controlled turn-off the ramp-down time is included in the turn-off delay as shown in Figure 33.

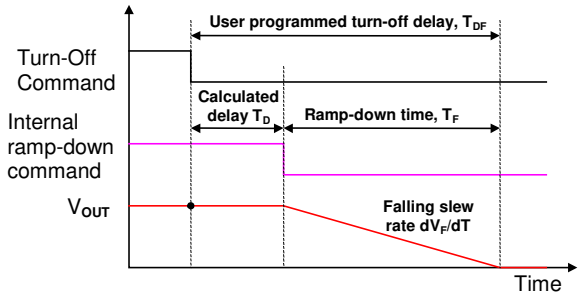

Figure 33. Relationship between Turn-Off Delay and Falling Slew Rate

As it can be seen from the figure, the internally calculated delay T_D is determined by the equation below.

$$T_D = T_{DF} - \frac{V_{OUT}}{dV_F/dT},$$

For proper operation T_D shall be greater than zero. The appropriate value of the turn-off delay needs to be programmed to satisfy the condition.

If the falling slew rate control is not utilized, the turn-off delay only determines an interval from the application of the Turn-Off command until both high side and low side switches are turned off. In this case, the output voltage ramp-down process is determined by load parameters.

8.2.3 Rising and Falling Slew Rates

The output voltage tracking is accomplished by programming the rising and falling slew rates of the output voltage. To achieve programmed slew rates, the output voltage is being changed in 12.5mV steps where duration of each step determines the slew rate. For example, ramping up a 1.0V output with a slew rate of 0.5V/ms will require 80 steps duration of 25µs each.

Duration of each voltage step is calculated by dividing the master clock frequency generated by the DPM. Since all POLs in the system are synchronized to the master clock, the matching of voltage slew rates of different outputs is very accurate as it can be seen in Figure 8 and Figure 12.

During the turn on process, a POL not only delivers current required by the load (I_{LOAD}), but also charges the load capacitance. The charging current can be determined from the equation below:

$$I_{CHG} = C_{LOAD} \times dV_R/dt$$

Where, C_{LOAD} is load capacitance, dV_R/dt is rising voltage slew rate, and I_{CHG} is charging current.

When selecting the rising slew rate, a user needs to ensure that

$$I_{LOAD} + I_{CHG} < I_{OCP}$$

Where I_{OCP} is the overcurrent protection threshold of the ZY7007. If the condition is not met, then the overcurrent protection will be triggered during the turn-on process. To avoid this, dV_R/dt and the overcurrent protection threshold should be programmed to meet the condition above.

U	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0
---	R2	R1	R0	SC	F2	F1	F0
Bit 7							Bit 0

Bit 7 **Unimplemented** , read as '0'

Bit 6:4 **R[2:0]**: Value of Vo rising slope
0: corresponds to 0.1V/ms (default)
1: corresponds to 0.2V/ms
2: corresponds to 0.5V/ms
3: corresponds to 1.0V/ms
4: corresponds to 2.0V/ms
5: corresponds to 5.0V/ms
6: corresponds to 8.3V/ms
7: corresponds to 8.3V/ms

Bit 3 **SC**, Slew rate control at turn-off
0: Slew rate control is disabled
1: Slew rate control is enabled

Bit 2:0 **F[2:0]**: Value of Vo falling slope
0: corresponds to -0.1V/ms (default)
1: corresponds to -0.2V/ms
2: corresponds to -0.5V/ms
3: corresponds to -1.0V/ms
4: corresponds to -2.0V/ms
5: corresponds to -5.0V/ms
6: corresponds to –8.3V/ms
7: corresponds to –8.3V/ms

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

Figure 34. Tracking Configuration Register TC

8.3 Fault and Error Protection

ZY7007 Series converters have a comprehensive set of programmable fault and error protection provisions. The set includes the output over- and undervoltage protection, overcurrent protection, overtemperature protection, tracking protection, overtemperature warning, and Power Good signal. Status of protection logic is stored in the ST register shown in Figure 35.

R-1	R-0	R-1	R-1	R-1	R-1	R-1	R-1
TP	PG	TR	OT	OC	UV	OV	PV
Bit 7							Bit 0

Bit 7 **TP**: Temperature Warning
Bit 6 **PG**: Power Good Warning
Bit 5 **TR**: Tracking Fault
Bit 4 **OT**: Overtemperature Fault
Bit 3 **OC**: Overcurrent Fault
Bit 2 **UV**: Undervoltage Fault
Bit 1 **OV**: Overvoltage Error
Bit 0 **PV**: Phase Voltage Error

Note:
- An activated warning/fault/error is encoded as '0'

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

Figure 35. Protection Status Register ST

Thresholds of overcurrent, over- and undervoltage protection responses, and Power Good limits can be programmed in the POL Configure Output window or directly via the I^2C bus by writing into the CLS and PC2 registers shown in Figure 36 and Figure 37.

R/W-0	R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-1	R/W-1
LR2	LR1	LR0	TCE	CLS3	CLS2	CLS1	CLS0
Bit 7							Bit 0

Bit 7:5 **LR[2:0]**, Load regulation configuration
000: 0 V/A/Ohm
001: 0.39 V/A/Ohm
010: 0.78 V/A/Ohm
011: 1.18 V/A/Ohm
100: 1.57 V/A/Ohm
101: 1.96 V/A/Ohm
110: 2.35 V/A/Ohm
111: 2.75 V/A/Ohm

Bit 4 **TCE**, Temperature compensation enable
0: disabled
1: enabled

Bit 3:0 **CLS[3:0]**, Current limit setting
0h: corresponds to 37%
1h: corresponds to 47%
…
Bh: corresponds to 140%
Values higher than Bh are translated to Bh (140%)

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

Figure 36. Current Limit Setpoint Register CLS

U	U	U	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0
---	---	---	PGLL	OVPL1	OVPL0	UVPL1	UVPL0
Bit 7							Bit 0

Bit 7:5 **Unimplemented**, read as '0'
Bit 4 **PGLL**: Set Power Good Low Level
1 = 95% of Vo
0 = 90% of Vo (Default)

Bit 3:2 **OVPL[1:0]**: Set Over Voltage Protection Level
00 = 110% of Vo
01 = 120% of Vo
10 = 130% of Vo (Default)
11 = 130% of Vo

Bit 1:0 **UVPL[1:0]**: Set Under Voltage Protection Level
00 = 75% of Vo (Default)
01 = 80% of Vo
10 = 85% of Vo

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

Figure 37. Protection Configuration Register PC2

Note that the overvoltage and undervoltage protection thresholds and Power Good limits are defined as percentages of the output voltage. Therefore, the absolute levels of the thresholds change when the output voltage setpoint is changed either by output voltage adjustment or by margining.

In addition, a user can change protection between latching and non-latching, or disable certain protection responses entirely. These settings are programmed in the POL Configure Fault window shown in Figure 38 or directly via the I^2C by writing into the PC1 register shown in Figure 39.

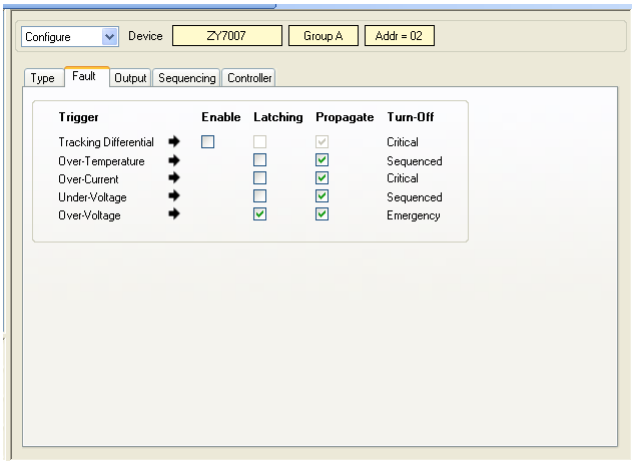

Figure 38. POL Configure Fault Window

R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1
TRE	PVE	TRP	OTP	OCP	UVP	OVP	PVP
Bit 7							Bit 0

Bit 7 **TRE**: Tracking fault enable
1 = enabled
0 = disabled

Bit 6 **PVE**: Phase voltage error enable
1 = enabled
0 = disabled

Bit 5 **TRP**: Tracking fault protection
1 = latching
0 = non latching

Bit 4 **OTP**: Overtemperature protection configuration
1 = latching
0 = non latching

Bit 3 **OCP**: Overcurrent protection configuration
1 = latching
0 = non latching

Bit 2 **UVP**: Undervoltage protection configuration
1 = latching
0 = non latching

Bit 1 **OVP**: Overvoltage protection configuration
1 = latching
0 = non latching

Bit 0 **PVP**: Phase Voltage Protection
1 = latching
0 = non latching

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

Figure 39. Protection Configuration Register PC1

If the non-latching protection is selected, a POL will attempt to restart every 130ms until the condition that triggered the protection is removed. When restarting, the output voltages follow tracking and sequencing settings.

If the latching type is selected, a POL will turn off and stay off. The POL can be turned on after 130ms, if the condition that caused the fault is removed and the respective bit in the ST register was cleared, or the Turn On command was recycled, or the input voltage was recycled.

All protection functions can be classified into three groups based on their effect on system operation: warnings, faults, and errors.

8.3.1 Warnings

This group includes Overtemperature Warning and Power Good Signal. The warnings do not turn off POLs but rather generate signals that can be transmitted to a host controller via the I^2C bus.

8.3.1.1 Overtemperature Warning

The Overtemperature Warning is generated when temperature of the controller exceeds 120°C. The Overtemperature Warning changes the PT bit of the status register ST to 0 and sends the signal to the DPM. Reporting is enabled in the DPM Configuration Fault management window or directly via the I^2C by writing into the PC3 register shown in Figure 41. When the temperature falls below 117°C, the PT bit is cleared and the Overtemperature Warning is removed.

8.3.1.2 Power Good

Power Good is an open collector output that is pulled low, if the output voltage is outside of the Power Good window. The window is formed by the Power Good High threshold that is equal to 110% of the output voltage and the Power Good Low threshold that can be programmed at 90 or 95% of the output voltage.

The Power Good protection is only enabled after the output voltage reaches its steady state level. The PG pin is pulled low during transitions of the output voltage from one level to other as shown in Figure 40.

The Power Good Warning pulls the Power Good pin low and changes the PG bit of the status register ST to 0. It sends the signal to the DPM, if the reporting is enabled. When the output voltage returns within the Power Good window, the PG pin is pulled high, the PG bit is cleared and the Power Good Warning is removed. The Power Good pin can also be pulled low by an external circuit to initiate the Power Good Warning.

Note: To retrieve status information, Status Monitoring in the GUI DPM Configure Devices window should be enabled (refer to Digital Power Manager Data Sheet). The DPM will retrieve the status information from each POL on a continuous basis.

8.3.2 Faults

This group includes overcurrent, overtemperature, undervoltage, and tracking protection settings. Triggering any protection in this group will turn off the POL.

8.3.2.1 Overcurrent Protection

Overcurrent protection is active whenever the output voltage of the POL exceeds the prebias voltage (if any). When the output current reaches the OC threshold, the output voltage will start decreasing. As soon as the output voltage decreases below the undervoltage protection threshold, the OC fault signal is generated, the POL turns off and the OC bit in the register ST is changed to 0. Both high side and low side switches of the POL are turned off instantly (fast turn-off).

The temperature compensation is added to keep the OC threshold approximately constant at temperatures above room temperature. Note that the temperature compensation can be disabled in the POL Configure Output window or directly via the I^2C by writing into the CLS register. However, it is recommended to keep the temperature compensation enabled.

8.3.2.2 Undervoltage Protection

The undervoltage protection is only active during steady state operation of the POL to prevent nuisance tripping. If the output voltage decreases below the UV threshold and there is no OC fault, the UV fault signal is generated, the POL turns off, and the UV bit in the register ST is changed to 0. The output voltage is ramped down according to sequencing and tracking settings (regular turn-off).

8.3.2.3 Overtemperature Protection

Overtemperature protection is active whenever the POL is powered up. If temperature of the controller exceeds 130°C, the OT fault is generated, POL turns off, and the OT bit in the register ST is changed to 0. The output voltage is ramped down according to sequencing and tracking settings (regular turn-off).

If non-latching OTP is programmed, the POL will restart as soon as the temperature of the controller decreases below the Overtemperature Warning threshold of 120°C.

8.3.2.4 Tracking Protection

Tracking protection is active only when the output voltage is ramping up. The purpose of the protection is to ensure that the voltage differential between multiple rails being tracked does not exceed 250mV. This protection eliminates the need for external clamping diodes between different voltage rails which are frequently recommended by ASIC manufacturers.

When the tracking protection is enabled, the POL continuously compares actual value of the output voltage to its programmed value as defined by the output voltage and its rising slew rate. If absolute value of the difference exceeds 250mV, the tracking fault signal is generated, the POL turns off, and the TR bit in the register ST is changed to 0. Both high side and low side switches of the POL are turned off instantly (fast turn-off).

The tracking protection can be disabled, if it contradicts requirements of a particular system (for example turning into high capacitive load where rising slew rate is not important). It can be disabled in the POL Configure Fault window or directly via the I^2C bus by writing into the PC1 register.

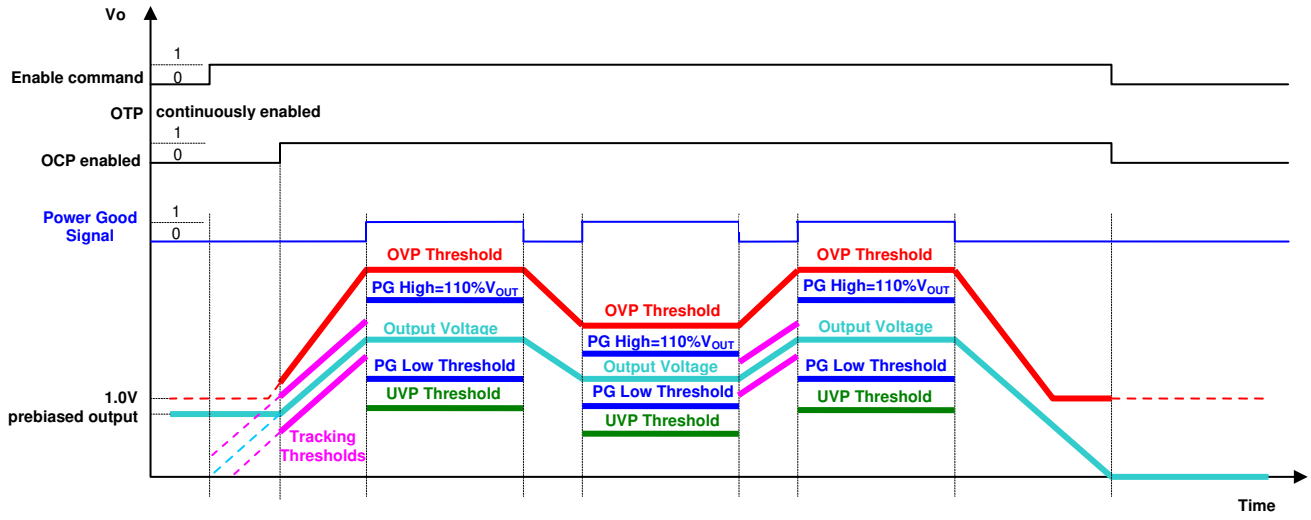

Figure 40. Protection Enable Conditions

8.3.3 Errors

The group includes overvoltage protection and the phase voltage error. The phase voltage error is not available in ZY7007.

8.3.3.1 Overvoltage Protection

The overvoltage protection is active whenever the output voltage of the POL exceeds the pre-bias voltage (if any). If the output voltage exceeds the overvoltage protection threshold, the overvoltage error signal is generated, the POL turns off, and the OV bit in the register ST is changed to 0. The high side switch is turned off instantly, and simultaneously the low side switch is turned on to ensure reliable protection of sensitive loads. The low side switch provides low impedance path to quickly dissipate energy stored in the output filter and achieve effective voltage limitation.

The OV threshold can be programmed from 110% to 130% of the output voltage setpoint, but not lower than 1.0V.

8.3.4 Faults and Errors Propagation

The feature adds flexibility to the fault management scheme by giving users control over propagation of fault signals within and outside of the system. The propagation means that a fault in one POL can be programmed to turn off other POLs and devices in the system, even if they are not directly affected by the fault.

8.3.4.1 Grouping of POLs

Z-Series POLs can be arranged in several groups to simplify fault management. A group of POLs is defined as a number of POLs with interconnected OK pins. A group can include from 1 to 32 POLs. If

fault propagation within a group is desired, the propagation bit needs to be checked in the DPM Configure Faults window. The parameters can also be programmed directly via the I^2C bus by writing into the PC3 register shown in Figure 41.

When propagation is enabled, the faulty POL pulls its OK pin low. A low OK line initiates turn-off of other POLs in the group.

R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
PTM	PGM	TRP	OTP	OCP	UVP	OVP	PVP
Bit 7							Bit 0

Bit 7 **PTM**: Temperature warning Message
1 = enabled
0 = disabled

Bit 6 **PGM**: Power good message
1 = enabled
0 = disabled

Bit 5 **TRP**: Tracking fault propagation
1 = enabled
0 = disabled

Bit 4 **OTP**: Overtemperature fault propagation
1 = enabled
0 = disabled

Bit 3 **OCP**: Overcurrent fault propagation
1 = enabled
0 = disabled

Bit 2 **UVP**: Undervoltage fault propagation
1 = enabled
0 = disabled

Bit 1 **OVP**: Overvoltage error propagation
1 = enabled
0 = disabled

Bit 0 **PVP**: Phase voltage error propagation
1 = enabled
0 = disabled

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

Figure 41. Protection Configuration Register PC3

In addition, the OK lines can be connected to the DPM to facilitate propagation of faults and errors between groups. One DPM can control up to 4 independent groups. To enable fault propagation between groups, the respective bit needs to be checked in the DPM Configure Faults window, Group Fault Propagation sub window shown in Figure 42.

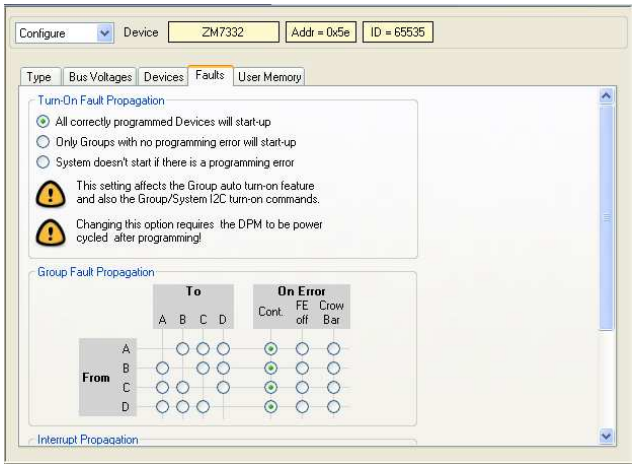

Figure 42. DPM Configure Faults Window

In this case low OK line will signal DPM to pull other OK lines low to initiate shutdown of other POLs as programmed in the Group Fault Propagation window. If an error is propagated, the DPM can also generate commands to turn off a front end (a DC-DC converter generating the intermediate bus voltage) and trigger an optional crowbar protection to accelerate removal of the IBV voltage.

8.3.4.2 Propagation Process

Propagation of a fault (OCP, UVP, OTP, and TRP) initiates regular turn-off of other POLs. The faulty POL in this case performs either the regular or the fast turn-off depending on a specific fault as described in section 8.3.2.

Propagation of an error initiates fast turn-off of other POLs. The faulty POL performs the fast turn-off and turns on its low side switch.

Example of the fault propagation is shown in Figure 43 - Figure 44. In this three-output system (refer to the block diagram in Figure 23), the POL powering the output V3 (Ch 1 in the picture) encounters the undervoltage fault after the turn-on. When the fault propagation is not enabled, the POL turns off and generates the UV fault signal. Because the UV fault triggers the regular turn off, the POL meets its turn-off delay and falling slew rate settings during the turn-ff process as shown in Figure 43. Since the UV fault is programmed to be non-latching, the POL will attempt to restart every 130ms, repeating the process described above until the condition causing the undervoltage is removed.

If the fault propagation between groups is enabled, the POL powering the output V3 pulls its OK line low and the DPM propagates the signal to the POL powering the output V1 that belongs to other group. The POL powering the output V1 (Ch3 in the picture) executes the regular turn-off. Since both V1 and V3 have the same delay and slew rate settings they will continue to turn off and on synchronously every 130ms as shown in Figure 44 until the condition causing the undervoltage is removed. The POL powering the output V2 continues to ramp up until it reaches its steady state level.

130ms is the interval from the instant of time when the output voltage ramps down to zero until the output voltage starts to ramp up again. Therefore, the 130ms hiccup interval is guaranteed regardless of the turn-off delay setting.

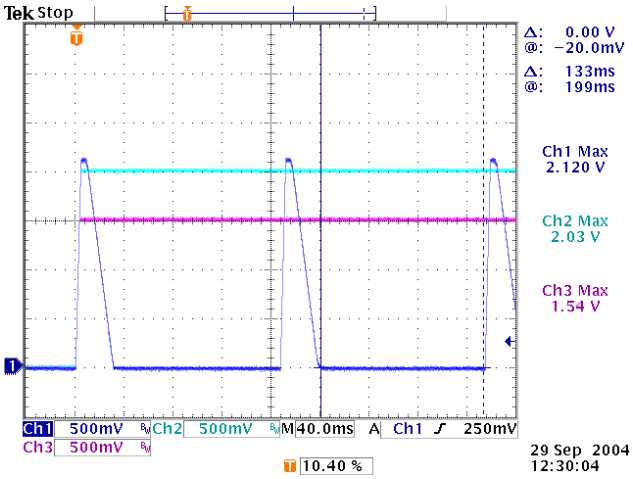

Figure 43. Turn-On into UVP on V3. The UV Fault Is Programmed To Be Non-Latching. Ch1 – V3 (Group C), Ch2 – V2, Ch3 – V1 (Group A)

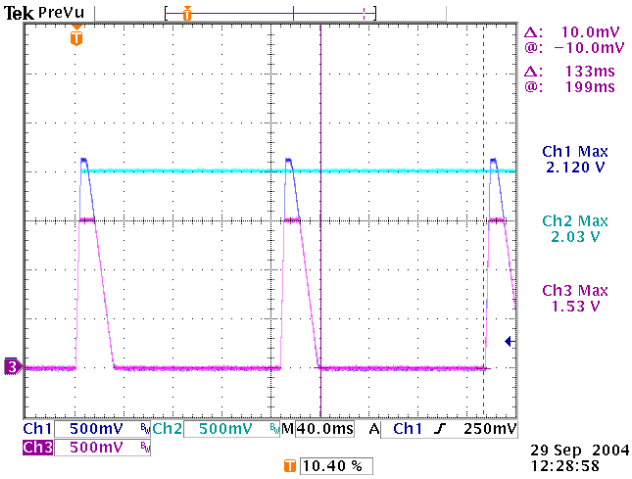

Figure 44. Turn-On into UVP on V3. The UV Fault Is Programmed To Be Non-Latching and Propagate From Group C to Group A. Ch1 – V3 (Group C), Ch2 – V2, Ch3 – V1 (Group A)

Summary of protection support, their parameters and features are shown in Table 3

Table 3. Summary of Protection Parameters and Features

Code	Name	Type	When Active	Turn Off	Low Side Switch	Propagation	Disable
PT	Pretemperature Warning	Warning	Whenever V_{IN} is applied	No	N/A	Readable by DPM	No
PG	Power Good	Warning	During steady state	No	N/A	Readable DPM	No
TR	Tracking	Fault	During ramp up	Fast	Off	Regular turn off	Yes
OT	Overtemperature	Fault	Whenever V_{IN} is applied	Regular	Off	Regular turn off	No
OC	Overcurrent	Fault	When V_{OUT} exceeds prebias	Fast	Off	Regular turn off	No
UV	Undervoltage	Fault	During steady state	Regular	Off	Regular turn off	No
OV	Overvoltage	Error	When V_{OUT} exceeds prebias	Fast	On	Fast turn off	No